1 Mb High Speed Quad I/O SPI MRAM

FEATURES

- High bandwidth – Read and Write at 52MB/sec
- Quad I/O with the use of dual purpose pins to maintain a low pin count
- Operates in both standard, single SPI mode and high speed quad SPI mode
- Fast quad Read and Write with quad address input and quad I/O
- Intended for next generation RAID controllers, server system logs, storage device buffers, and embedded system data and program memory
- Data is non-volatile with retention greater than 20 years
- Automatic data protection on power loss
- Unlimited write endurance
- Low-current sleep mode
- Tamper detect feature
- Dual 3.3v V_{DD} / 1.8v V_{DDQ} power supply
- Available in a 16-pin SOIC RoHS-compliant package
- Quad Peripheral Interface (QPI) mode is supported to enhance system performance in XIP

RoHS

16-SOIC

DESCRIPTION

The MR10Q010 Quad SPI MRAM is a high bandwidth extension of our SPI MRAM product offering. It is a 1,048,576-bit magnetoresistive random access memory (MRAM) device organized as 131,072 words of 8 bits. Four I/O's allow very fast reads and writes, making it an attractive alternative to conventional parallel data bus interfaces in next generation RAID controllers, server system logs, storage device buffers, and embedded system data and program memory.

Unlike other serial memories, both reads and writes can occur randomly in memory with no delay between writes. Standard Serial Peripheral Interface (SPI) and Quad SPI modes are supported at a clock rate up to 104MHz. The MR10Q010 is the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of pins, low power, and space saving packages.

1MB HIGH SPEED QUAD I/O SPI MRAM

Density	Interface	Voltage (V)	Read/ Write	Active Current R/W (mA)	Standby Current (mA)	Sleep Current (µA)	Package
1 Mb	104MHz Quad SPI	3.3/1.8 V_{DDQ}	52MB/sec	80/200	5.0	100	16-SOIC

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OVERVIEW

The Serial Peripheral Interface, SPI, is becoming increasingly popular in system design due to the reduced pin count of the serial interface and increasing data bandwidth offered when compared against x8 or x16 parallel interface architectures. The SPI interface has evolved from a single data line to a four data line, or quad architecture. This interface provides a data bandwidth in excess of 50Mbytes/sec.

SPI is currently well-established in microcontroller/microprocessor based systems. The Everspin family of single I/O SPI MRAM is popular in smart meter applications and a variety of other embedded systems. However, the 40MHz limitation with a single data I/O is too slow for higher performance applications such as the next generation RAID controllers, server system logs, and storage device buffers .

Operating at 52MB/second for both Read and Write the Everspin 1Mb Quad I/O SPI MRAM will meet the needs of these applications. And as a non-volatile memory with over 20 years of data retention, this SPI memory family is equally suited for embedded system data and program memory.

The Quad Peripheral Interface, QPI, mode provides a lower overhead to load commands, which will improve system throughput when operating in an Execute in Place, XIP, environment. This added feature will make the device attractive in embedded applications that store program code in an external memory. QPI effectively increases the effective clock rate and, when combined with Quad SPI instructions, Quad SPI memory performance will outstrip asynchronous parallel memories.

Figure 1 – Block Diagram

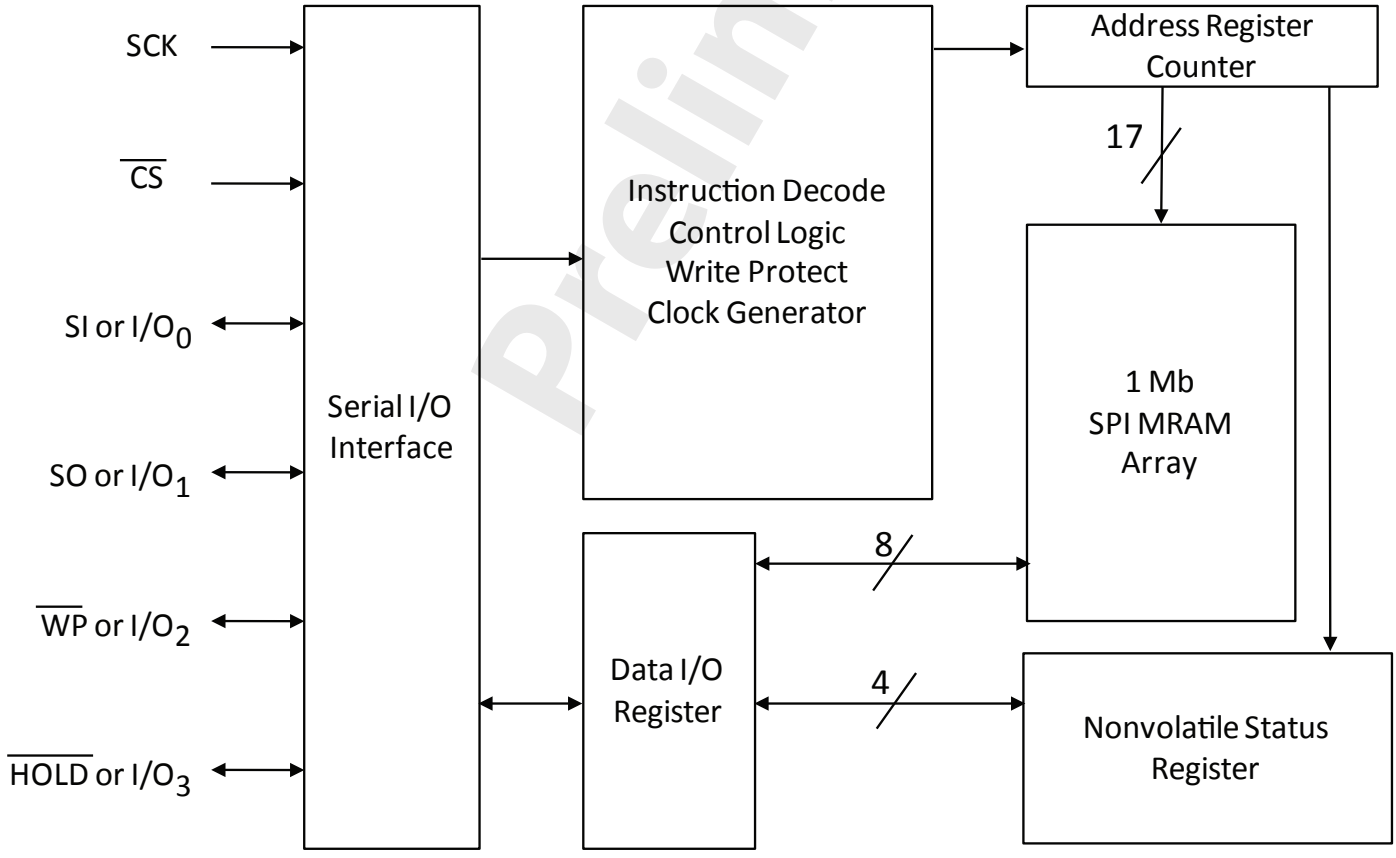


Figure 2 – System Configuration

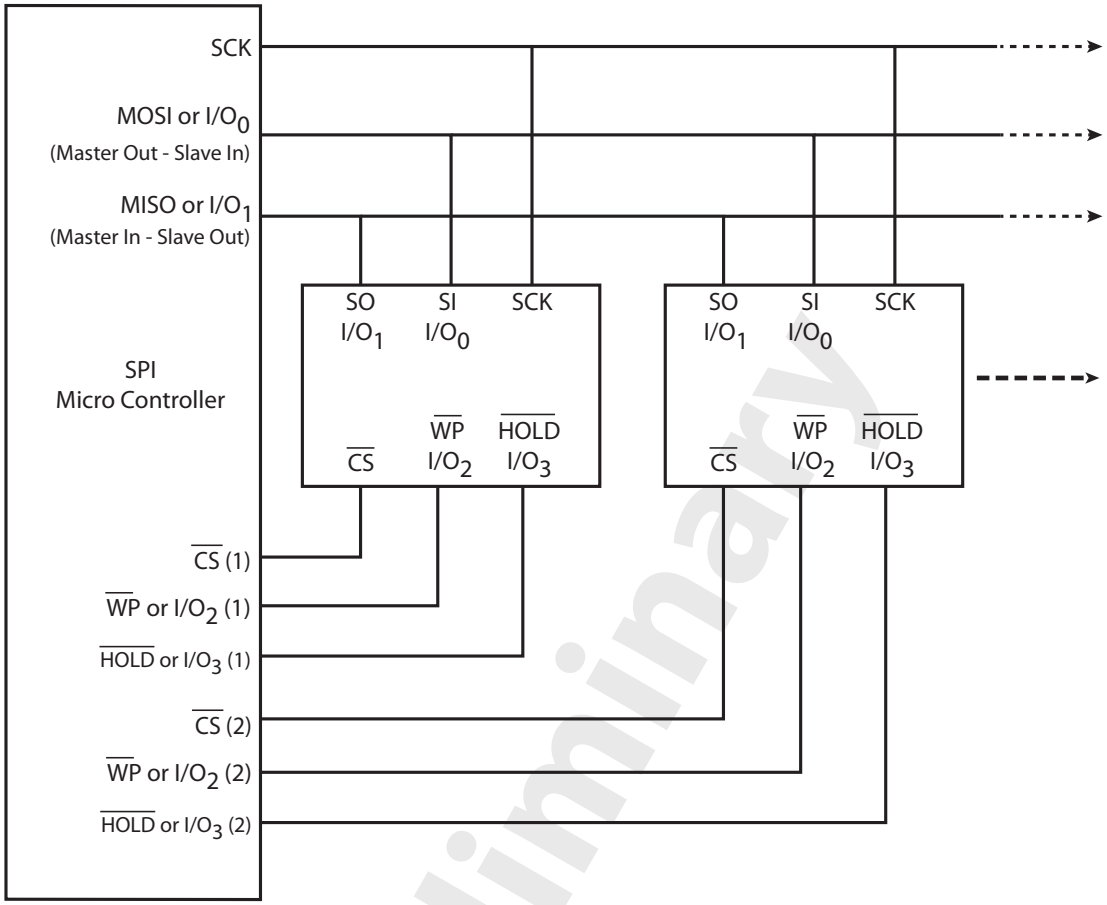


Figure 3 – Block Diagram

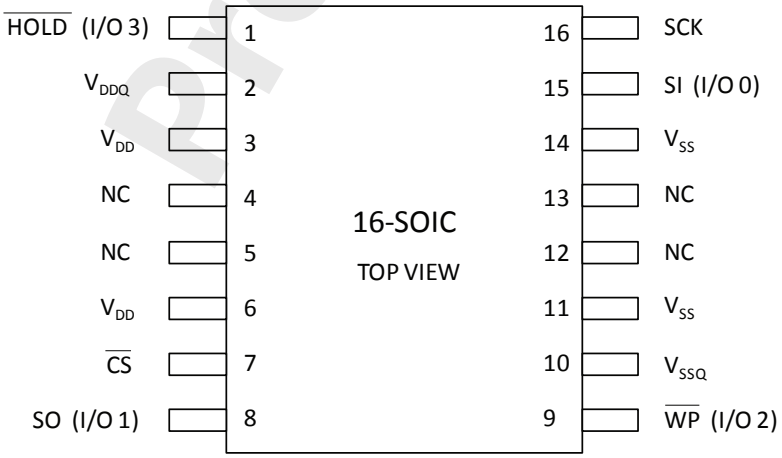


Table 1 – Pin Functions

Signal Name	Pin	SPI Mode	Quad SPI Mode [1]	Description
$\overline{CS}$	7	Chip Select	Chip Select	An active low chip select for the serial MRAM. When chip select is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z. Multiple serial memories can share a common set of data pins by using a unique chip select for each memory.
SO (I/O_1)	8	Serial Output	I/O_1	SPI Mode: The data output pin is driven during a read operation and remains Hi-Z at all other times. SO is Hi-Z when $\overline{HOLD}$ is low. Data transitions on the data output occur on the falling edge of SCK. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
$\overline{WP}$ (I/O_2)	9	Write Protect	I/O_2	SPI Mode: A low on the write protect input prevents write operations to the Status Register. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
V_{SS}	11, 14	Ground	Ground	Power supply ground pin.
V_{SSQ}	10	Ground	Ground	I/O Voltage ground pin.
SI (I/O_0)	15	Serial Input	I/O_0	SPI Mode: All data is input to the device through this pin. This pin is sampled on the rising edge of SCK and ignored at other times. SI can be tied to SO to create a single bidirectional data bus if desired. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.

Table continues on next page.

Pin Functions - Continued

Signal Name	Pin	SPI Mode	Quad SPI Mode [1]	Description
SCK	16	Clock	Clock	Synchronizes the operation of the MRAM. The clock can operate up to 104 MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high. Memory operation is static so the clock can be stopped at any time.
$\overline{\text{HOLD}}$ (I/O_3)	1	$\overline{\text{HOLD}}$	I/O_3	SPI Mode: A low on the $\overline{\text{HOLD}}$ pin interrupts a memory operation for another task. When $\overline{\text{HOLD}}$ is low, the current operation is suspended. The device will ignore transitions on the $\overline{\text{CS}}$ and SCK when $\overline{\text{HOLD}}$ is low. All transitions of $\overline{\text{HOLD}}$ must occur while $\overline{\text{CS}}$ is low. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK.
V_{DD}	3, 6	Power Supply	Power Supply	Power supply voltage from +3.0 to +3.6 volts.
V_{DDQ}	2	I/O Bus Power Supply	I/O Bus Power Supply	I/O Bus supply voltage from +1.7 volts to +1.9 volts.

SPI COMMUNICATIONS PROTOCOL

The MR10Q010 can be operated in either SPI Mode 0 (CPOL=0, CPHA =0) or SPI Mode 3 (CPOL=1, CPHA=1). For both modes, inputs are captured on the rising edge of the clock and data outputs occur on the falling edge of the clock. When not conveying data, SCK remains low for Mode 0; while in Mode 3, SCK is high. The memory determines the mode of operation (Mode 0 or Mode 3) based upon the state of the SCK when $\overline{CS}$ falls.

All memory transactions start when $\overline{CS}$ is brought low to the memory. The first byte is a command code. Depending upon the command, subsequent bytes of address are input. Data is either input or output. There is only one command performed per $\overline{CS}$ active period. $\overline{CS}$ must go inactive before another command can be accepted. To ensure proper part operation according to specifications, it is necessary to terminate each access by raising $\overline{CS}$ at the end of a byte (a multiple of 8 clock cycles from $\overline{CS}$ dropping to avoid partial or aborted accesses.

Command Codes

Table 2 – SPI Mode Command Codes

		Clock Number					
Instruction	**Description**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - 47
WREN	Write Enable	06h	-	-	-	-	-
WRDI	Write Disable	04h	-	-	-	-	-
RDSR	Read Status Register	05h	S7-S0	-	-	-	-
WRSR	Write Status Register	01h	S7-S0	-	-	-	-
READ	Read Data Bytes	03h	A23-A16	A15-A8	A7-A0	D7-D0	-
FREAD	Fast Read Data Bytes	0Bh	A23-A16	A15-A8	A7-A0	Dummy (7-0)	D7-D0, until $\overline{CS}$ high
WRITE	Write Data Bytes	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0, until $\overline{CS}$ high
SLEEP	Enter Sleep Mode	B9h	-	-	-	-	-
WAKE	Exit Sleep Mode	ABh	-	-	-	-	-
TDET	Tamper Detect	TBD	TBD	TBD	TBD	TBD	TBD
RDID	Read ID	4Bh	Dummy Clocks 8 - 15	Device ID [2] Clocks 16 - 55	-	-	-

Notes:
1. Clocks 0 - 7 are the command byte.
2. The Device ID is contained within 40 bits following the 8 dummy clocks. See "Read ID (RDID)" on page 22 for more details.

Table 3 – Quad SPI Mode Command Codes

		Clock Number					
Instruction	**Description**	0 - 7 [1]	8 - 15	16 - 23	24 - 31	32 - 39	40 - 47
FRQO	Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	2 Dummy Clocks D7-D0 x4 [2]	D7-D0 x4
FRQAD	Fast Read Quad Address and Data	EBh	A23-A0 x4 2 Dummy Clocks	D7-D0 x4	-	-	-
FWQD	Fast Write Quad Data	32h	A23-A16	A15-A8	A7-A0	D7-D0 x4	-
FWQAD	Fast Write Quad Address and Data	12h	A23-A0 x4 D7-D0 x4	D7-D0 x4	-	-	-

Notes:
1. Clocks 0 - 7 are the command byte.
2. Data and address on all four IOs.

Table 4 – QPI Mode Command Codes

		Clock Number					
Instruction	**Description**	0 - 1 [1]	2 - 3	4 - 5	6 - 7	8 - 9	10 - 11
	Disable QPI	FFh	-	-	-	-	-
WREN	Write Enable	06h	-	-	-	-	-
WRDI	Write Disable	04h	-	-	-	-	-
RDSR	Read Status Register	05h	S7-S0	-	-	-	-
WRSR	Write Status Register	01h	S7-S0	-	-	-	-
FREAD	Fast Read Data Bytes	08h	A23-A16	A15-A8	A7-A0	Dummy	D7-D0
WRITE	Write Data Bytes	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0 until $\overline{CS}$ high
SLEEP	Enter Sleep Mode	B9h	-	-	-	-	-
WAKE	Exit Sleep Mode	ABh	-	-	-	-	-
RDID	Read ID	4Bh	Dummy	Device ID	-	-	-
FRQO	Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	?	D7-D0 x4
FWQD	Fast Write Quad Data	32h	A23-A16	A15-A8	A7-A0	-	

Notes:
1. Clocks 0 - 1 are the command bits.
2. Data and address on all four IOs.

Table 5 – QPI Command, Address and Data Clock Sequencing

	Clock Number											
	0	1	2	3	4	5	6	7	8	9	10	11
IO_0	C4	C0	A20	A16	A12	A8	A4	A0	D4	D0	D4	D0
IO_1	C5	C1	A21	A17	A13	A9	A5	A1	D5	D1	D5	D1
IO_2	C6	C2	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2
IO_3	C7	C3	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3

Notes:

1. C = Command bit; A = Address bit; D = Data bit
2. Command, Data and Address on all four IOs.

Status Register, Memory Protection and Block Write Protection

The status register consists of the 8 bits listed in Table 6 below. The Status Register Write Disable bit (SRWD) defined in "Table 7 – Memory Protection Modes" is used in conjunction with bit 1 (WEL) and the Write Protection pin ($\overline{WP}$) to provide hardware memory block protection. Bits BP0 and BP1 define the memory block arrays that are protected as described in Table 7. The fast writing speed of the MR10Q010 does not require write status bits. The state of bits 6,5,4, and 0 can be modified by the user and do not affect memory operation. All bits in the status register are pre-set at the factory to the "0" state.

Table 6 – Status Register Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRWD (Non volatile)	R3	R2	R1	BP1 (Non-Volatile)	BP0 (Non-Volatile)	WEL (Volatile)	R0

1. Notes:
2. SRWD - Status Register Write Disable
3. R3 - Reserved bit 3
4. R2 - Reserved bit 2
5. R1 - Reserved bit 1
6. BP1 - Block Protect bit 1
7. BP0 - Block Protect bit 0
8. WEL - Write Enable Latch
9. R0 - Reserved bit 0

Memory Protection Modes

When WEL is reset to 0, writes to all blocks and the status register are protected. When WEL is set to 1, BP0 and BP1 determine which memory blocks are protected. While SRWD is reset to 0 and WEL is set to 1, status register bits BP0 and BP1 can be modified. Once SRWD is set to 1, $\overline{WP}$ must be high to modify SRWD, BP0 and BP1.

Table 7 – Memory Protection Modes

WEL	SRWD	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Writable	Writable
1	1	Low	Protected	Writable	Protected
1	1	High	Protected	Writable	Writable

Block Protection Modes

The memory enters hardware block protection when the $\overline{WP}$ input is low and the Status Register Write Disable (SRWD) bit is set to 1. The memory leaves hardware block protection only when the $\overline{WP}$ pin goes high. While $\overline{WP}$ is low, the write protection blocks for the memory are determined by the status register bits BP0 and BP1 and cannot be modified without taking the $\overline{WP}$ signal high again.

If the $\overline{WP}$ signal is high (independent of the status of SRWD bit), the memory is in software protection mode. This means that block write protection is controlled solely by the status register BP0 and BP1 block write protect bits and this information can be modified using the WRSR command.

Table 8 – Block Memory Write Protection

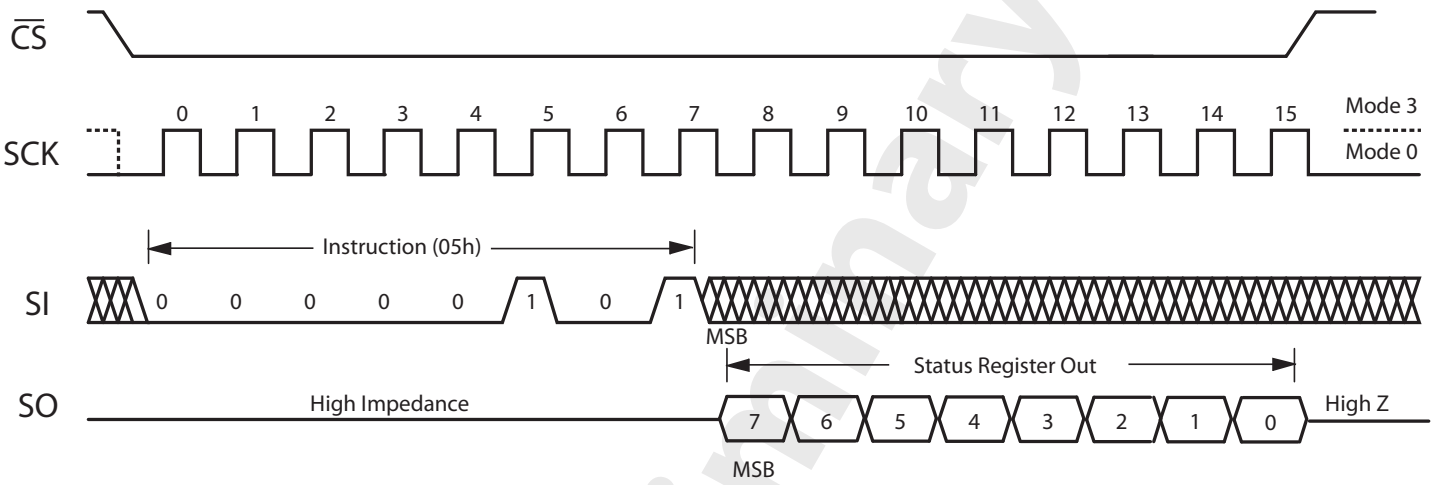
Status Register		Memory Contents	
BP1	BP0	Protected Area	Unprotected Area
0	0	None	All Memory
0	1	Upper Quarter	Lower Three-Quarters
1	0	Upper Half	Lower Half
1	1	All	None

SPI MODE COMMANDS

Read Status Register (RDSR)

The Read Status Register (RDSR) command allows the Status Register to be read. The Status Register can be read at any time to check the status of write enable latch bit, status register write protect bit, and block write protect bits. For MR10Q010, the write in progress bit (bit 0) is not written by the memory because there is no write delay. The RDSR command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

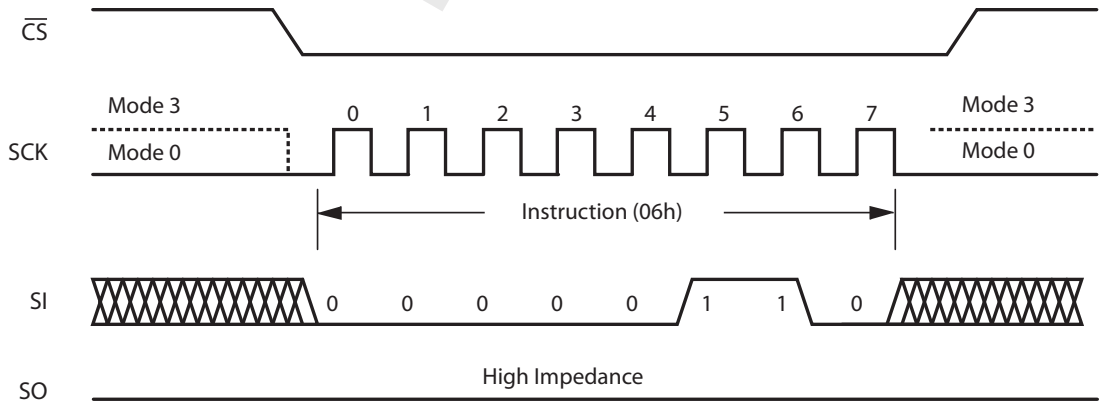
Figure 4 – Read Status Register Command (RDSR)



Write Enable (WREN)

The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit in the status register (bit 1). The Write Enable Latch must be set prior to writing in the status register or the memory. The WREN command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

Figure 5 – Write Enable Command (WREN)

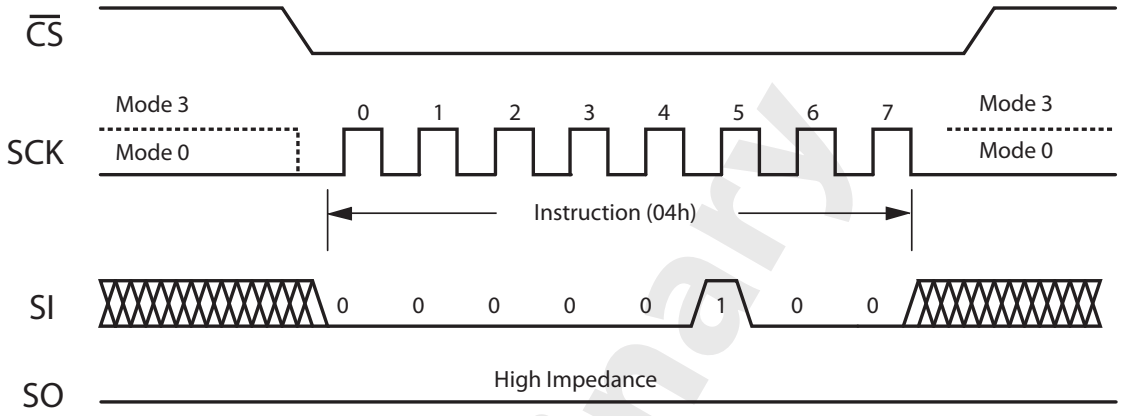


Write Disable (WRDI)

The Write Disable (WRDI) command resets the Write Enable Latch (WEL) bit in the status register (bit 1) to 0. This prevents writes to status register or memory. The WRDI command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

The Write Enable Latch (WEL) is reset to 0 on power-up or when the WRDI command is completed.

Figure 6 – Write Disable Command (WRDI)

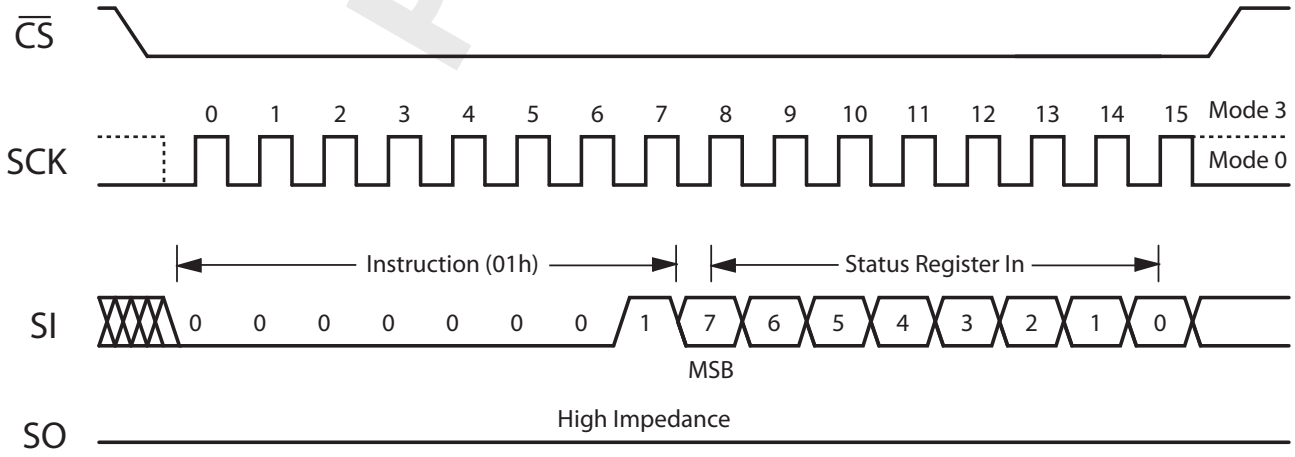


Write Status Register (WRSR)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. The WRSR command is not executed unless the Write Enable Latch (WEL) has been set to 1 by executing a WREN command while pin $\overline{WP}$ and bit SRWD correspond to values that make the status register writable as seen in Table 7 on page 15. Status Register bits are non-volatile with the exception of the WEL which is reset to 0 upon power cycling.

The WRSR command is entered by driving $\overline{CS}$ low, sending the command code and status register write data byte, and then driving $\overline{CS}$ high.

Figure 7 – Write Status Register Command (WRSR)

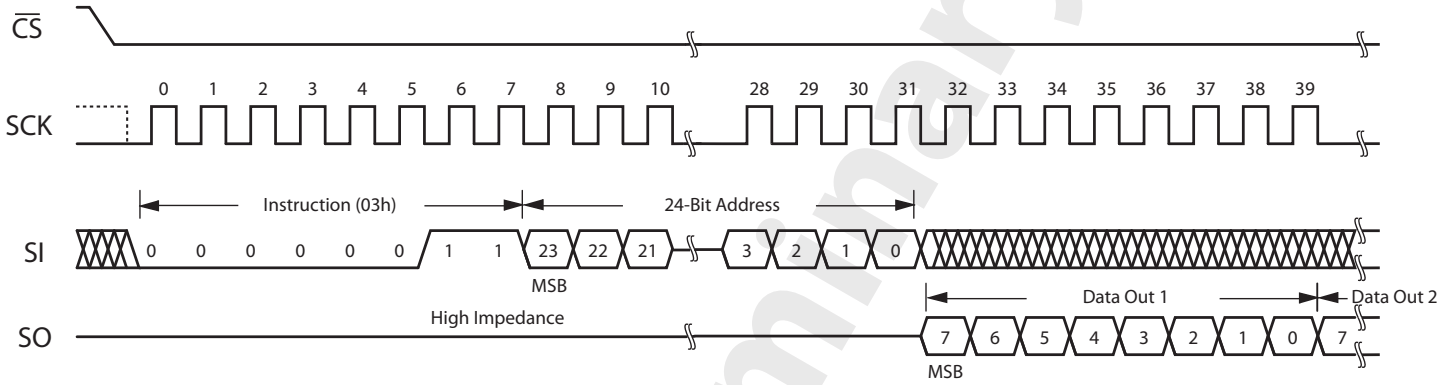


Read Data Bytes (READ)

The Read Data Bytes (READ) command allows data bytes to be read starting at an address specified by the 24-bit address. Only address bits 0-16 are decoded by the memory. The data bytes are read out sequentially from memory until the read operation is terminated by bringing $\overline{CS}$ high. The entire memory can be read in a single command. The address counter will roll over to 0000H when the address reaches the top of memory.

The READ command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the SO pin. Reads continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 8 – Read Data Bytes Command (READ)

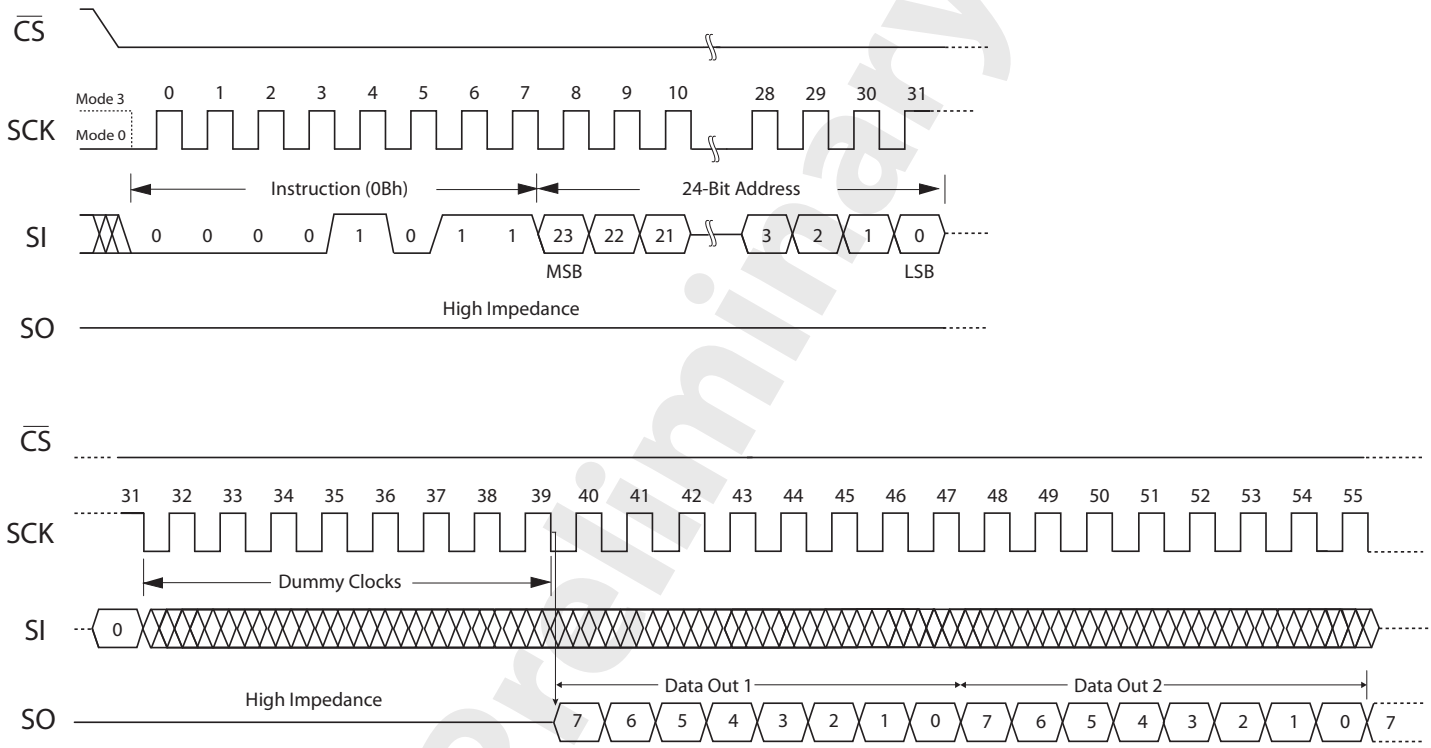


Fast Read Data Bytes (FREAD)

The Fast Read Data Bytes FREAD command is similar to the READ command except that it can operate at the highest frequency ^{f}SCK = 104MHz. This is accomplished by adding eight "Dummy" clocks after the 24 bit address. Only address bits 0-16 are decoded by the memory. The Dummy clocks provide the time required for the device to set up the initial address.

The FREAD command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the SO pin. Reads continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 9 – Fast Read Data Bytes Command (FREAD)



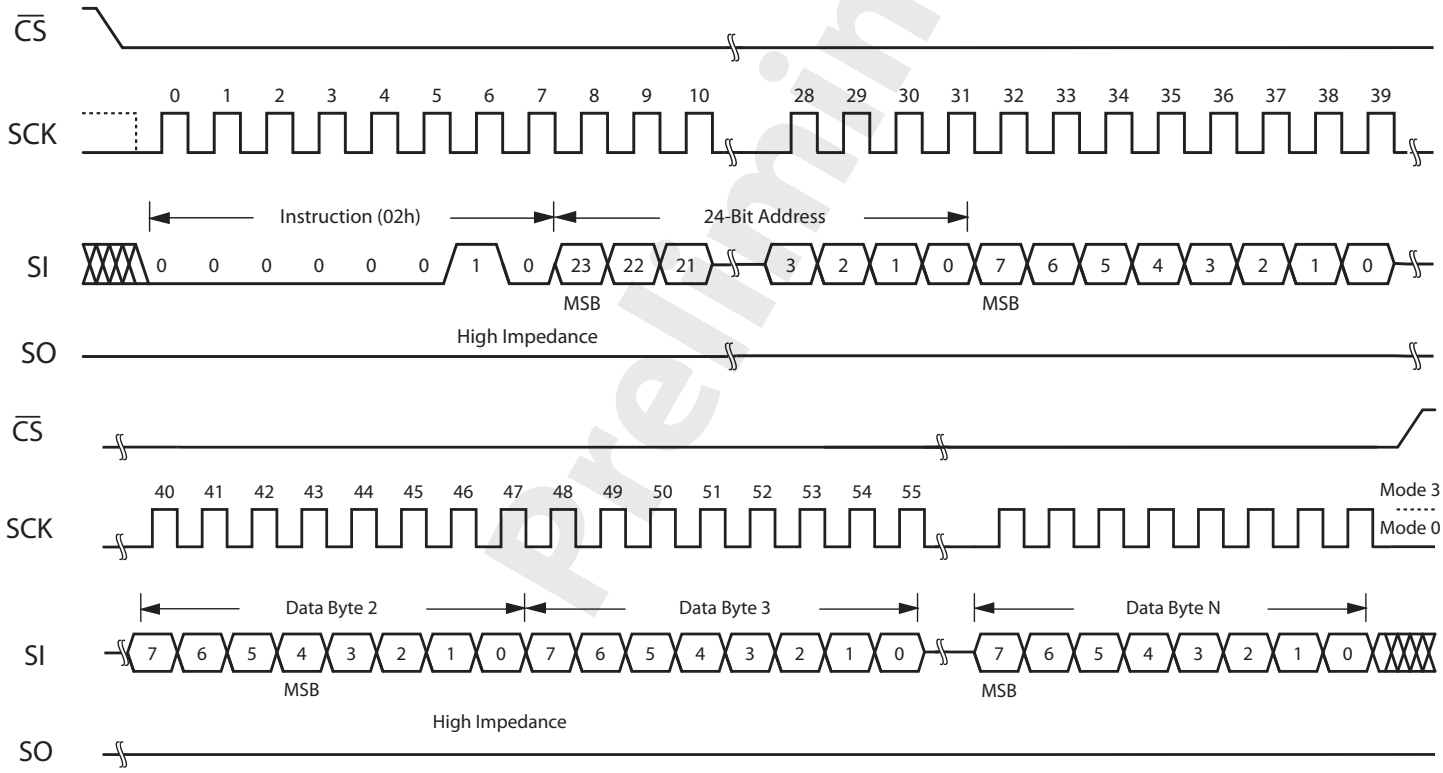
Write Data Bytes (WRITE)

The Write Data Bytes (WRITE) command allows data bytes to be written starting at an address specified by the 24-bit address. Only address bits 0-16 are decoded by the memory. The data bytes are written sequentially in memory until the write operation is terminated by bringing $\overline{CS}$ high. The entire memory can be written in a single command. The address counter will roll over to 0000h when the address reaches the top of memory.

Unlike EEPROM or Flash Memory, MRAM can write data bytes continuously at its maximum rated clock speed without write delays or data polling. Back to back WRITE commands to any random location in memory can be executed without write delay. MRAM is a random access memory rather than a page, sector, or block organized memory so it is ideal for both program and data storage.

The WRITE command is entered by driving $\overline{CS}$ low, sending the command code, and then sequential write data bytes. Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

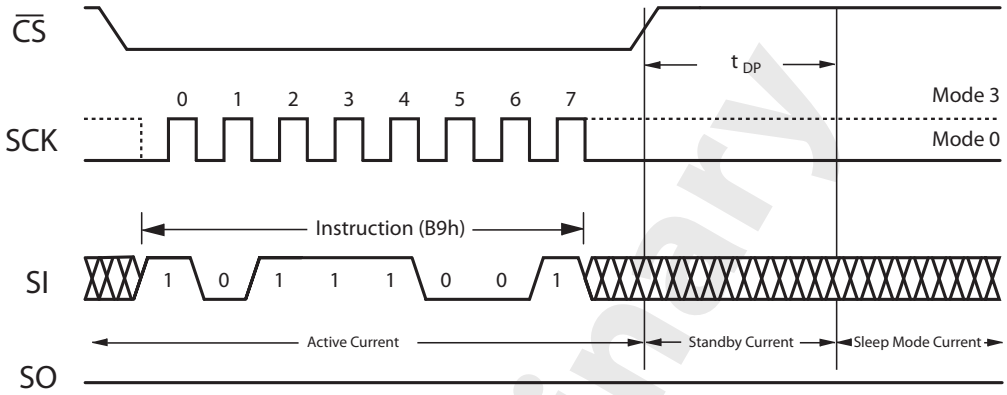
Figure 10 – Write Data Bytes Command (WRITE)



Enter Sleep Mode (SLEEP)

The Enter Sleep Mode (SLEEP) command turns off all MRAM power regulators in order to reduce the overall chip standby power to 15 µA typical. The SLEEP command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The standby current is achieved after time, ^{t}DP. If power is removed when the part is in sleep mode, upon power restoration, the part enters normal standby. The only valid command following SLEEP mode entry is a WAKE command.

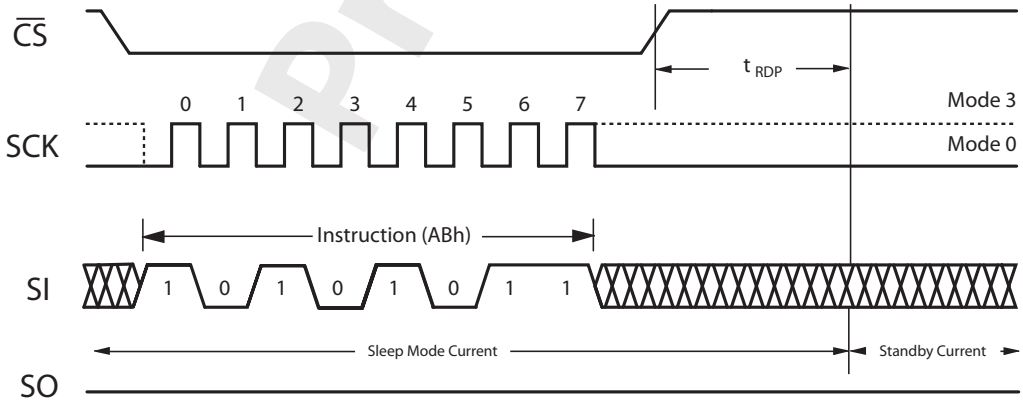
Figure 11 – Enter Sleep Mode Command (SLEEP)



Exit Sleep Mode (WAKE)

The Exit Sleep Mode (WAKE) command turns on internal MRAM power regulators to allow normal operation. The WAKE command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The memory returns to standby mode after ^{t}RDP. The $\overline{CS}$ pin must remain high until the ^{t}RDP period is over. WAKE must be executed after sleep mode entry and prior to any other command.

Figure 12 – Exit Sleep Mode Command (WAKE)



Tamper Detect (TDET)

Command Details are TBD

Read ID (RDID)

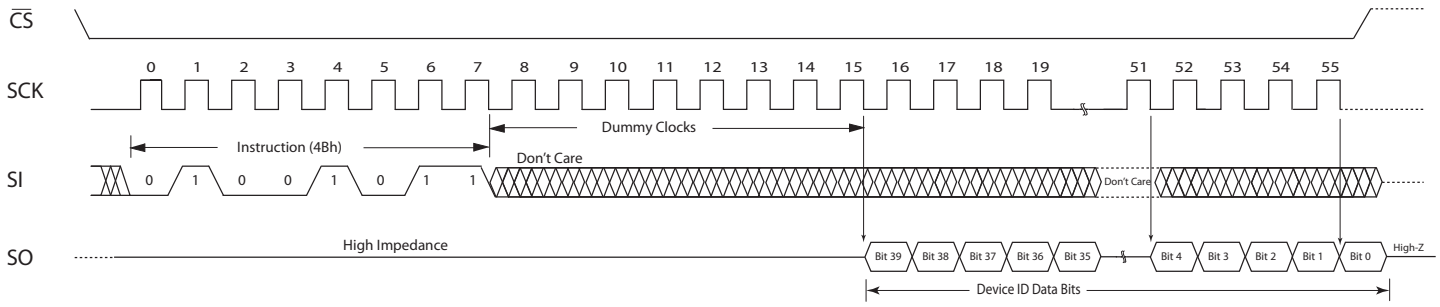
The Read Device ID command (RDID) returns 40 bits of information to identify the Everspin device. The command is invoked with $\overline{CS}$ low, sending command code 4Bh on the Serial Input (SI) pin. See "Figure 13 – Read ID (RDID) Command Timing" below. After 8 dummy clocks, 40 bits of data uniquely identifying the Everspin device are returned on the Serial Out (SO) pin. See "Table 9 – Device ID for MR10Q010". If $\overline{CS}$ remains low after reading the 40 ID bits, additional clocks with $\overline{CS}$ low will return zeros on SO until $\overline{CS}$ goes high.

Table 9 – Device ID for MR10Q010

RDID Device ID for MR10Q010							
Bit #	**39 - 24**	**23 - 20**	**19 - 16**	**15 - 12**	**11 - 8**	**7 - 4**	**3 - 0**
Meaning	**Manufacturer's ID (JEP 106AH)**	**Technology**	**Interface**	**Speed**	**Density**	**Voltage**	**Die Rev**
MR10Q10	6Bh, eighth bank	Toggle MRAM	Quad IO SPI	104MHz	1 Mb	3.3v V_{DD} / 1.8v V_{DDQ}	A
Binary	0000_0111_0110_1011	0001	0001	0001	0001	0001	0001

Complete Hexadecimal and Binary Device ID for MR10Q010	
Hexadecimal	076B111111
Binary	0000_0111_0110_1011_0001_0001_0001_0001_0001_0001

Figure 13 – Read ID (RDID) Command Timing



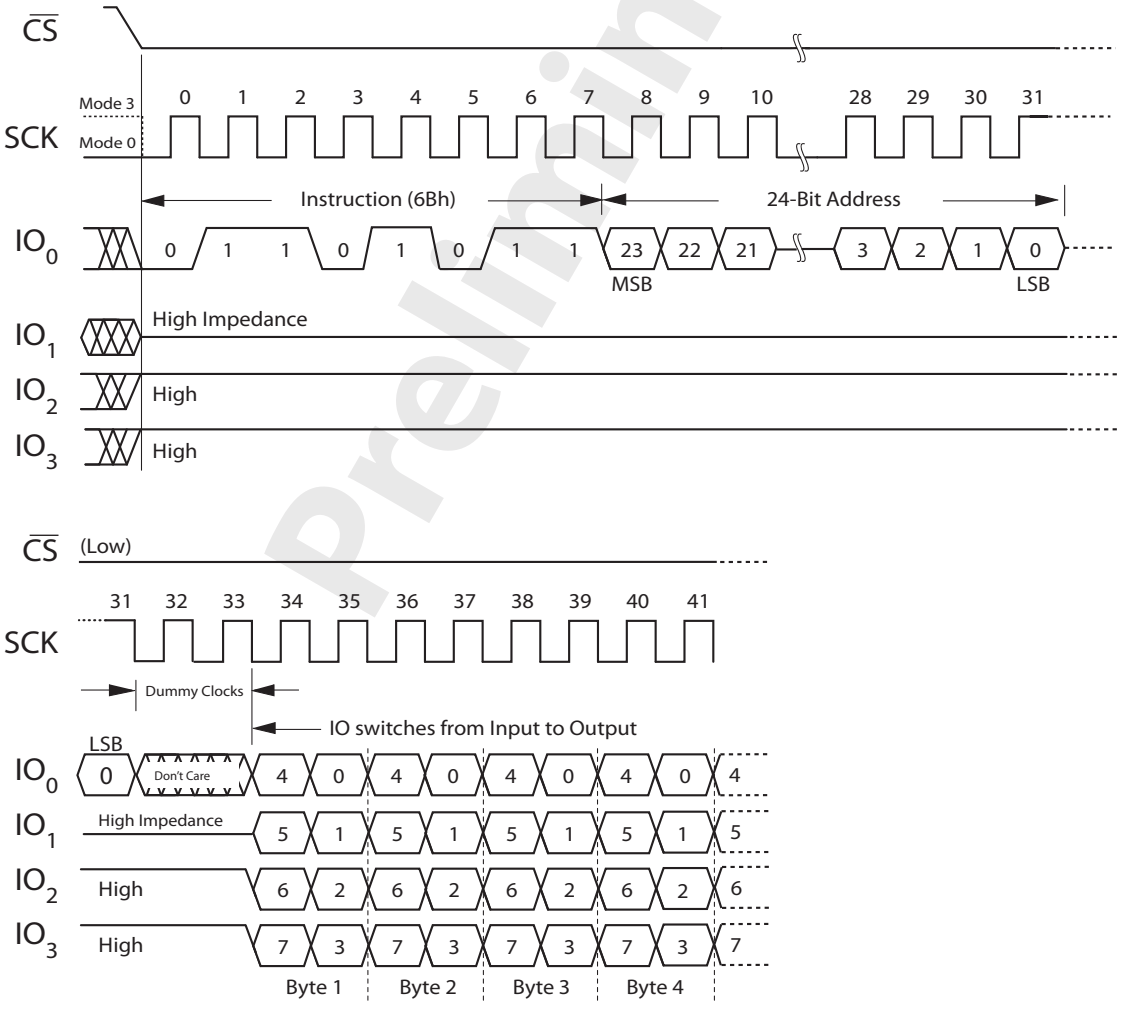
QUAD SPI MODE COMMANDS

Quad SPI commands allow data to be transferred to or from the device at least four times the rate of conventional SPI mode. When using Quad SPI commands the DI and DO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively. Address and data information can be input to the device on four IO's and data output can be read from four IO's, offering a significant improvement in continuous and random access transfers.

Fast Read Quad Output (FRQO)

The Fast Read Quad Ouptut (6Bh) command is similar to the Fast Read Output except that data is output on the four pins, I/O_{0-3}. The FRQO command can operate at the highest frequency by adding eight "Dummy" clocks after the 24-bit address. The Dummy clocks provide the time required for the device to set up the initial address. The input data during the Dummy clocks is "Don't Care," however the IO pins should be high impedance prior to the falling edge of the first data clock.

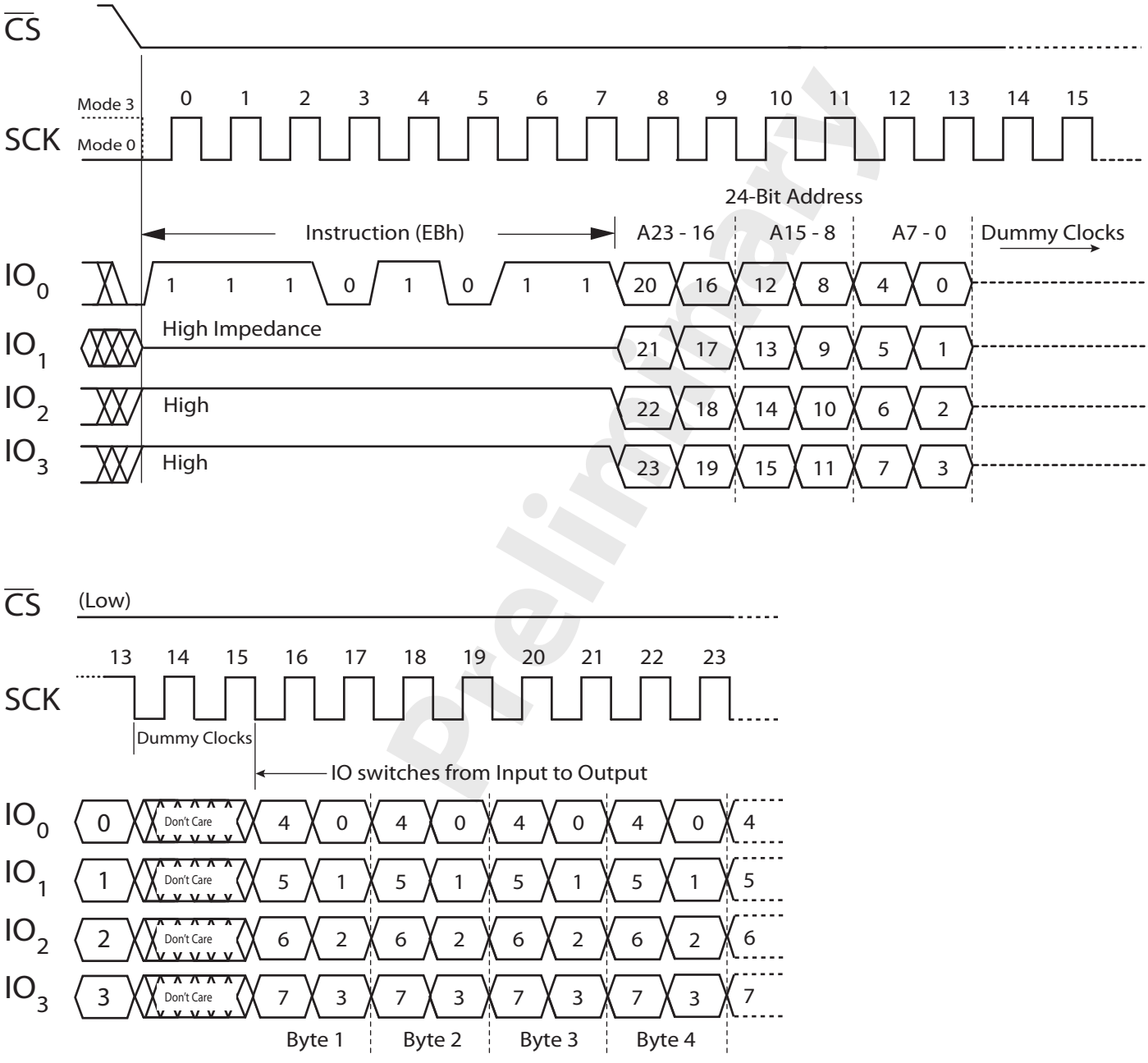
Figure 14 – Fast Read Quad Output Command (FRQO)



Fast Read Quad Address and Data (FRQAD)

The Fast Read Quad Address and Data (FRQAD) command is similar to the FRQO command except that the address bits are loaded into the four I/O's, providing a way to perform a Quad read in fewer clock cycles. The data bytes also are read from the four I/O's as shown in Figure 15 below.

Figure 15 – Fast Read Quad Address and Data Command (FRQAD)

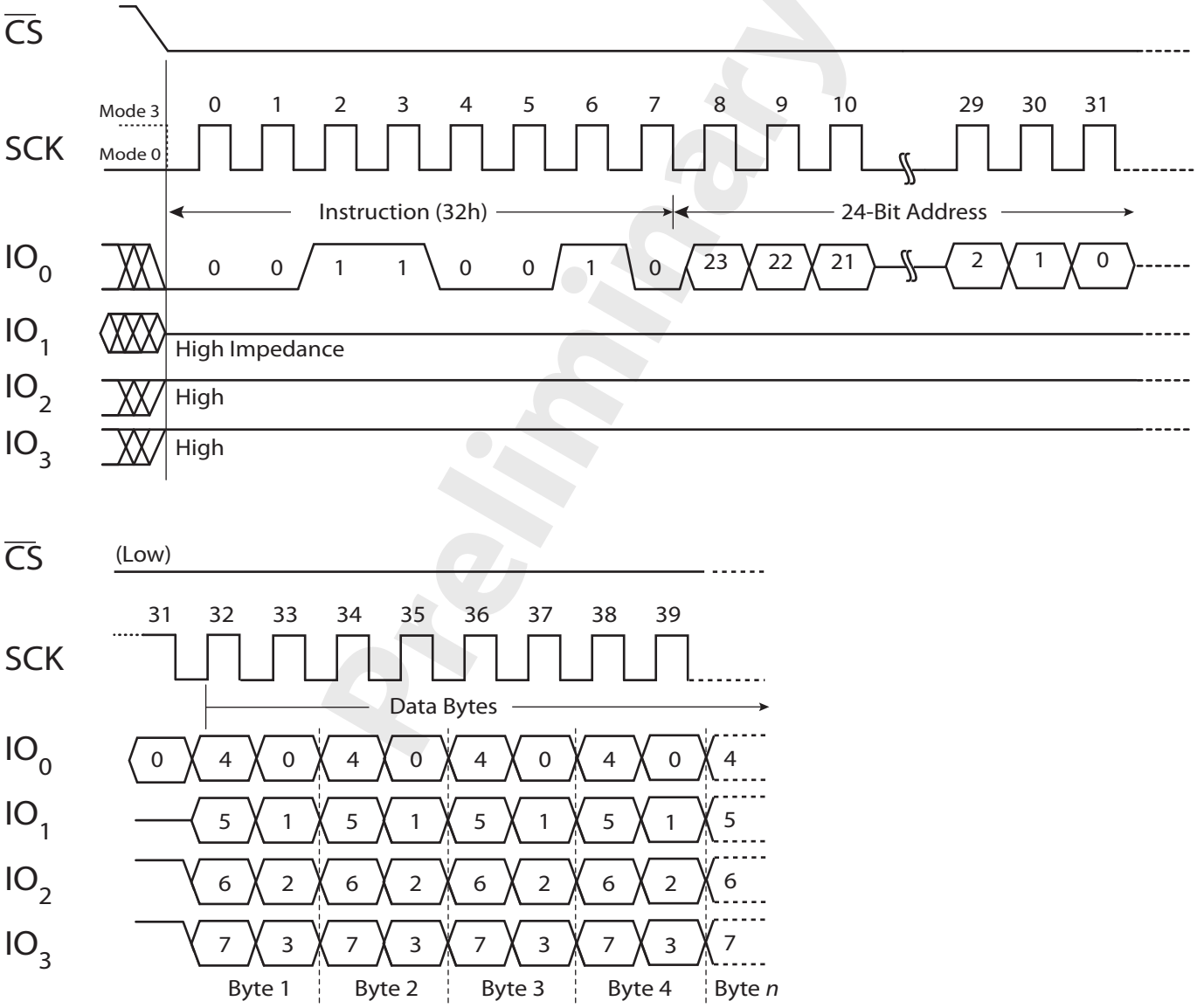


Fast Write Quad Data (FWQD)

The Fast Write Quad Data FWQD command provides a high speed write capability to the memory using four I/O's for data input. The FWQD command can operate at the highest frequency, $^{f}SCK = 104MHz$.

The FWQD command is entered by driving $\overline{CS}$ low and sending the command code (32h). Data is input on all four I/O's and Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 16 – Fast Write Quad Data Command (FWQD)

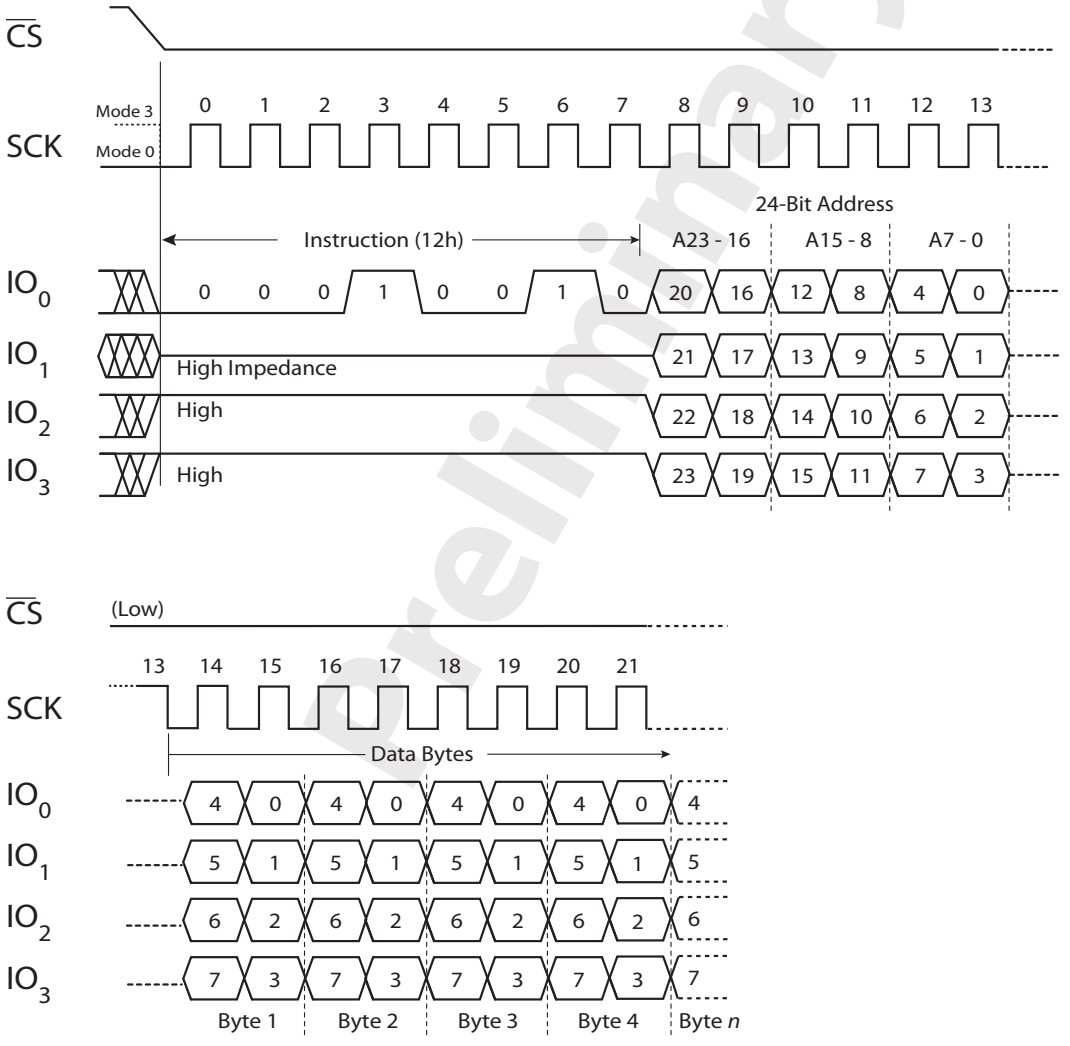


Fast Write Quad Address and Data (FWQAD)

The Fast Write Quad Address and Data Command (FWQAD) provides a very fast write at both the highest frequency and fewest clock cycles. The 24-bit address is input on all four I/O's, reducing the number of clock cycles. The data bytes to be written are also input on all four I/O's following the address bits. The FWQAD command can operate at the highest frequency, $^{f}SCK = 104MHz$.

The FWQAD command is entered by driving $\overline{CS}$ low and sending the command code (12h). Data are input on all four I/O's and Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 17 – Fast Write Quad Address and Data Command (FWQAD)



Notes:
The data bytes being written start on Clock 14 and continue until the end of the command.

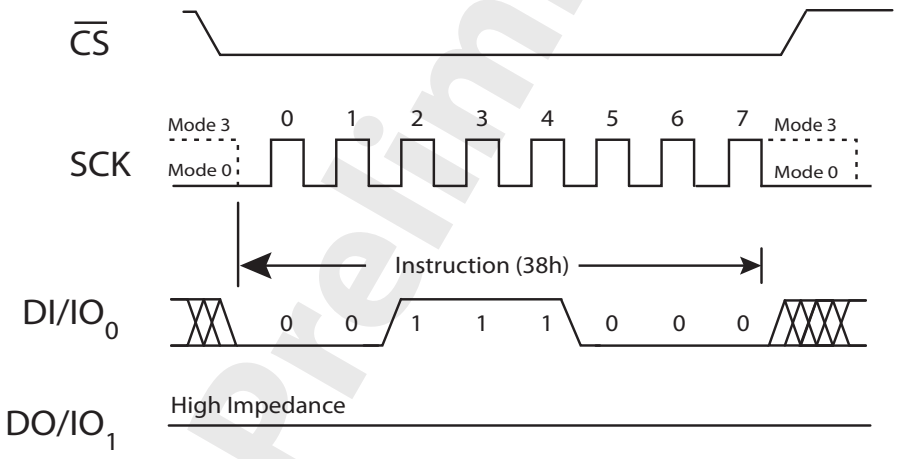
QPI MODE COMMANDS

The MR10Q010 supports Quad Peripheral Interface (QPI) operation when the device is switched from SPI/Quad SPI mode to QPI mode. This is done by applying the "Enable QPI" command. The QPI mode utilizes all four I/O's to input the instruction code, which reduces the clock cycles required for command entry to two cycles. This reduces SPI instruction overhead and improves system performance in an XIP environment. Standard SPI/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. The Enable QPI and Disable QPI instructions are used to switch between these two modes. At power up the default state is Standard SPI/Quad SPI mode. When using QPI instructions, the DI and DO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become bidirectional IO_2 and IO_3 respectively.

Enable QPI (EQPI)

The Enable QPI command is used to enter the device into QPI mode. The command code, 38h, is entered on the DI pin. The command is entered by driving $\overline{CS}$ low and sending the command code. The command is terminated by driving $\overline{CS}$ high. The device stays in QPI mode until a power-on reset or the Disable QPI command is entered.

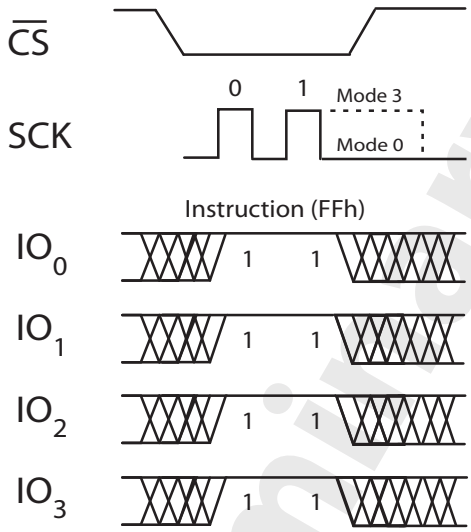
Figure 18 – Enable QPI Command (EQPI)



Disable QPI (DQPI)

The Disable QPI command is used to exit QPI mode and return to the standard SPI/Quad SPI mode. The command code FFh is entered on all four IO's in just two clock cycles as shown below. The command is entered by driving $\overline{CS}$ low and sending the command code. The command is terminated by driving $\overline{CS}$ high.

Figure 19 – Disable QPI Command (DQPI)



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 10 – Absolute Maximum Ratings

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

Symbol	Parameter	Conditions	Value	Unit
V_{DD}	Supply voltage [2]		-0.5 to 4.0	V
V_{DDQ}	I/O Bus Supply voltage [2]		-0.5 to 2.4	V
V_{IN}	Voltage on any pin [2]		-0.5 to V_{DD} + 0.5	V
I_{OUT}	Output current per pin		±20	mA
P_D	Package power dissipation [3]		0.600	W
T_{BIAS}	Temperature under bias	Commercial Grade	-45 to 95	°C
T_{stg}	Storage Temperature		-55 to 150	°C
T_{Lead}	Lead temperature during solder (3 minute max)		260	°C
H_{max_write}	Maximum magnetic field during write	Write	12,000	A/m
H_{max_read}	Maximum magnetic field during read or standby	Read or Standby	12,000	A/m

Notes:

1. All voltages are referenced to V_{SS}. The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.
2. Power dissipation capability depends on package characteristics and use environment.

Table 11 – Operating Conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{DD}	Power supply voltage		3.0	3.3	3.6	V
V_{DDQ}	I/O Bus Power supply voltage		1.7	1.8	2.0	V
V_{IH}	Input high voltage		1.4		V_{DDQ} + 0.2	V
V_{IL}	Input low voltage		-0.2		0.4	V
T_A	Ambient temperature under bias	Commercial Grade	0		70	°C
		Industrial Grade	-40		85	°C

Table 12 – DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
I_{IL}	Input leakage current		-	±2	µA
I_{OL}	Output leakage current		-	±2	µA
V_{OL}	Output low voltage	I_{OL} = 4mA	-	0.4	V
V_{OH}	Output high voltage	I_{OH} = -100µA	1.4	-	V

Table 13 – Power Supply Characteristics

Symbol	Parameter	Conditions	Typical	Max	Unit
I_{DDR}	Active Read Current	SPI @ 1 MHz	5.0	11	mA
		SPI @ 40 MHz	12	17	mA
		Quad SPI @ 104MHz	-	80	mA
I_{DDW}	Active Write Current	@ 1 MHz	9.0	25	mA
		@ 40 MHz	28	42	mA
		Quad SPI @ 104MHz	-	220	mA
I_{DDQ}	Active V_{DDQ} Current	TBD	-	TBD	mA
I_{SB1}	AC Standby Current ($\overline{CS}$ High = V_{IH}. No other restrictions on other inputs.)	f ≤104MHz	-	5	mA
I_{SB2}	CMOS Standby Current ($\overline{CS}$ High)	f = 0 MHz	-	TBD	mA
I_{ZZ}	Standby Sleep Mode Current ($\overline{CS}$ High)	Sleep Mode	-	100	µA

Capacitance

Table 14 – Capacitance

Symbol	Parameter	Typical	Max	Unit
C_{In}	Control input capacitance [1]	-	6	pF
$C_{I/O}$	Input/Output capacitance [1]	-	8	pF

Notes:

1. f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

TIMING SPECIFICATIONS

AC Measurement Conditions

Table 15 – AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	0.9	V
Logic output timing measurement reference level	0.9	V
Logic input pulse levels	0 to 1.6	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 20	
Output load for all other timing parameters	See Figure 21	

Figure 20 – Output Load for Impedance Parameter Measurements

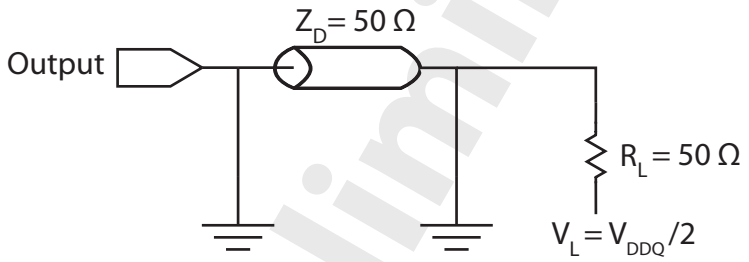
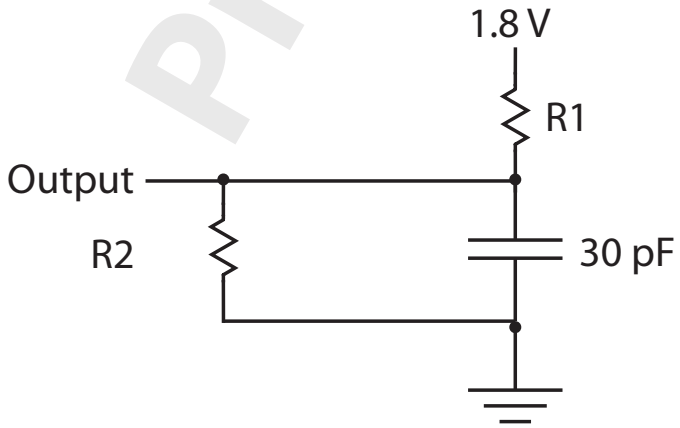


Figure 21 – Output Load for all Other Parameter Measurements



Power Up Timing

To provide protection for data during initial power up, power loss or brownout, whenever V_{DD} falls below V_{WIDD} or V_{DDQ} falls below V_{WIDDQ} the device cannot be selected ($\overline{CS}$ is restricted from going low) and the device is inhibited from Read or Write operations. See "Table 16 – Power-Up Delay Minimum Voltages and Timing" below.

Power Up Delay Time

During initial power up or when recovering from brownout or power loss, a power up delay time (^{t}PU) must be added to the time required for voltages to rise to their specified minimum voltages ($V_{DD(min)}$ and $V_{DDQ(min)}$) before normal operations may commence. This time is required to insure that the device internal voltages have stabilized. See "Table 16 – Power-Up Delay Minimum Voltages and Timing" below.

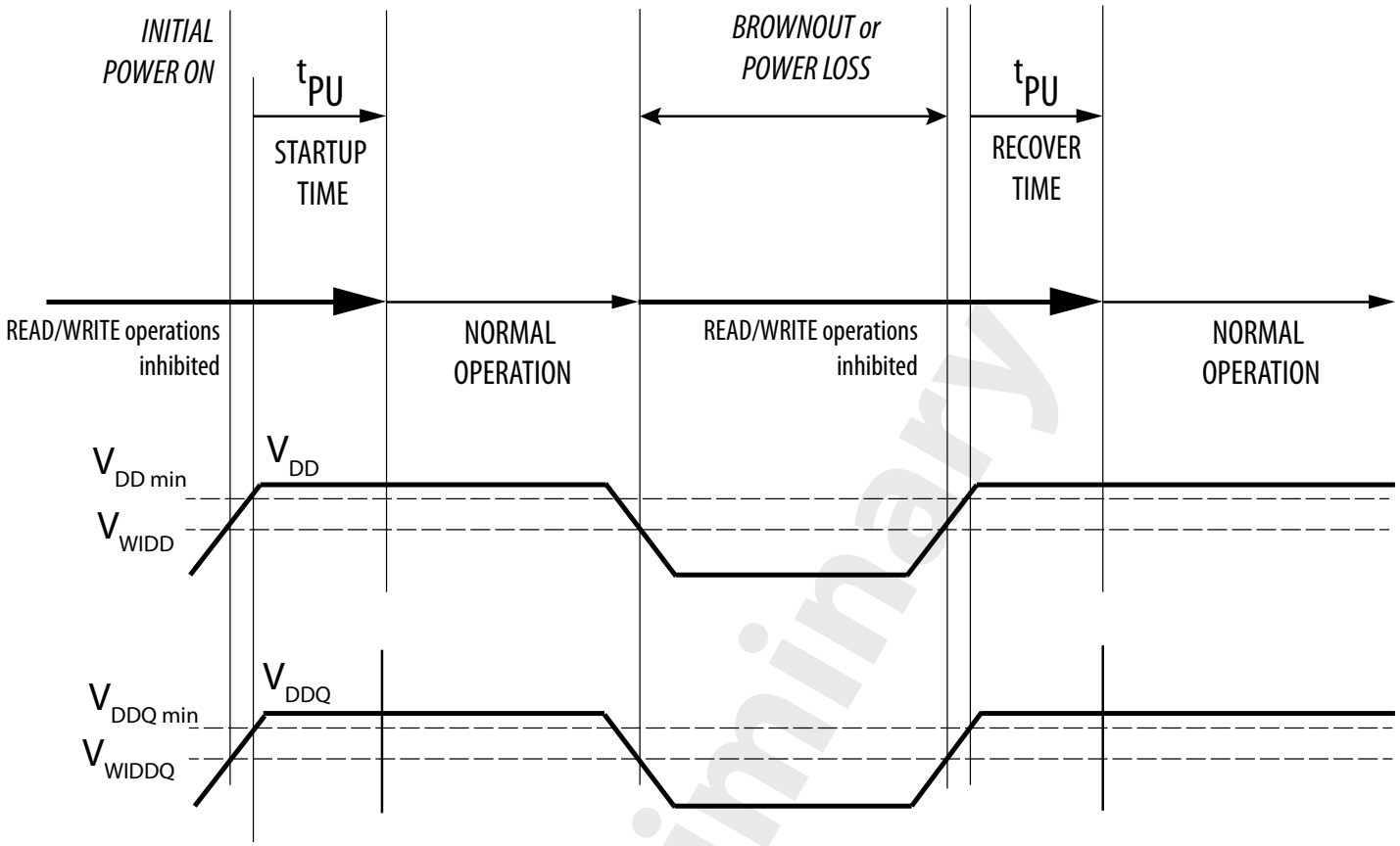
^{t}PU is measured from the time that both V_{DD} and V_{DDQ} have reached their specified minimum voltages. See "Figure 22 – Power-Up Timing" for an illustration of the timing.

During initial startup or power loss recovery the $\overline{CS}$ pin should always track V_{DDQ} (up to V_{DDQ} + 0.2 V) or V_{IH}, whichever is lower, and remain high for the total startup time, ^{t}PU. In most systems, this means that $\overline{CS}$ should be pulled up to V_{DDQ} with a resistor. Any logic that drives other inputs or IOs should hold the signals at V_{DDQ} until normal operation can commence.

Table 16 – Power-Up Delay Minimum Voltages and Timing

Symbol	Parameter	Min	Typical	Max	Unit
V_{WIDD}	Write Inhibit Voltage	2.2	-	TBD	V
V_{WIDDQ}	I/O Write Inhibit Voltage	1.2	1.4	1.6	V
^{t}PU	Power Up Delay Time	400	-	-	µs

Figure 22 – Power-Up Timing



Note: $\overline{CS}$ may not be enabled until ^{t}PU startup or recovery time is met.

AC Timing Parameters

Table 17 – AC Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
^{f}SCK	SCK Clock Frequency for all instructions except READ	-	-	104	MHz
	SCK Clock freq for READ	-	-	40	MHz
^{t}RI	Input Rise Time	-	-	50	ns
^{t}RF	Input Fall Time	-	-	50	ns
^{t}WH	SCK High Time except READ	4	-	-	ns
^{t}WHR	SCK High Time READ	11	-	-	ns
^{t}WL	SCK Low Time except READ	4	-	-	ns
^{t}WLR	SCK Low Time READ	11	-	-	ns
Synchronous Data Timing see Figure 23					
^{t}CS	CS High Time	40	-	-	ns
^{t}CSS	CS Setup Time	5	-	-	ns
^{t}CSH	CS Hold Time	5	-	-	ns
^{t}SU	Data In Setup Time	2	-	-	ns
^{t}H	Data In Hold Time	5	-	-	ns
^{t}V	Output Valid	0	-	7	ns
^{t}HO	Output Hold Time	0	-	-	ns
^{t}CSW	$\overline{CS}$ High Time at end of Write Cycles	50	-	-	ns
^{t}CSR	$\overline{CS}$ High Time at end of Read Cycles	10	-	-	ns

AC Timing Parameters - Continued

Symbol	Parameter	Min	Typical	Max	Unit
$\overline{HOLD}$ Timing see "$\overline{HOLD}$ Timing" on page 39					
^tHD	$\overline{HOLD}$ Setup Time	2	-	-	ns
^tCD	$\overline{HOLD}$ Hold Time	2	-	-	ns
^tLZ	$\overline{HOLD}$ to Output Low Impedance	-	-	12	ns
^tHZ	$\overline{HOLD}$ to Output High Impedance	-	-	7	ns
Other Timing Specifications					
^tWPS	WP Setup To CS Low	5	-	-	ns
^tWPH	WP Hold From CS High	5	-	-	ns
^tDP	Sleep Mode Entry Time	-	-	3	µs
^tRDP	Sleep Mode Exit Time	-	-	400	µs
^tDIS	Output Disable Time	-	-	7	ns

Figure 23 – Synchronous Data Timing (READ)

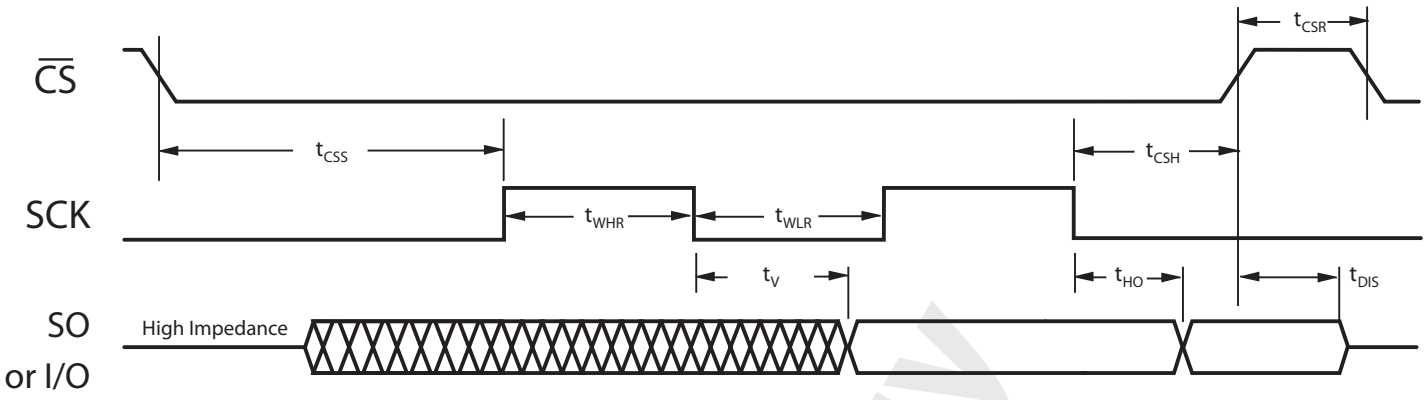


Figure 24 – Synchronous Data Timing Fast Read (FREAD)

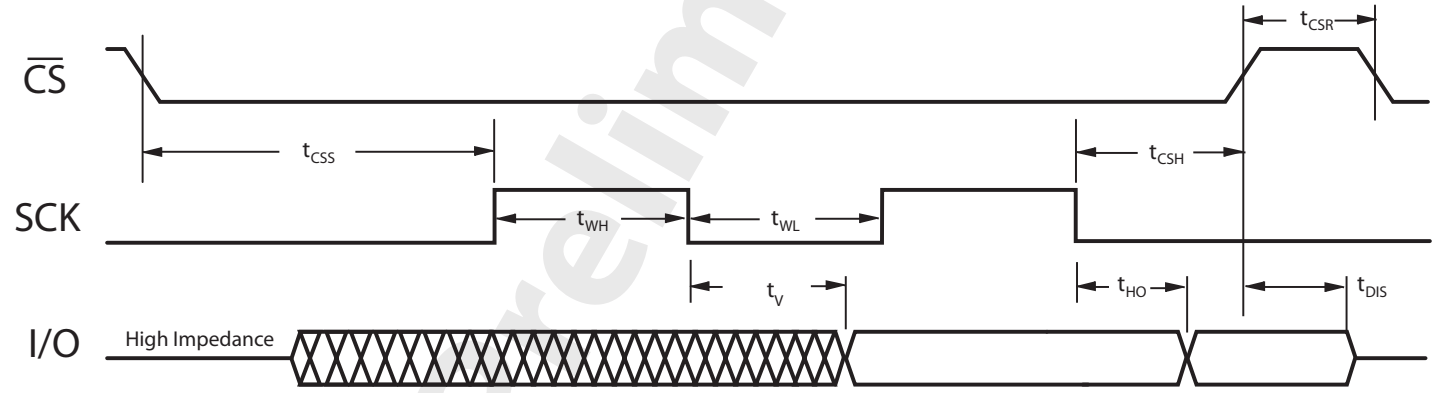


Figure 25 – Synchronous Data Timing (WRITE)

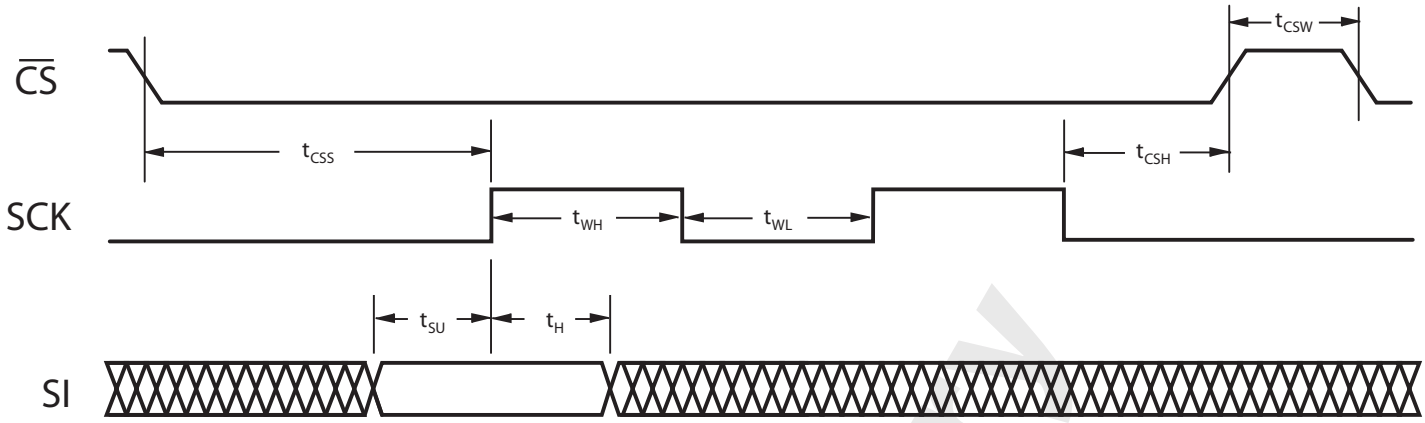


Figure 26 – Synchronous Data Timing Fast Write Quad Data and Fast Write Quad Address and Data (FWQD and FWQAD)

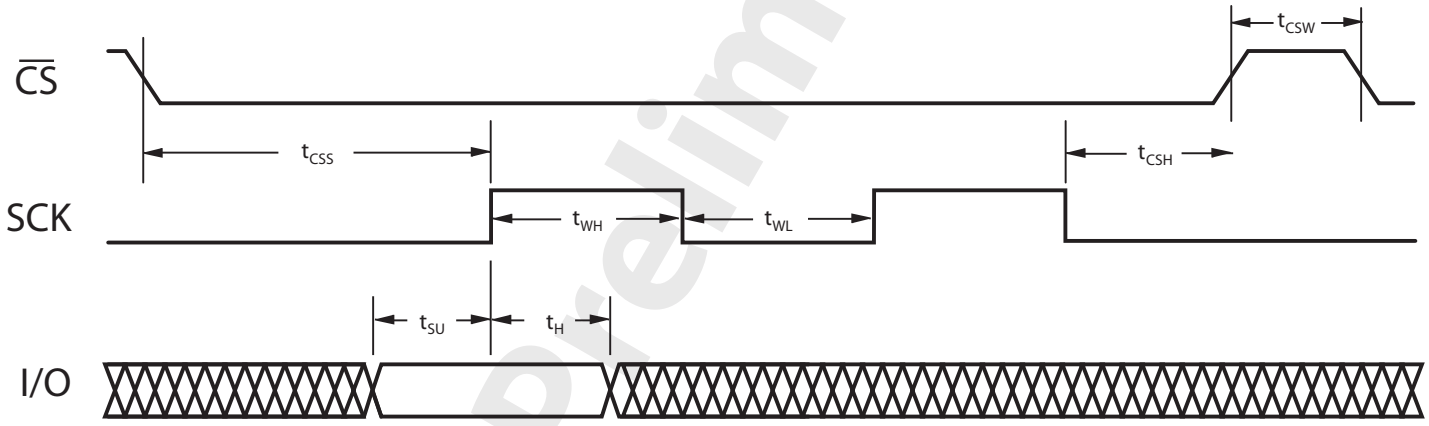
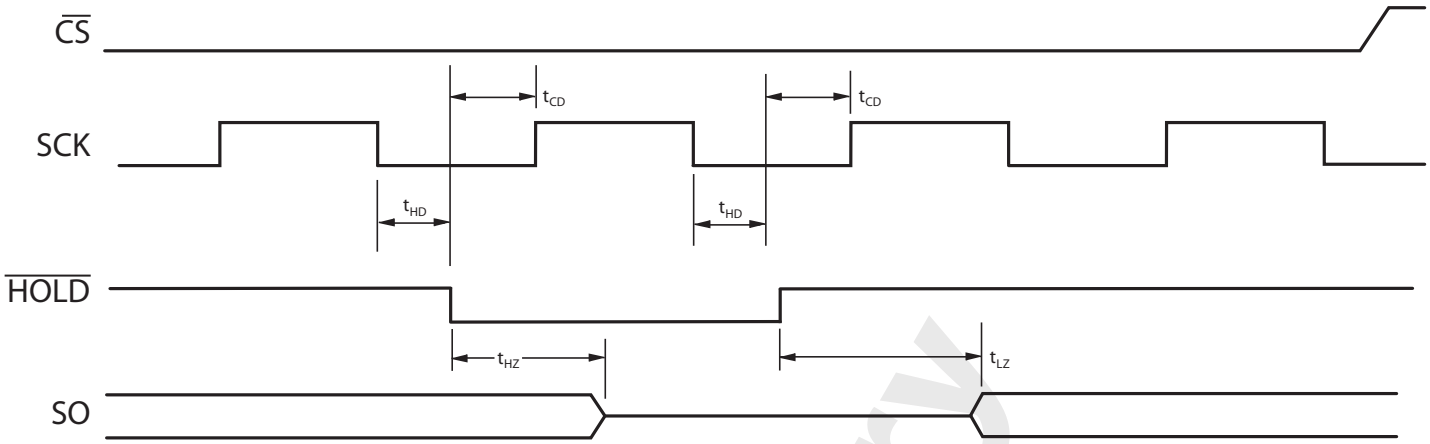


Figure 27 – $\overline{\text{HOLD}}$ Timing



PART NUMBERS AND ORDERING

Table 18 – Part Numbering System

Product Family Number		MR	10Q	xxx				
		Memory	**Interface**	**Density**	**Revision**	**Temp**	**Package**	**Grade**
Example Ordering Part Number		MR	10Q	010			SC	ES
MRAM (Toggle)		MR						
104MHz Quad SPI Family		10Q						
1 Mb		010						
4 Mb		040						
16Mb		160						
No Revision		Blank						
Revision A		A						
Revision B		B						
Commercial	0 to 70°C	Blank						
Industrial	-40 to 85°C	C						
16-pin SOIC		SC						
Engineering Samples		ES						
Customer Samples		CS						
Mass Production		Blank						

Product Family Number and Ordering Part Number given are for illustration only.

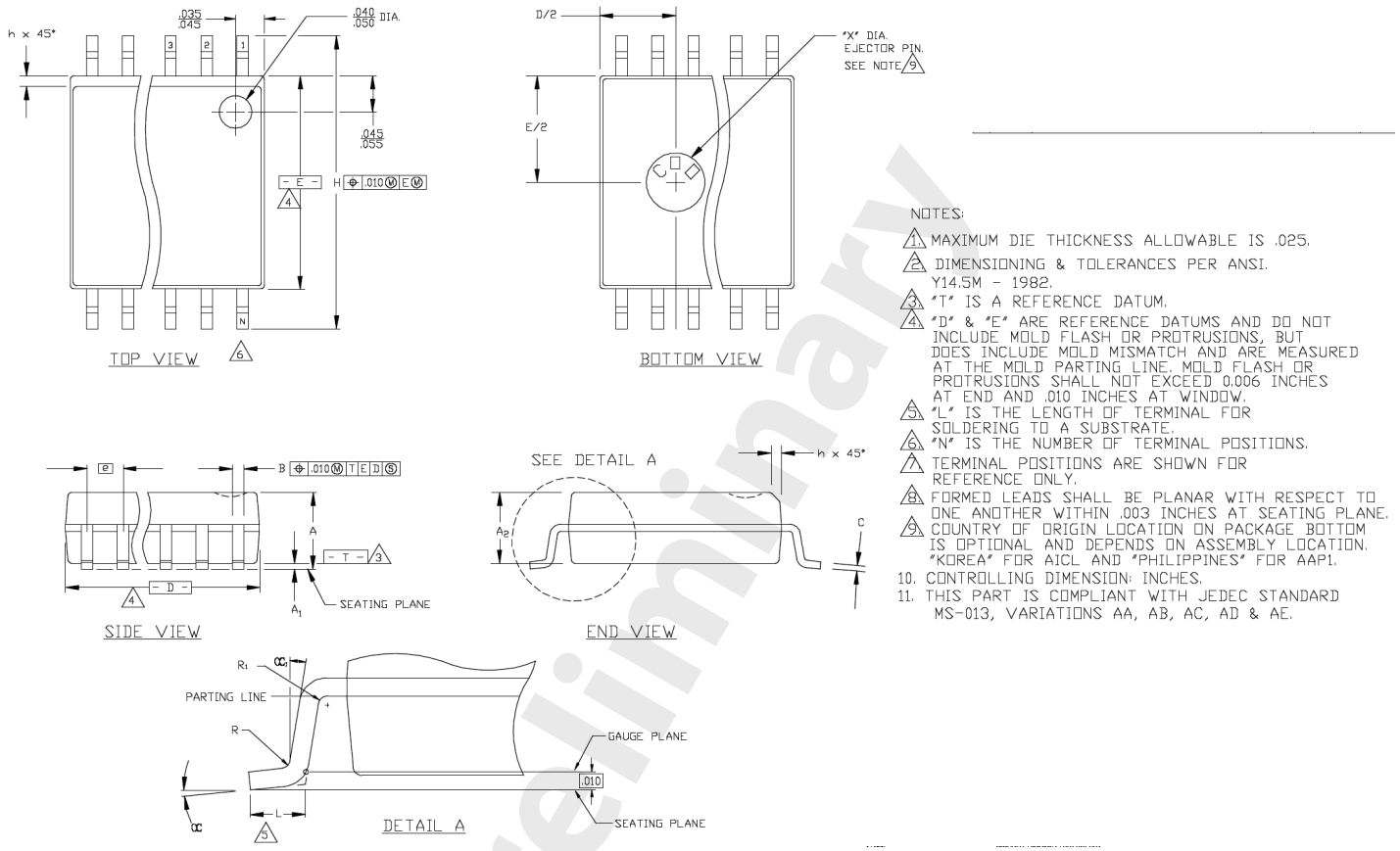
Table 19 – Ordering Part Numbers

Temp Grade	Temperature	Package	Density	Shipping Container	Order Part Number
Commercial	0 to 70°C	16-SOIC	1Mb	Trays	MR10Q010SC
				Tape and Reel	MR10Q010SCR
Industrial	-40 to 85°C	16-SOIC	1Mb	Trays	MR10Q010CSC
				Tape and Reel	MR10Q010CSCR

Preliminary Products: These products are classified as Preliminary until the completion of all qualification tests. The specifications in this data sheet are intended to be final but are subject to change. Please check the Everspin web site www.everspin.com for the latest information on product status.

PACKAGE OUTLINE DRAWINGS

Figure 28 – 16-SOIC Package Outline



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M – 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES AT END AND .010 INCHES AT WINDOW.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION. "KOREA" FOR AICL AND "PHILIPPINES" FOR AAP1.
10. CONTROLLING DIMENSION: INCHES.
11. THIS PART IS COMPLIANT WITH JEDEC STANDARD MS-013, VARIATIONS AA, AB, AC, AD & AE.

16-SOIC Package Outline - Continued

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
α_1	0°	–	–						
R	.0028	–	–						
R_1	.0028	–	–						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
α_1	0°	–	–						
R	0.07	–	–						
R	0.07	–	–						
X	2.16	2.36	2.54						

REVISION HISTORY

Revision	Date	Description of Change
1.7	February 26, 2013	Initial Release Preliminary.
1.8	3/7/2013	Revision to Table 5. Revision to $\overline{\text{HOLD}}$ timing Table 15. Corrected package illustration.
1.9	5/14/2013	Added QPI Commands.

HOW TO REACH US

Everspin Technologies, Inc.

Home Page:

www.everspin.com

E-Mail:

support@everspin.com
orders@everspin.com
sales@everspin.com

USA/Canada/South and Central America

World Headquarters
1347 N. Alma School Road, Suite 220
Chandler, Arizona 85224
1-877-347-MRAM (6726)
1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

support.asia@everspin.com

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