

## FEATURES

256K x 16 MRAM Memory

- Fast 35 ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Non-volatile for >20 years at Temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in System for Simpler, More Efficient Design
- Replace battery-backed SRAM solutions with MRAM to improve reliability
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Commercial, Industrial, Extended Temperatures
- RoHS-Compliant SRAM TSOP2 and BGA Packages - MSL Level 3
- AEC-Q100 Grade 1 option



## INTRODUCTION

The **MR2A16A** is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 262,144 words of 16 bits. The **MR2A16A** offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The **MR2A16A** is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **M24A16B** is available in a small footprint 48-pin ball grid array (BGA) package and a 44-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR2A16A** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial (0 to +70 °C), industrial (-40 to +85 °C), extended (-40 to +105 °C) and AEC-Q100 Grade 1 (-40 to +125 °C) operating temperature range options.

## CONTENTS

1. DEVICE PIN ASSIGNMENT.....	2
2. ELECTRICAL SPECIFICATIONS.....	4
3. TIMING SPECIFICATIONS.....	7
4. ORDERING INFORMATION.....	12
5. MECHANICAL DRAWING.....	13
6. REVISION HISTORY.....	15
How to Reach Us.....	15

## 1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram

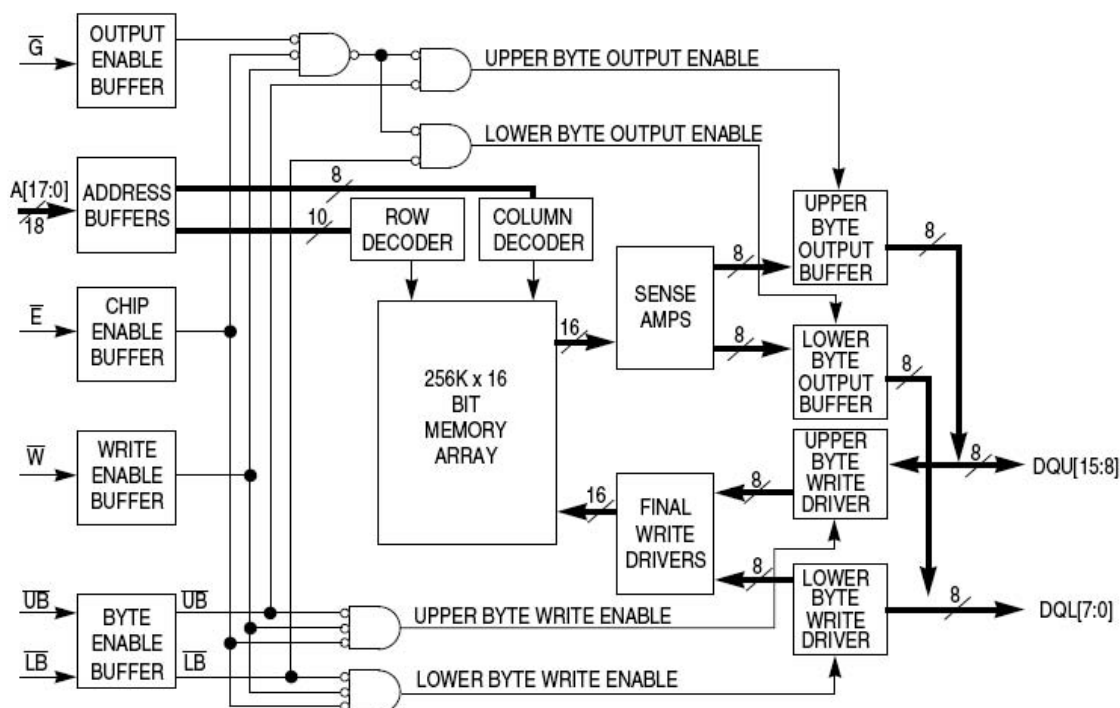
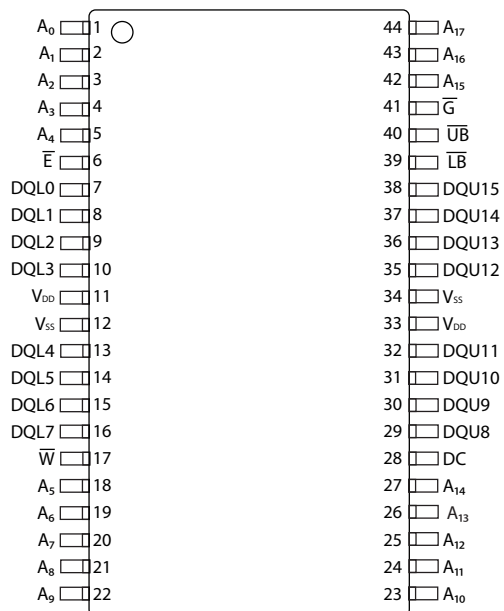


Figure 1. Block Diagram

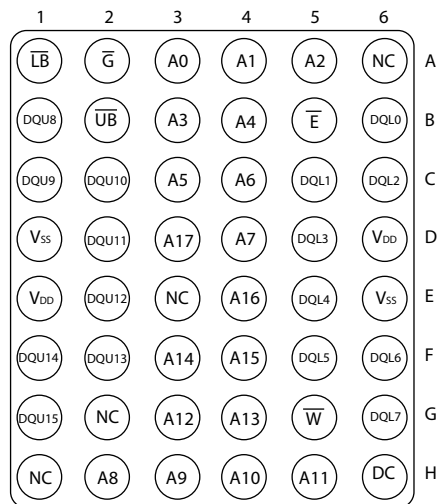
Table 1.1 Pin Functions

Signal Name	Function
A	Address Input
$\bar{E}$	Chip Enable
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
$\bar{UB}$	Upper Byte Enable
$\bar{LB}$	Lower Byte Enable
DQ	Data I/O
$V_{DD}$	Power Supply
$V_{SS}$	Ground
DC	Do Not Connect
NC	No Connection

Figure 1.2 Pin Diagrams for Available Packages (Top View)



44-Pin TSOP Type2



48-Pin BGA

Table 1.2 Operating Modes

$\overline{E}^1$	$\overline{G}^1$	$\overline{W}^1$	$\overline{LB}^1$	$\overline{UB}^1$	Mode	$V_{DD}$ Current	DQL[7:0] <sup>2</sup>	DQU[15:8] <sup>2</sup>
H	X	X	X	X	Not selected	$I_{SB1}, I_{SB2}$	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	$I_{DDR}$	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	$I_{DDR}$	Hi-Z	Hi-Z
L	L	H	L	H	Lower Byte Read	$I_{DDR}$	$D_{Out}$	Hi-Z
L	L	H	H	L	Upper Byte Read	$I_{DDR}$	Hi-Z	$D_{Out}$
L	L	H	L	L	Word Read	$I_{DDR}$	$D_{Out}$	$D_{Out}$
L	X	L	L	H	Lower Byte Write	$I_{DDW}$	$D_{in}$	Hi-Z
L	X	L	H	L	Upper Byte Write	$I_{DDW}$	Hi-Z	$D_{in}$
L	X	L	L	L	Word Write	$I_{DDW}$	$D_{in}$	$D_{in}$

<sup>1</sup> H = high, L = low, X = don't care

<sup>2</sup> Hi-Z = high impedance

## 2. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

**Table 2.1 Absolute Maximum Ratings<sup>1</sup>**

Symbol	Parameter	Temp Range	Package	Value	Unit
$V_{DD}$	Supply voltage <sup>2</sup>	-	-	-0.5 to 4.0	V
$V_{IN}$	Voltage on any pin <sup>2</sup>	-	-	-0.5 to $V_{DD} + 0.5$	V
$I_{OUT}$	Output current per pin	-	-	±20	mA
$P_D$	Package power dissipation <sup>3</sup>	-	Note 3	0.600	W
$T_{BIAS}$	Temperature under bias	Commercial	-	-10 to 85	°C
		Industrial	-	-45 to 95	
		Extended	-	-45 to 110	
		AEC-Q100 Grade 1	-	-45 to 130	
$T_{stg}$	Storage Temperature	-	-	-55 to 150	°C
$T_{Lead}$	Lead temperature during solder (3 minute max)	-	-	260	°C
$H_{max\_write}$	Maximum magnetic field during write	Commercial	TSOP2, BGA	2,000	A/m
		Industrial, Extended	BGA	2,000	
			TSOP2	10,000	
		AEC-Q100 Grade 1	TSOP2	2,000	
$H_{max\_read}$	Maximum magnetic field during read or standby	Commercial	TSOP2, BGA	8,000	A/m
		Industrial, Extended	BGA	8,000	
			TSOP2	10,000	
		AEC-Q100 Grade 1	TSOP2	8,000	

#### Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to  $V_{SS}$ .
3. Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage <sup>1</sup>	$V_{DD}$	3.0	3.3	3.6	V
Write inhibit voltage	$V_{WI}$	2.5	2.7	3.0 <sup>1</sup>	V
Input high voltage	$V_{IH}$	2.2	-	$V_{DD} + 0.3$ <sup>2</sup>	V
Input low voltage	$V_{IL}$	-0.5 <sup>3</sup>	-	0.8	V
Temperature under bias MR2A16A (Commercial) MR2A16AC (Industrial) MR2A16AV (Extended) MR2A16AM (AEC-Q100 Grade 1) <sup>4</sup>	$T_A$	0 -40 -40 -40		70 85 105 125	°C

<sup>1</sup> There is a 2 ms startup time once  $V_{DD}$  exceeds  $V_{DD(max)}$ . See **Power Up and Power Down Sequencing** below.

<sup>2</sup>  $V_{IH(max)} = V_{DD} + 0.3 V_{DC}$ ;  $V_{IH(max)} = V_{DD} + 2.0 V_{AC}$  (pulse width  $\leq 10$  ns) for  $I \leq 20.0$  mA.

<sup>3</sup>  $V_{IL(min)} = -0.5 V_{DC}$ ;  $V_{IL(min)} = -2.0 V_{AC}$  (pulse width  $\leq 10$  ns) for  $I \leq 20.0$  mA.

<sup>4</sup> AEC-Q100 Grade 1 temperature profile assumes 10% duty cycle at maximum temperature (2 years out of 20 years life.)

### Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever  $V_{DD}$  is less than  $V_{WI}$ . As soon as  $V_{DD}$  exceeds  $V_{DD(min)}$ , there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The  $\bar{E}$  and  $\bar{W}$  control signals should track  $V_{DD}$  on power up to  $V_{DD} - 0.2$  V or  $V_{IH}$  (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives E and W should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where  $V_{DD}$  goes below  $V_{WI}$ , writes are protected and a startup time must be observed when power returns above  $V_{DD(min)}$ .

Figure 2.1 Power Up and Power Down Diagram

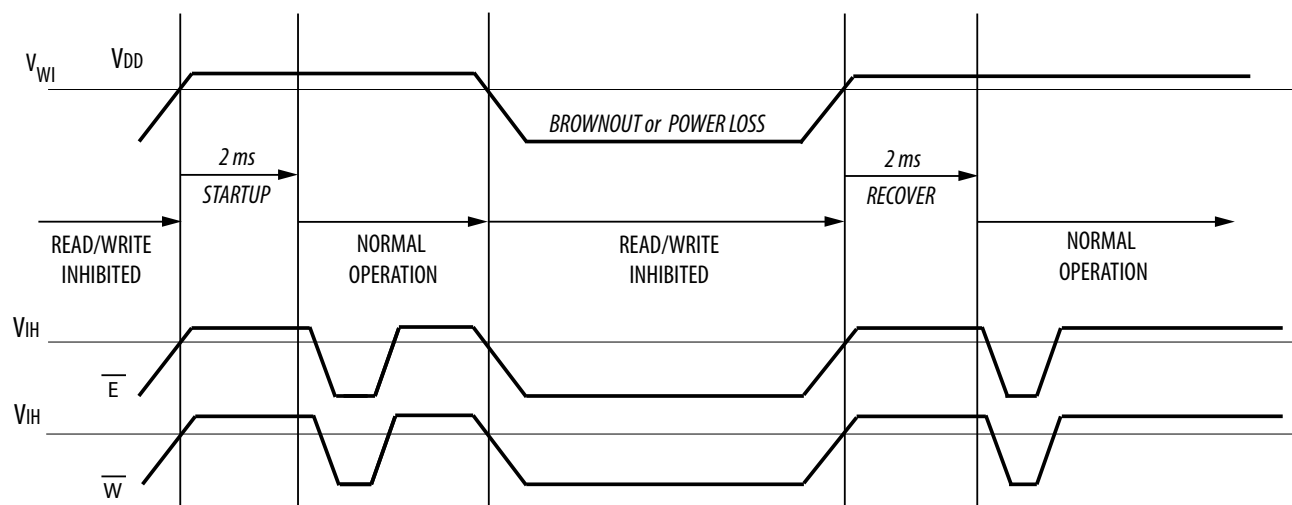


Table 2.3 DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	$I_{lkg(I)}$	-	-	$\pm 1$	$\mu\text{A}$
Output leakage current	$I_{lkg(O)}$	-	-	$\pm 1$	$\mu\text{A}$
Output low voltage ( $I_{OL} = +4 \text{ mA}$ ) ( $I_{OL} = +100 \mu\text{A}$ )	$V_{OL}$	-	-	0.4 $V_{SS} + 0.2$	V
Output high voltage ( $I_{OH} = -4 \text{ mA}$ ) ( $I_{OH} = -100 \mu\text{A}$ )	$V_{OH}$	2.4 $V_{DD} - 0.2$	-	-	V

Table 2.4 Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes <sup>1</sup> ( $I_{OUT} = 0 \text{ mA}$ , $V_{DD} = \text{max}$ )	$I_{DDR}$	55	80	mA
AC active supply current - write modes <sup>1</sup> ( $V_{DD} = \text{max}$ ) Commercial Grade Industrial Grade Extended Grade AEC-Q100 Grade	$I_{DDW}$	105 105 105 105	155 165 165 165	mA
AC standby current ( $V_{DD} = \text{max}$ , $\bar{E} = V_{IH}$ ) <i>no other restrictions on other inputs</i>	$I_{SB1}$	18	28	mA
CMOS standby current ( $\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$ ) ( $V_{DD} = \text{max}$ , $f = 0 \text{ MHz}$ )	$I_{SB2}$	9	12	mA

<sup>1</sup> All active current measurements are measured with one address transition per cycle and at minimum cycle time.

### 3. TIMING SPECIFICATIONS

**Table 3.1 Capacitance<sup>1</sup>**

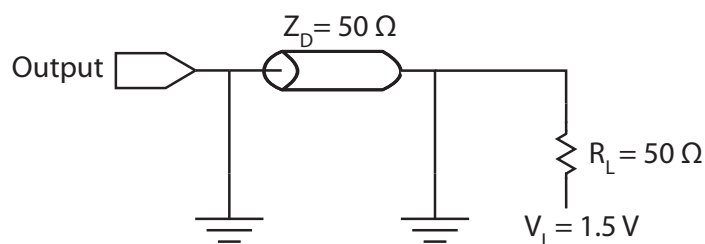
Parameter	Symbol	Typical	Max	Unit
Address input capacitance	$C_{In}$	-	6	pF
Control input capacitance	$C_{In}$	-	6	pF
Input/Output capacitance	$C_{I/O}$	-	8	pF

<sup>1</sup>  $f = 1.0 \text{ MHz}$ ,  $dV = 3.0 \text{ V}$ ,  $T_A = 25 \text{ }^\circ\text{C}$ , periodically sampled rather than 100% tested.

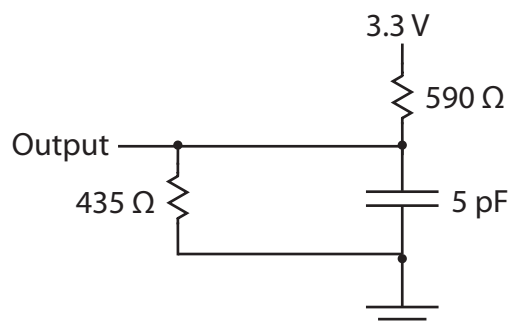
**Table 3.2 AC Measurement Conditions**

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 3.1	
Output load for all other timing parameters	See Figure 3.2	

**Figure 3.1 Output Load Test Low and High**



**Figure 3.2 Output Load Test All Others**



Read Mode

Table 3.3 Read Cycle Timing<sup>1</sup>

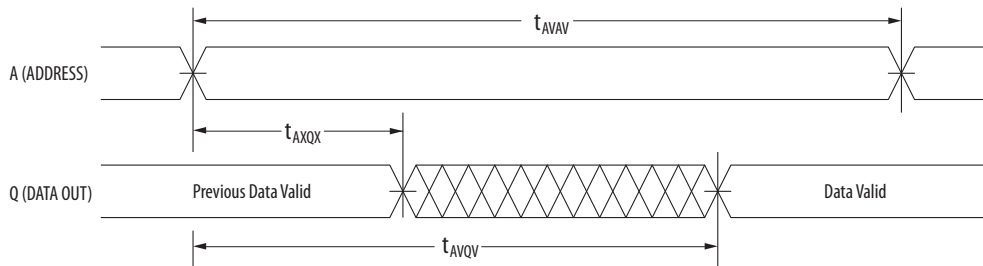
Parameter	Symbol	Min	Max	Unit
Read cycle time	$t_{AVAV}$	35	-	ns
Address access time	$t_{AVQV}$	-	35	ns
Enable access time <sup>2</sup>	$t_{ELOV}$	-	35	ns
Output enable access time	$t_{GLOV}$	-	15	ns
Byte enable access time	$t_{BLOV}$	-	15	ns
Output hold from address change	$t_{AXOX}$	3	-	ns
Enable low to output active <sup>3</sup>	$t_{ELOX}$	3	-	ns
Output enable low to output active <sup>3</sup>	$t_{GLOX}$	0	-	ns
Byte enable low to output active <sup>3</sup>	$t_{BLOX}$	0	-	ns
Enable high to output Hi-Z <sup>3</sup>	$t_{EHOZ}$	0	15	ns
Output enable high to output Hi-Z <sup>3</sup>	$t_{GHOZ}$	0	10	ns
Byte high to output Hi-Z <sup>3</sup>	$t_{BHOZ}$	0	10	ns

<sup>1</sup>  $\overline{W}$  is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

<sup>2</sup> Addresses valid before or at the same time  $\overline{E}$  goes low.

<sup>3</sup> This parameter is sampled and not 100% tested. Transition is measured  $\pm 200$  mV from the steady-state voltage.

Figure 3.3A Read Cycle 1



Note: Device is continuously selected ( $\overline{E} \leq V_{IL}$ ,  $\overline{G} \leq V_{IL}$ ).

Figure 3.3B Read Cycle 2

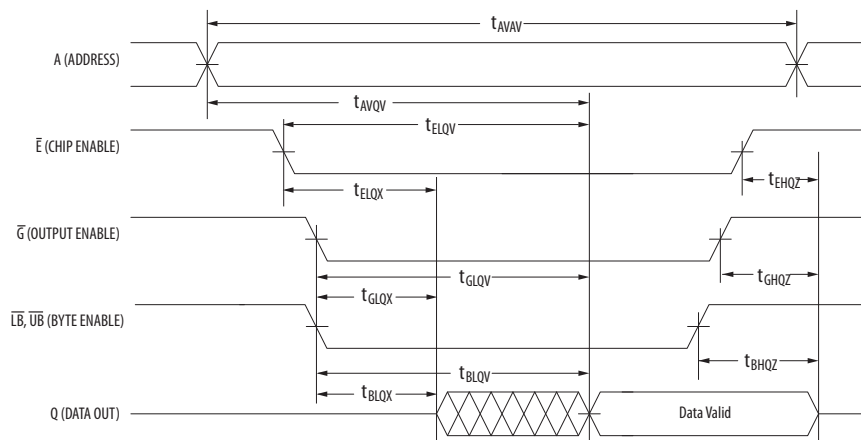




Table 3.4 Write Cycle Timing 1 ( $\overline{W}$  Controlled)<sup>1</sup>

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>2</sup>	$t_{AVAV}$	35	-	ns
Address set-up time	$t_{AVWL}$	0	-	ns
Address valid to end of write (G high)	$t_{AVWH}$	18	-	ns
Address valid to end of write (G low)	$t_{AVWH}$	20	-	ns
Write pulse width (G high)	$t_{WLWH}$ $t_{WLEH}$	15	-	ns
Write pulse width (G low)	$t_{WLWH}$ $t_{WLEH}$	15	-	ns
Data valid to end of write	$t_{DVWH}$	10	-	ns
Data hold time	$t_{WHDX}$	0	-	ns
Write low to data Hi-Z <sup>3</sup>	$t_{WLQZ}$	0	12	ns
Write high to output active <sup>3</sup>	$t_{WHQX}$	3	-	ns
Write recovery time	$t_{WHAX}$	12	-	ns

<sup>1</sup> All write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high impedance state. After  $\overline{W}$ ,  $\overline{E}$  or  $\overline{UB/LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

<sup>2</sup> All write cycle timings are referenced from the last valid address to the first transition address.

<sup>3</sup> This parameter is sampled and not 100% tested. Transition is measured  $\pm 200$  mV from the steady-state voltage. At any given voltage or temperature,  $t_{WLQZ}(\max) < t_{WHQX}(\min)$

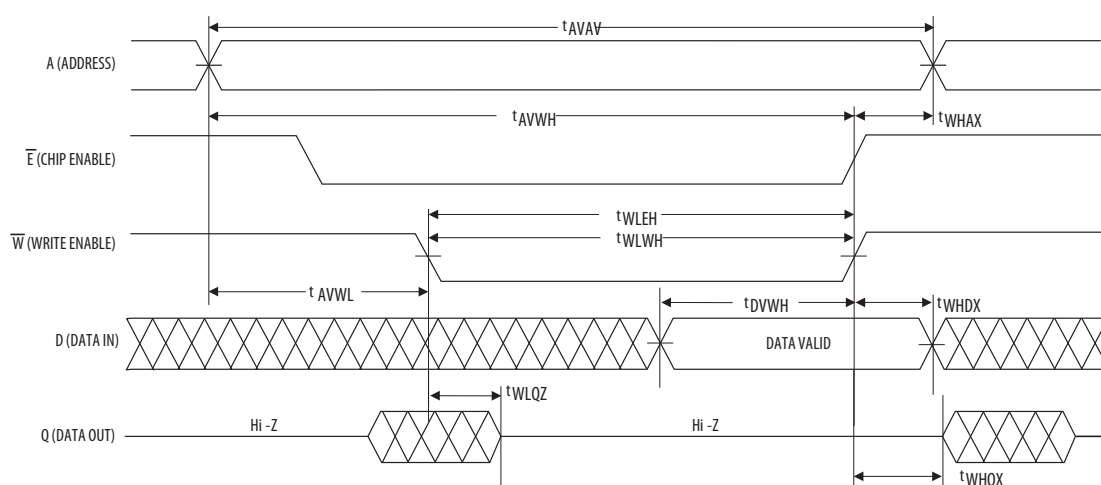
Figure 3.4 Write Cycle Timing 1 ( $\overline{W}$  Controlled)

Table 3.5 Write Cycle Timing 2 ( $\bar{E}$  Controlled)<sup>1</sup>

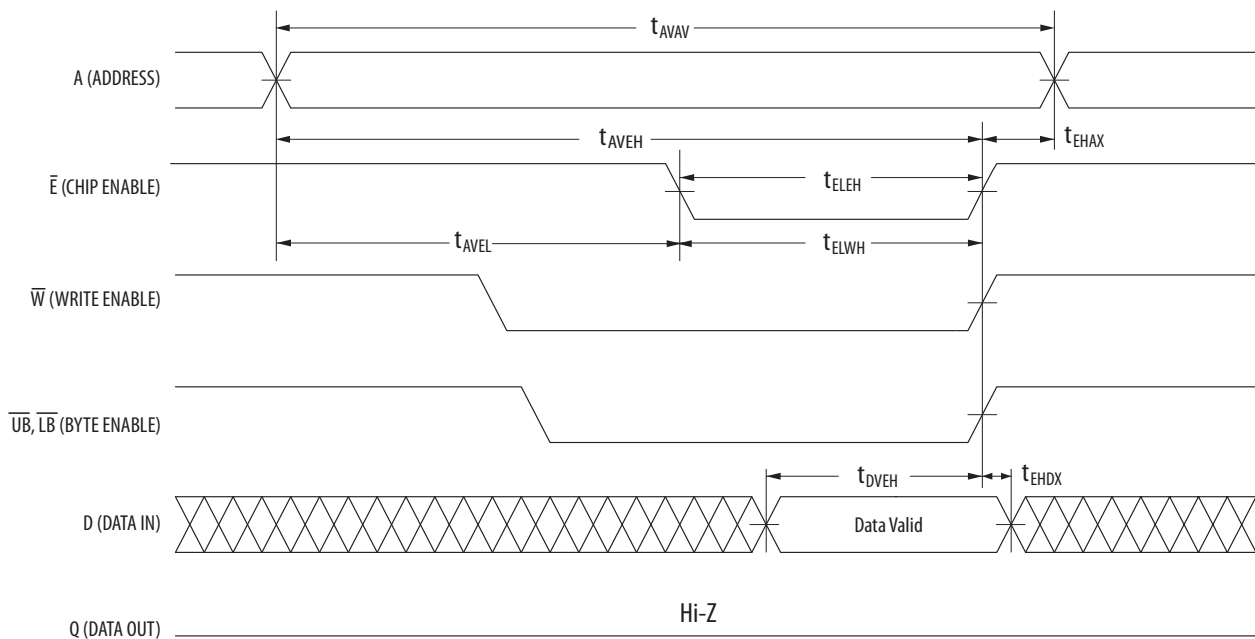
Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>2</sup>	$t_{AVAV}$	35	-	ns
Address set-up time	$t_{AVEL}$	0	-	ns
Address valid to end of write ( $\bar{G}$ high)	$t_{AVEH}$	18	-	ns
Address valid to end of write ( $\bar{G}$ low)	$t_{AVEH}$	20	-	ns
Enable to end of write ( $\bar{G}$ high)	$t_{ELEH}$ $t_{ELWH}$	15	-	ns
Enable to end of write ( $\bar{G}$ low) <sup>3</sup>	$t_{ELEH}$ $t_{ELWH}$	15	-	ns
Data valid to end of write	$t_{DVEH}$	10	-	ns
Data hold time	$t_{EHDX}$	0	-	ns
Write recovery time	$t_{EHAX}$	12	-	ns

<sup>1</sup> All write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If  $\bar{G}$  goes low at the same time or after  $\bar{W}$  goes low, the output will remain in a high impedance state. After  $\bar{W}$ , E or  $\bar{UB}/\bar{LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between  $\bar{E}$  being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

<sup>2</sup> All write cycle timings are referenced from the last valid address to the first transition address.

<sup>3</sup> If  $\bar{E}$  goes low at the same time or after  $\bar{W}$  goes low, the output will remain in a high-impedance state. If  $\bar{E}$  goes high at the same time or before  $\bar{W}$  goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 ( $\bar{E}$  Controlled)<sup>1</sup>



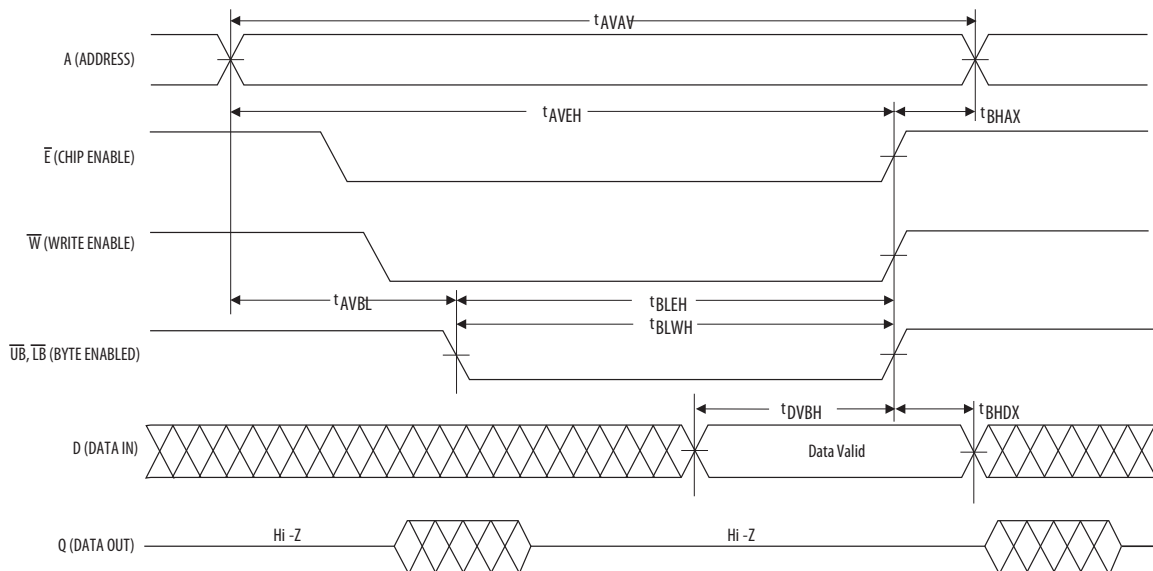
**Table 3.6 Write Cycle Timing 3 ( $\overline{\text{LB}} / \overline{\text{UB}}$  Controlled)<sup>1</sup>**

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>2</sup>	$t_{\text{AVAV}}$	35	-	ns
Address set-up time	$t_{\text{AVBL}}$	0	-	ns
Address valid to end of write ( $\overline{\text{G}}$ high)	$t_{\text{AVBH}}$	18	-	ns
Address valid to end of write ( $\overline{\text{G}}$ low)	$t_{\text{AVBH}}$	20	-	ns
Write pulse width ( $\overline{\text{G}}$ high)	$t_{\text{BLEH}}$ $t_{\text{BLWH}}$	15	-	ns
Write pulse width ( $\overline{\text{G}}$ low)	$t_{\text{BLEH}}$ $t_{\text{BLWH}}$	15	-	ns
Data valid to end of write	$t_{\text{DVBH}}$	10	-	ns
Data hold time	$t_{\text{BHDX}}$	0	-	ns
Write recovery time	$t_{\text{BHAX}}$	12	-	ns

<sup>1</sup> All write occurs during the overlap of  $\overline{\text{E}}$  low and  $\overline{\text{W}}$  low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If  $\overline{\text{G}}$  goes low at the same time or after  $\overline{\text{W}}$  goes low, the output will remain in a high impedance state. After  $\overline{\text{W}}$ ,  $\overline{\text{E}}$  or  $\overline{\text{LB}}/\overline{\text{UB}}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between  $\overline{\text{E}}$  being asserted low in one cycle to E being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

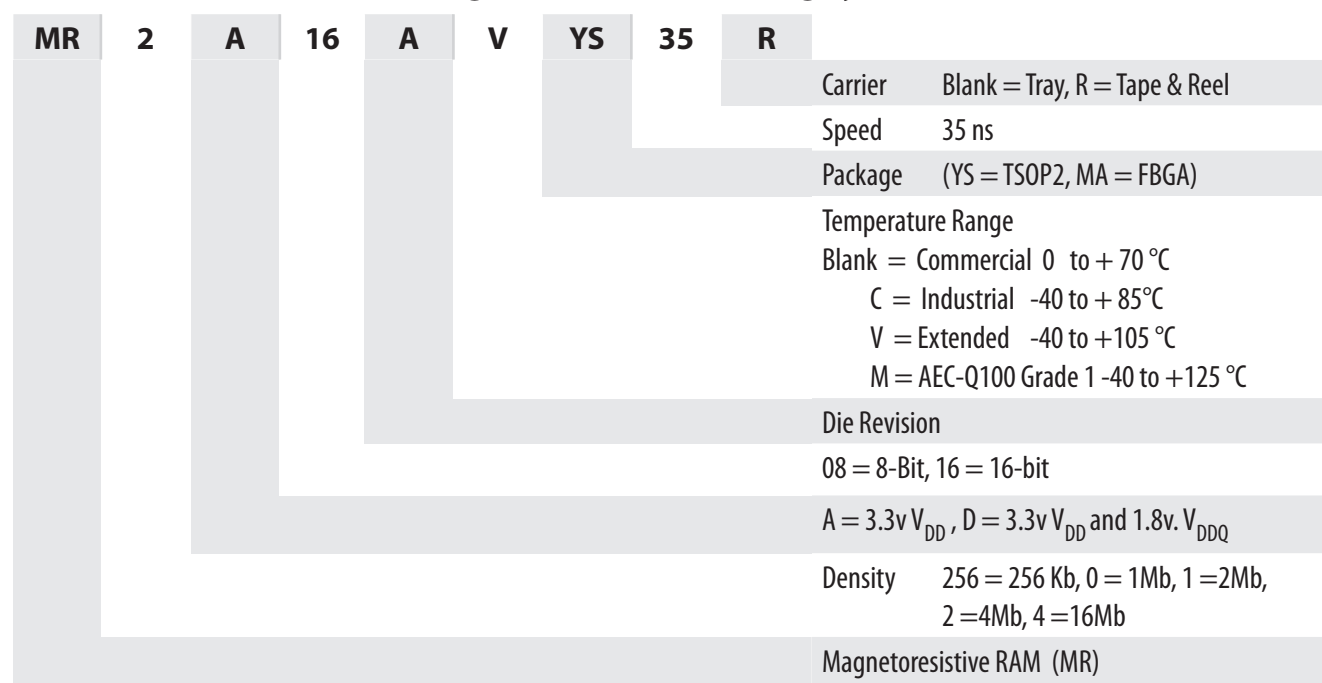
<sup>2</sup> All write cycle timings are referenced from the last valid address to the first transition address.

**Figure 3.6 Write Cycle Timing 3 ( $\overline{\text{LB}} / \overline{\text{UB}}$  Controlled)**



## 4. ORDERING INFORMATION

**Figure 4.1 Part Numbering System**



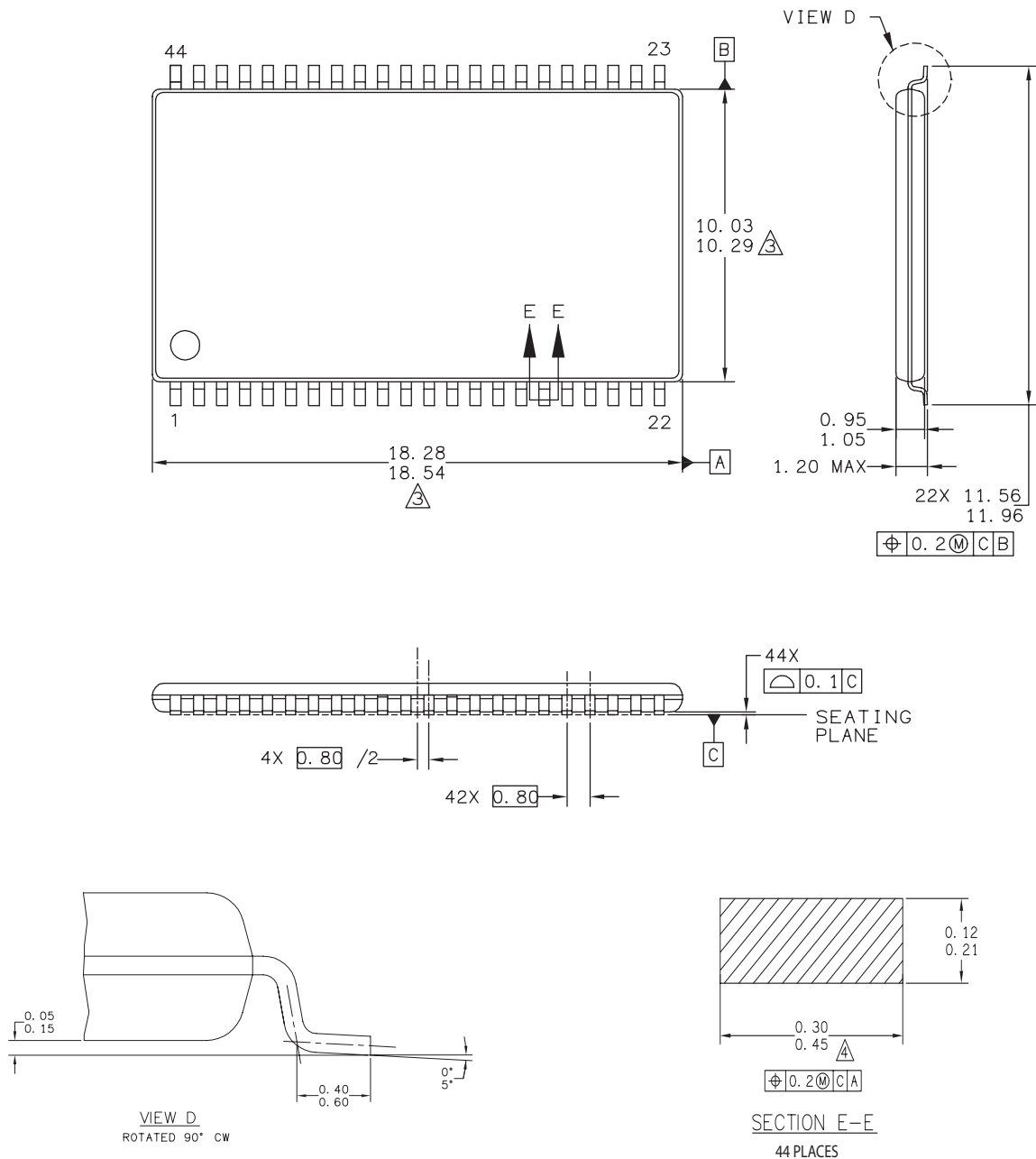
**Table 4.1 Available Parts**

Part Number	Description - Operating Temperature Grade	Package	Ship Pack	Temp Range
MR2A16AYS35	3.3v 256Kx16 MRAM Commercial	44-TSOP2	Tray	0 to +70 °C
MR2A16ACYS35	3.3v 256Kx16 MRAM Industrial	44-TSOP2	Tray	-40 to +85 °C
MR2A16AVYS35	3.3v 256Kx16 MRAM Extended	44-TSOP2	Tray	-40 to +105 °C
MR2A16AMYS35 <sup>1</sup>	3.3v 256Kx16 MRAM AEC-Q100 Grade 1	44-TSOP2	Tray	-40 to +125 °C
MR2A16AYS35R	3.3v 256Kx16 MRAM Commercial	44-TSOP2	Tape & Reel	0 to +70 °C
MR2A16ACYS35R	3.3v 256Kx16 MRAM Industrial	44-TSOP2	Tape & Reel	-40 to +85 °C
MR2A16AVYS35R	3.3v 256Kx16 MRAM Extended	44-TSOP2	Tape & Reel	-40 to +105 °C
MR2A16AMYS35R <sup>1</sup>	3.3v 256Kx16 MRAM AEC-Q100 Grade 1	44-TSOP2	Tape & Reel	-40 to +125 °C
MR2A16AMA35	3.3v 256Kx16 MRAM Commercial	48-BGA	Tray	0 to +70 °C
MR2A16ACMA35	3.3v 256Kx16 MRAM Industrial	48-BGA	Tray	-40 to +85 °C
MR2A16AVMA35	3.3v 256Kx16 MRAM Extended	48-BGA	Tray	-40 to +105 °C
MR2A16AMA35R	3.3v 256Kx16 MRAM Commercial	48-BGA	Tape & Reel	0 to +70 °C
MR2A16ACMA35R	3.3v 256Kx16 MRAM Industrial	48-BGA	Tape & Reel	-40 to +85 °C
MR2A16AVMA35R	3.3v 256Kx16 MRAM Extended	48-BGA	Tape & Reel	-40 to +105 °C

<sup>1</sup> Preliminary Products: These products are classified as Preliminary until the completion of all qualification tests. The specifications in this data sheet are intended to be final but are subject to change. Please check the Everspin web site [www.everspin.com](http://www.everspin.com) for the latest information on product status.

## 5. MECHANICAL DRAWING

Figure 5.1 44-TSOP2



**Print Version Not To Scale**

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.  
DAM Bar protrusion shall not cause the lead width to exceed 0.58.



## 6. REVISION HISTORY

Revision	Date	Description of Change
5	Sept 21, 2007	Changed MR2A16ATS35C product description to Legacy Commercial. Added the New Commercial temperature product (MR2A16AYS35) information. Table 3: MR2A16AYS35 Hmax-write=25 Oe. Table 4: MR2A16AYS35 has a 2 ms power up waiting period. Table 6: Applied values to TBD's in IDD specifications.
6	Nov 12, 2007	Table 2: Changed IDDA to IDDR or IDDW. Table 13: Added note indicating that TS and YS are both valid package codes. Current Part Numbering System: Added commercial (missing letter) temperature range.
7	Sep 12, 2008	Reformat Datasheet for EverSpin, Add BGA Packaging Information, Add Tape & Reel Part Numbers, Add Power Sequencing Info, Correct IOH spec of VOH to -100 uA, Correct ac Test Conditions.
8	July 22, 2009	Add TSOP2 Lead Cross-Section, Add Production Note. Converted to new document format.
9	Dec 16, 2011	Added AEC-Q100 Grade 1 product option for TSOP2 package to Table 4.1. Revised Tables 2.1, 2.2 and 4.1 to include AEC-Q100 Grade 1 specifications. New logo design.
10	August 29, 2012	Corrected error in Table 1.1. Corrected Figure 2.1. Improved magnetic immunity for Industrial and Extended Grades. Corrected minor errors in Table 4.1 Product Numbering.
10.1	July 30, 2013	Corrected G to read $\bar{G}$ for 44-TSOP Type2 in Figure 1.2.

### How to Reach Us:

Home Page:  
www.everspin.com

### E-Mail:

support@everspin.com  
orders@everspin.com  
sales@everspin.com

### USA/Canada/South and Central America

Everspin Technologies  
1347 N. Alma School Road, Suite 220  
Chandler, Arizona 85224  
+1-877-347-MRAM (6726)  
+1-480-347-1111

### Europe, Middle East and Africa

support.europe@everspin.com

### Japan

support.japan@everspin.com

### Asia Pacific

support.asia@everspin.com

### Filename:

EST00193\_MR2A16B\_Datasheet\_Rev10.pdf

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.

©Everspin Technologies, Inc. 2012

