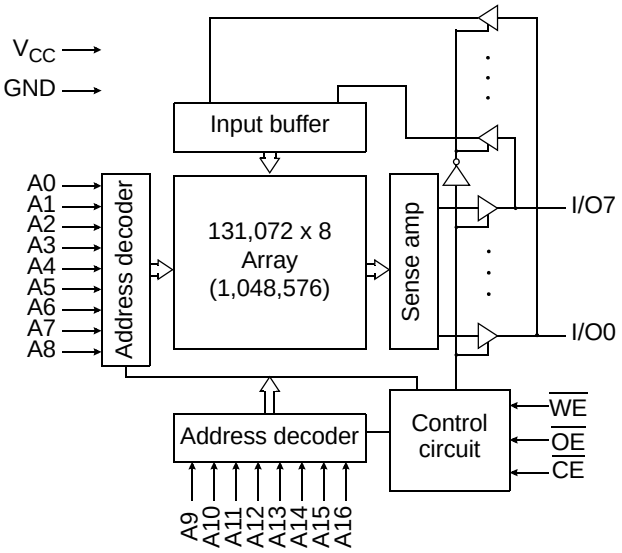
3.3V 128K X 8 CMOS SRAM (Center power and ground)

Features

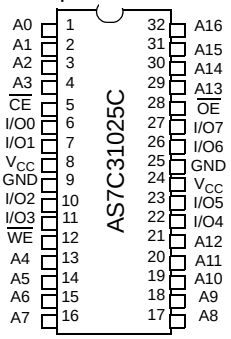
- Industrial and commercial temperatures
- Organization: 131,072 x 8 bits
- High speed
  - 10/12 ns address access time
  - 5 ns output enable access time
- Low power consumption via ship deselect
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- Center power and ground
- TTL/LVTTL-compatible, three-state I/O
- JEDEC-standard packages
  - 32-pin, 300 mil SOJ
  - 32-pin, 400 mil SOJ
  - 32-pin, TSOP 2
- ESD protection ≥ 2000 volts

Logic block diagram

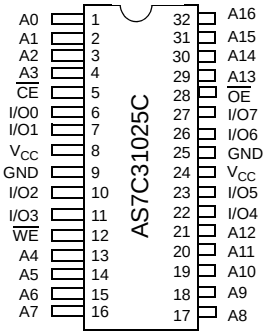


Pin arrangement

32-pin TSOP 2



32-pin SOJ (300 mil)
32-pin SOJ (400 mil)



Functional description

The AS7C31025C is 3V a high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) device organized as 131,072 x 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10 ns with output enable access times (t_{OE}) of 5 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory and expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the device enters standby mode. A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0 throug h I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus co ntention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word ref erenced by the input address. When either chip enable or output en able is inactive or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 3.3 V supply. The AS7C31025C is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.50	+4.6	V
Voltage on any pin relative to GND	V_{t2}	–0.50	V_{CC} + 0.5	V
Power dissipation	P_D	–	1.25	W
Storage temperature (plastic)	T_{stg}	–55	+125	^oC
Ambient temperature with V_{CC} applied	T_{bias}	–55	+125	^oC
DC current into outputs (low)	I_{OUT}	–	50	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Key: X = don't care, L = low, H = high.