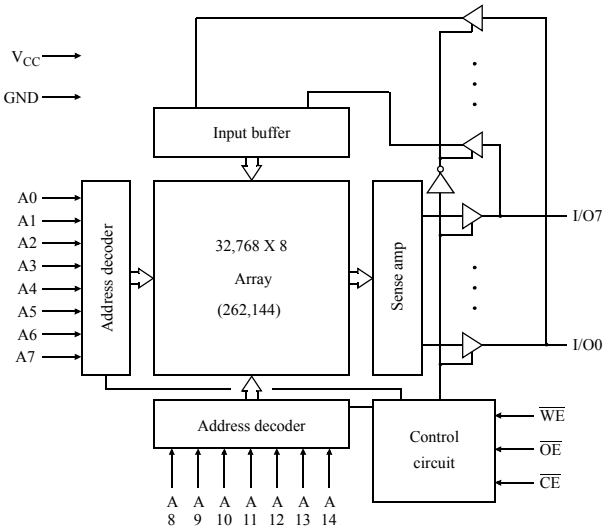
5V 32K X 8 CMOS SRAM (Common I/O)

Features

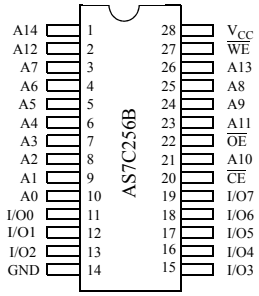
- Industrial (-40° to 85°C) temperature
- Organization: 32,768 words × 8 bits
- High speed
  - 15 ns address access time
  - 6 ns output enable access time
- Low power consumption via chip deselect
- One chip select plus one Output Enable pin
- Bidirectional data inputs and outputs
- TTL-compatible
- 28-pin JEDEC standard packages
  - 300 mil SOJ
  - 8 × 13.4 mm TSOP
  - 300 mil PDIP
- ESD protection ≥ 2000 volts

Logic block diagram

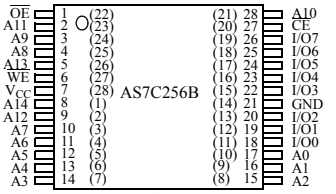


Pin arrangement

28-pin DIP, SOJ (300 mil)



28-pin TSOP 1 (8×13.4mm)



Note: This part is compatible with both pin numbering conventions used by various manufacturers.

Functional description

The AS7C256B is a 5V high-performance CMOS 262,144-bit Static Random-Access Memory (SRAM) device organized as 32,768 words × 8 bits. It is designed for memory applications requiring fast data access at low voltage, including Pentium™, PowerPC™, and port able computing. All iance's advanced circuit design and process t echniques permit 5.0V op eration without sacrificing performance or operating margins.

The device enters *standby mode* when $\overline{CE}$ is high. Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 12 ns with output enable access times (t_{OE}) of 6 ns are ideal for high-performance applications. The chip enable ($\overline{CE}$) input permits easy memory expansion with multiple-bank memory organizations.

A write cycle is accomplished by asserting chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is high, or write enable is low, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible. Operation is from a single 5.0±0.5V supply. The AS7C256B is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.5	+7.0	V
Voltage on any pin relative to GND	V_{t2}	–0.5	V_{CC} + 0.5	V
Power dissipation	P_D	–	1.25	W
Storage temperature (plastic)	T_{stg}	–55	+125	°C
Ambient temperature with V_{CC} applied	T_{bias}	–55	+125	°C
DC current into outputs (low)	I_{OUT}	–	50	mA

Note:
Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress ratin g only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Notes:
H = V_{IH}, L = V_{IL}, x = Don't care.
V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V.
Other inputs ≥ V_{HC} or V_{LC}.