

512Mbit Single-Data-Rate (SDR) SDRAM

AS4C64M8S-7TCN 64Mx8 (16M x 8 x 4 Banks)

AS4C32M16S-7TCN 32Mx16 (8M x 16 x 4 Banks)

Revision History

Rev. 1.1 April 2012

Revised Operating-, Standby- and Refresh Currents

Rev. 1.0 March 2012

initial version

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document.

1 | Overview

This chapter gives an overview of the 512Mbit SDRAM product and describes its main characteristics.

1.1 Features

- Single 3.3 V \pm 0.3 V Power Supply
- LVTTTL – compatible I/O
- DRAM organizations with 8, 16 Data In/Outputs
- Single Pulsed $\overline{\text{RAS}}$ interface
- Fully synchronous to Positive Clock Edge
- Four Banks controlled by BA0/BA1 (Bank Select)
- Programmable CAS Latency: 2, 3
- Programmable Burst Length: 1,2,4,8 or full page
- Programmable Wrap: Sequential or Interleave
- Multiple Burst Read with Single Write Option
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write Control (x8)
- Dual Data Mask for byte control (x16)
- Suspend Mode and Power Down Mode
- Standard Power Operation
- Random Column Address every CK (1-N Rule)
- Operating Temperature range 0°C to 70°C. Industrial Temperature devices (Ordering code ending with "I") allow an operating temperature range of -40°C to 85°C¹
- Auto Refresh(CBR) and Self Refresh
- 8192 Refresh Cycles/64ms
- 54-pin TSOP II (400 mil) Package
- RoHS Compliant Product²
- Electrically and mechanically JEDEC compliant

¹ ambient Temperature

² RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit <http://www.alliancememory.com>

Table 1 - Performance Table

				Unit	Note
Speed Code			-7/-7I	-7A/-7AI ¹	
Max. Data Rate	SDR		133	133	MHz
CAS-RCD-RP Latencies			3-3-3	2-2-2	t _{CK} ¹
Max. Clock Frequency	CL3	f _{CK3}	133	133	MHz
	CL2	f _{CK2}	100	133	MHz
Min. RAS-CAS-Delay		t _{RCD}	20	15	ns
Min. Row Precharge Time		t _{RP}	20	15	ns
Min. Row Active Time		t _{RAS}	45	42	ns
Min. Row Cycle Time		t _{RC}	67.5	60	ns

¹ Versions marked -7A(I) support both: 2-2-2 and 3-3-3 at 133MHz (CAS-RCD-RP)

1.2 Description

The 512Mbit SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits internally configured as a quad-bank DRAM with a synchronous interface.

The x8 device is organized as 16M × 8 I/O × 4 banks, the x16 device is organized as 8M × 16 I/O × 4 banks. These synchronous devices achieve data transfer rates of up to 133 Mb/sec/pin for general applications.

See Table 1 for performance figures.

The device is designed in compliance with JEDEC standards for SDRAM memory components both electrically and mechanically.

The control signals \overline{RAS} , \overline{CAS} , \overline{WE} and \overline{CS} are pulsed signals which are sampled at the positive edge of each externally applied clock (CK).

A thirteen bit address bus A[12:0] together with 2 Bank select lines BA[1:0] accept address data in a $\overline{RAS}/\overline{CAS}$ multiplexing style.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 133 MHz is possible depending on Burst Length and \overline{CAS} Latency. Auto Refresh (CBR) and Self Refresh operation, both are supported. The 512Mb SDRAM is available in 54-pin TSOP-Type II package.

Table 2 - Ordering Information for RoHS Compliant Products

Product Part Number ¹	Org.	CAS-RCD-RP Latencies ^{2 3 4}	Max. Clock (MHz)	Package	Note
Standard Temperature Range (0°C to 70°C) ⁶					
AS4C64M8S-7TCN	×8	3-3-3	133	54 TSOP II	⁵
AS4C32M16S-7TCN	×16	3-3-3	133	54 TSOP II	⁵
AS4C64M8S-7A	×8	2-2-2	133	54 TSOP II	^{5 7}
AS4C32M16S-7A	×16	2-2-2	133	54 TSOP II	^{5 7}
Industrial Temperature Range (-40°C to 85°C) ⁶					
AS4C64M8S-7TIN	×8	3-3-3	133	54 TSOP II	⁵
AS4C32M16S-7TIN	×16	3-3-3	133	54 TSOP II	⁵
AS4C64M8S-7AI	×8	2-2-2	133	54 TSOP II	^{5 7}
AS4C32M16S-7AI	×16	2-2-2	133	54 TSOP II	^{5 7}

¹ For detailed information regarding the part numbering of Alliance Memory products, please contact Alliance Memory for a separated "Part No. Decoder".

² CAS: Column Address Strobe

³ RCD: Row Column Delay

⁴ RP: Row Precharge

⁵ RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit <http://www.alliancememory.com>

⁶ Operating ambient temperature surrounding the package

⁷ Versions marked **-7A** support both: **2-2-2** and **3-3-3** (CAS-RCD-RP)

1.3 Addressing

Table 3 - Addressing

Configuration	64 Mb x 8 ¹	32 Mb x16 ¹	Note
Bank Address	BA[1:0]	BA[1:0]	
Number of Banks	4	4	
Auto Precharge	A10 / AP	A10 / AP	
Auto Refresh Cycles	8192	8192	
Row Address	A[12:0]	A[12:0]	
Column Address	A[9:0] A11	A[9:0]	
Number of I/Os	8	16	

Notes:

¹ Referred to as 'org'

2 | Configuration

This chapter contains the chip configuration.

2.1 Configuration for 54-pin TSOP II Package

The chip configuration of the SDRAM is listed by function in Table 3. The abbreviations used in the Pin# and Buffer Type column are explained in Table 4 and Table 5 respectively.

Table 4 - PIN Description for 54-pin TSOP II Package

Pin#	Name x8 ¹	Name x16 ¹	Pin Type	Buffer Type	Function
Clock Signals					
38	CLK	CLK	I	LVTTTL	Clock Signal, all SDRAM Inputs are sampled on the rising edge of the clock
37	CKE	CKE	I	LVTTTL	Clock Enable activates (HIGH) and deactivates (LOW) the CLK Signal
Control Signals					
18	$\overline{\text{RAS}}$	$\overline{\text{RAS}}$	I	LVTTTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)
17	$\overline{\text{CAS}}$	$\overline{\text{CAS}}$	I	LVTTTL	
16	$\overline{\text{WE}}$	$\overline{\text{WE}}$	I	LVTTTL	
19	$\overline{\text{CS}}$	$\overline{\text{CS}}$	I	LVTTTL	Chip Select enables (registered LOW) and disables (registered HIGH) the command decoder
Address Signals					
20	BA0	BA0	I	LVTTTL	Bank Address Bus BA[1:0]
21	BA1	BA1	I	LVTTTL	
23	A0	A0	I	LVTTTL	Address Inputs A[12:0]
24	A1	A1	I	LVTTTL	
25	A2	A2	I	LVTTTL	
26	A3	A3	I	LVTTTL	
29	A4	A4	I	LVTTTL	
30	A5	A5	I	LVTTTL	
31	A6	A6	I	LVTTTL	
32	A7	A7	I	LVTTTL	
33	A8	A8	I	LVTTTL	
34	A9	A9	I	LVTTTL	
22	A10	A10	I	LVTTTL	
35	A11	A11	I	LVTTTL	
36	A12	A12	I	LVTTTL	

- continued next page -

Notes:

¹ Referred to as 'org'

Continued Table 4 - PIN Description for 54-pin TSOP II Package

PIN#	Name x8	Name x16	PIN Type	Buffer Type	Function
Data Signals					
2	DQ0	DQ0	I/O	LVTTTL	Data Signal DQ[7:0] for x8 Data Signal DQ[15:0] for x16
4	NC	DQ1	I/O	LVTTTL	
5	DQ1	DQ2	I/O	LVTTTL	
7	NC	DQ3	I/O	LVTTTL	
8	DQ2	DQ4	I/O	LVTTTL	
10	NC	DQ5	I/O	LVTTTL	
11	DQ3	DQ6	I/O	LVTTTL	
42	NC	DQ8	I/O	LVTTTL	
44	DQ4	DQ9	I/O	LVTTTL	
45	NC	DQ10	I/O	LVTTTL	
47	DQ5	DQ11	I/O	LVTTTL	
48	NC	DQ12	I/O	LVTTTL	
50	DQ6	DQ13	I/O	LVTTTL	
51	NC	DQ14	I/O	LVTTTL	
53	DQ7	DQ15	I/O	LVTTTL	
13	NC	DQ7	I/O	LVTTTL	
Data Mask					
15	NC	DQML	I	LVTTTL	Data Mask
39	DQM	DQMH	I	LVTTTL	Data Mask
Power Supplies					
3, 9, 43, 49	V _{DDQ}	V _{DDQ}	PWR	–	DQ Power: DQ Power to the die for improved noise immunity
1, 14, 27	V _{DD}	V _{DD}	PWR	–	Power Supply +3.3V ± 0.3V
6, 12, 46, 52	V _{SSQ}	V _{SSQ}	PWR	–	DQ Ground: isolated power supply and ground for the output buffers for improved noise immunity
28, 41, 54	V _{SS}	V _{SS}	PWR	–	Power Supply Ground
Not Connected					
40	NC	NC	NC	–	Not Connected

Table 5 - Abbreviations for Pin Type

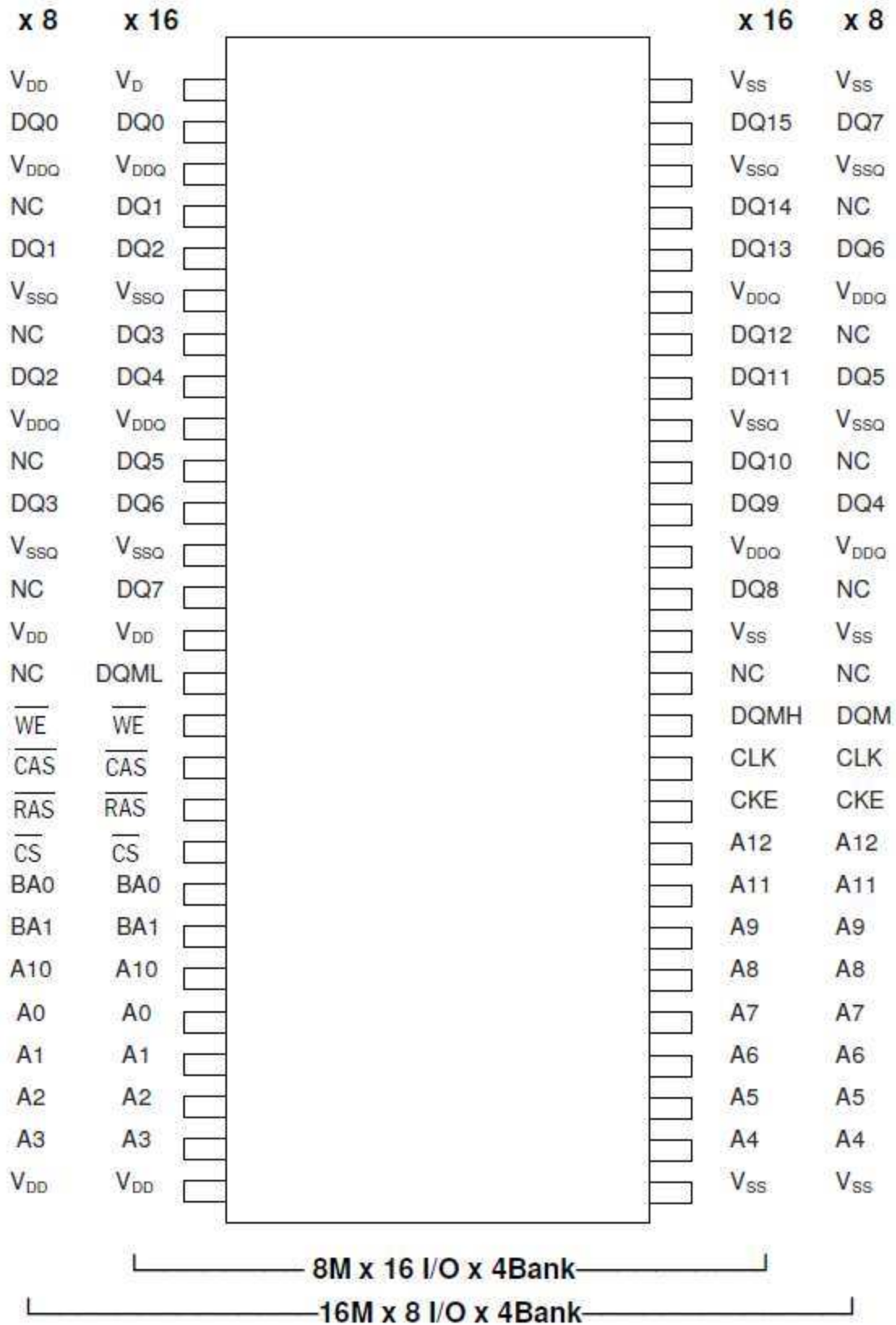
Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional Input/Output signal.
PWR	Power
GND	Ground
NC	Not Connected

Table 6 - Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LVTTL	Low Voltage TTL
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR allows multiple devices to share as a wire-OR.

Figure 1 - Ball Assignment for x8 and x16 Components, TSOP-54 (II)

54-pin TSOP (II) 400 mil (Top View)



3 | Functional Description

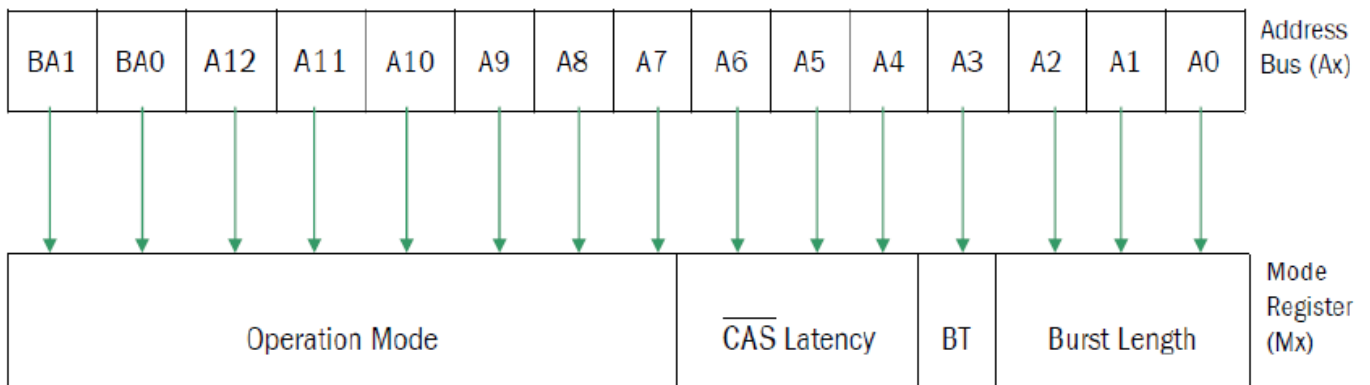
3.1 Mode Register Set (MRS)

The Mode Register ¹ stores data defining the specific mode of operation including Burst Length (BL), Burst Type, CAS Latency (CL)², Operating Mode and write Burst Mode of the SDRAM. Since power on state of the register is not defined it must be initialized in order to avoid unpredictable start-up modes.

The Mode Register content can be altered by re-executing the Mode Register Set Command if needed.

In such a case however all 4 variables must be redefined when the Mode Register Set Command is issued.

Figure 2 – Mode Register Structure



¹ Operation Mode, CAS Latency, Burst Type and Burst Length are user defined variables and must be programmed into the Mode Register before Read or Write Cycles may begin. The Mode Register is programmed using the Mode Register Set Command. It retains the data until it is reprogrammed or power is switched off the SDRAM.

² CAS Latency defines the delay from when a Read Command is registered on a rising Clock Edge to when the data from that Read Command becomes available at the Data I/O's.

Table 7 - Mode Register (MR) Definition

Field	Bits	Type ¹	Description
Operation Mode	[14:7]	w	0000000B Normal Mode 00000100B Multiple Burst with Single Write All other states reserved.*
CL	[6:4]	w	CAS Latency Note: All other bit combinations are reserved. 010 _B CL 2 011 _B CL 3
BT	3	w	Burst Type 0 _B BT Sequential 1 _B BT Interleaved
BL	[2:0]	w	Burst Length Note: All other bit combinations are reserved. BT (Bit3=0) BT (Bit3=0) 000 _B Sequential BL: 1 Interleave BL: 1 001 _B Sequential BL: 2 Interleave BL: 2 010 _B Sequential BL: 4 Interleave BL: 4 011 _B Sequential BL: 8 Interleave BL: 8 111 _B Sequential: Full Page Interleave BL: 8

¹ w = write only register bits

* BA1 and BA0 must be set to "0" when programming Mode Register MR

M9 (Write

Burst Mode): 0 -> Normal Mode (read and write with programmed Burst Length) 1 -> Multiple Burst & Single Write location access

3.2 Burst Mode Operation

Read and Write Operations to the device are burst oriented.

The Burst Type defines the sequence in which the data is Output and Input to the device. The Burst Types supported are sequential and interleaved. Please refer to the below table.

The Burst Length (BL) is programmable in the Mode Register Bits [2:0] and controls the number of bits that will be Output after a Read Command or being Input after a Write Command.

The Burst Operation Mode can be normal (Read and Write Cycles both are operated until the selected Burst Length is worked through) or Multiple Burst with Single Write Operation.

Table 8 - Burst Length and Sequence (Burst Type)

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
2	XX0	0, 1	0, 1
	XX1	1, 0	1, 0
4	X00	0, 1, 2, 3	0, 1, 2, 3
	X01	1, 2, 3, 0	1, 0, 3, 2
	X10	2, 3, 0, 1	2, 3, 0, 1
	X11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
256 (Full Page)	n	Cn, Cn+1, Cn+2...	1, 0, 3, 2

4 | Truth Tables

The truth tables in this chapter summarize the commands and the signal coding to control the SDRAM.

Table 9 - Command Truth Table

Function	Device State	CKE		CS	RAS	CAS	WE	DQM	BA0 BA1	A10	A12 A11 A[9:0]	Note ^{1 2 3}
		Previous Cycle	Current Cycle									
Mode Register Set	Idle	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	Idle	H	H	L	L	L	H	X	X	X	X	
Self-Refresh Entry	Idle	H	L	L	L	L	H	X	X	X	X	
Self-Refresh Exit	Idle (Self-Refresh)	L	H	H	X	X	X	X	X	X	X	
				L	H	H	H					
Single Bank Precharge	Re. Current State Table	H	X	L	L	H	L	X	BS	L	X	4
Precharge all Banks	Re. Current State Table	H	X	L	L	H	L	X	X	H	X	
Bank Activate	Idle	H	X	L	L	H	H	X	BS	Row Address		
Write	Active	H	X	L	H	L	L	X	BS	L	Column	4
Write with Auto-Precharge	Active	H	X	L	H	L	L	X	BS	H	Column	4
Read	Active	H	X	L	H	L	H	X	BS	L	Column	4
Read with Auto-Precharge	Active	H	X	L	H	L	H	X	BS	H	Column	4
Burst Stop	Active	H	X	L	H	H	L	X	X	X	X	
No Operation	Any	H	X	L	H	H	H	X	X	X	X	
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	5
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	5
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X	6
Data Write/Output Disable	Active	H	X	X	X	X	X	H	X	X	X	6
Power Down Entry	Idle/Active	H	L	H	X	X	X	X	X	X	X	7,8
				L	H	H	H					
Power Down Exit	Any(Power Down)	L	H	H	X	X	X	X	X	X	X	7,8
				L	H	H	H					

¹ All SDRAM Operations are defined by states of CS, WE, RAS, CAS, and CKE at the rising edge of the clock.

² "X" means H or L (but a defined logic level).

³ Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

⁴ Bank addresses BA[1:0] determine which bank is to be operated upon

⁵ In normal access mode, CKE is held high and CK is enabled. When CKE is low it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.

- 6 DQM has two functions for the data DQ Read and Write operations. During a Read Cycle when DQM goes high during a clock timing the data outputs are disabled and become high impedance after a two-clock delay. During Write Cycles when activated the Write operation at the clock cycle is prohibited (zero clock latency).
- 7 All banks must be precharged before entering Power Down Mode. If this command is issued during a Burst operation, the device state will be Clock Suspend Mode. The Power Down Mode does not perform any Refresh operations therefore the device can not remain in this mode longer than the Refresh period (t_{REF}) duration. One clock delay is required for mode entry and exit.
- 8 A No Operation or Device Deselect Command is required on the next clock edge following CKE going high.

Table 10 – Bank Selection Bits (BS) Truth Table

BA0	BA1	Bank
L	L	Bank 0
H	L	Bank 1
L	H	Bank 2
H	H	Bank 3

Table 11 - Clock Enable (CKE) Truth Table

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0, BA1	A12 - A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down Mode exit, all Banks Idle	2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L		OP Code	Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L		OP Code	Mode Register Set	
L	X	X	X	X	X	X	X	Power Down	4	
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next Cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next Cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

- For the given Current State CKE must be low in the previous Cycle.
- When CKE has a low to high transition, the Clock and other Inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CES}) must be satisfied. When exiting power down mode, a NOP command (or Device Deselected Command) is required on the first rising clock after CKE goes high (see page 26).
- The address inputs depend on the command that is issued. See the Idle State section of the current State Truth Table for more information.
- The Precharge Power Down Mode, the Self Refresh Mode, and the Mode Register Set can only entered from the all banks idle state.
- Must be a legal command as defined in the Current State Truth Table.

Table 12 – Current State Truth Table (See Note 1) Part 1/3

Current State	Command							Action	Notes
	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0, BA1	A12- A0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	2
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	2,3
	L	L	H	L	BS	X	Precharge	No Operation	
	L	L	H	H	BS	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BS	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BS	Column	Read w/o Precharge	ILLEGAL	4
	L	H	H	L	X	X	Burst Stop	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation	
Row Active	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	5
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Precharge	6
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto Precharge	7,8
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto Precharge	7,8
	L	H	H	L	X	X	Burst Stop	ILLEGAL	
Read	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start Write Cycle	8,9
	L	H	L	H	BS	Column	Read	Terminate Burst; Start a new Read Cycle	8,9
Write	L	H	H	L	X	X	Burst Stop	Burst Stop	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Terminate Burst; Start a new Write Cycle	8,9
L	H	L	H	BS	Column	Read	Terminate Burst; Start the Read Cycle	8,9	
L	H	H	L	X	X	Burst Stop	Burst Stop		
L	H	H	H	X	X	No Operation	Continue the Burst		
H	X	X	X	X	X	Device Deselect	Continue the Burst		

Table 12 – Current State Truth Table Part 2/3

Current State	Command						Action	Notes
	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0, BA1	A12- A0		
Read with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL
	L	L	H	L	BS	X	Precharge	ILLEGAL 4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL 4
	L	H	L	L	BS	Column	Write	ILLEGAL 4
	L	H	L	H	BS	Column	Read	ILLEGAL 4
	L	H	H	L	X	X	Burst Stop	ILLEGAL
	L	H	H	H	X	X	No Operation	Continue the Burst
	H	X	X	X	X	X	Device Deselect	Continue the Burst
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL
	L	L	H	L	BS	X	Precharge	ILLEGAL 4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL 4
	L	H	L	L	BS	Column	Write	ILLEGAL 4
	L	H	L	H	BS	Column	Read	ILLEGAL 4
	L	H	H	L	X	X	Burst Stop	ILLEGAL
	L	H	H	H	X	X	No Operation	Continue the Burst
	H	X	X	X	X	X	Device Deselect	Continue the Burst
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL
	L	L	H	L	BS	X	Precharge	No Operation; Bank(s) idle after t_{RP}
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL 4
	L	H	L	L	BS	Column	Write	ILLEGAL 4
	L	H	L	H	BS	Column	Read	ILLEGAL 4
	L	H	H	L	X	X	Burst Stop	ILLEGAL
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL
	L	L	H	L	BS	X	Precharge	ILLEGAL 4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL 4, 10
	L	H	L	L	BS	Column	Write	ILLEGAL 4
	L	H	L	H	BS	Column	Read	ILLEGAL 4
	L	H	H	L	X	X	Burst Stop	ILLEGAL
	L	H	H	H	X	X	No Operation	No Operation; Row Active after t_{RCD}
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after t_{RCD}

Table 12 – Current State Truth Table Part 3/3

Current State	Command							Action	Notes
	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0, BA1	A12- A0	Description		
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	Start Write; Determine if Auto Precharge	9
	L	H	L	H	BS	Column	Read	Start Read; Determine if Auto Precharge	9
	L	H	H	H	X	X	No Operation	No Operation; Row Active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row Active after t_{DPL}	
Write Recovering with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	4
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BS	Column	Write	ILLEGAL	4,9
	L	H	L	H	BS	Column	Read	ILLEGAL	4,9
	L	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after t_{DPL}	
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after t_{RC}	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	BS	X	Precharge	ILLEGAL	
	L	L	H	H	BS	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BS	Column	Write	ILLEGAL	
	L	H	L	H	BS	Column	Read	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

Legend of the Current State Truth Table (Part 1 to 3)

1. CKE is assumed to be active (high) in the previous cycle for all entries.
The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto (CBR) Refresh Operation, if CKE is inactive (low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal.
If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The \overline{RAS} to \overline{CAS} Delay (t_{RCD}) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time (t_{RBD}) is not satisfied

5 | Electrical Characteristics

This chapter describes the Electrical Characteristics.

5.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device at any time.

Table 13 - Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.3	+4.6	V	
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.3	+4.6	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3	$V_{DD} + 0.3$	V	
P_D	Power Dissipation	-	+1.0	W	
T_{STG}	Storage Temperature	-55	+125	°C	1

¹ Storage Temperature is the ambient (case surface) temperature (on the center/top side) of the DRAM

Attention:

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 14 - DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_A	Operating Temperature for standard product	0	+70	°C	1 2 3
T_A	Operating Temperature for Industrial Temperature product	-40	+85	°C	1 2 3

¹ Operating Temperature is the ambient temperature around the DRAM.

² The Operating Temperature ranges are the temperatures where all DRAM specification will be supported.

³ During operation, the temperature must be maintained under all other specification parameters.

5.2 DC Characteristics

Table 15 - Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
V _{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V _{DDQ}	Supply Voltage for Output	3.0	3.3	3.6	V	1
V _{IH}	Input High Voltage	2.0	--	V _{DD} + 0.3	V	12
V _{TT}	Termination Voltage	-0.3	--	0.8	V	13

- ¹ All Voltages are referenced to V_{SS} and V_{SSQ}
- ² V_{IH} (max) = V_{DD} + 1.2V for pulse width ≤ 5ns
- ³ V_{IL} (min) = V_{SS} + 1.2V for pulse width ≤ 5ns

Table 16 - Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Unit	Note
I _{IL}	Input Leakage Current; any input 0 V < V _{IN} < V _{DD}	-2	+2	μA	1, 2
I _{OL}	Output Leakage Current; 0 V < V _{OUT} < V _{DDQ}	-2	+2	μA	2

- ¹ All other pins not under test = 0 V
- ² V_{DD} = 3.3V ± 0.3V

Table 17 – DC Logic Output Levels

Symbol	Parameter / Condition	Min.	Max.	Unit	Note
V _{OH}	Output Level (LVTTTL); Output "H" Voltage Level	2.4	-	V	1
V _{OL}	Output Level (LVTTTL); Output "L" Voltage Level	-	0.4	V	2

- ¹ I_{out} = -2.0mA
- ² I_{out} = +2.0mA

5.3 Operating-, Standby- and Refresh Currents

Table 18 – Operating-, Standby- and Refresh Currents

Symbol	Parameter	Test Condition	-7/-7A (133MHz)	Unit	Note
			Max.		
I _{CC1}	Operating Current	1 bank operation ¹ t _{RC} = t _{RC(min)} , t _{CK} = min	130	mA	23
I _{CC2P}	Precharge Standby Current in Power Down Mode	CKE ≤ V _{IL(max)} , t _{CK} = min, C _S = V _{IH(min)}	7	mA	
I _{CC2PS}		CKE ≤ V _{IL(max)} , t _{CK} = ∞, C _S = V _{IH(min)}	5	mA	
I _{CC2N}	Precharge Standby Current in Non-Power Down Mode	CKE ≥ V _{IH(min)} , t _{CK} = min, C _S = V _{IH(min)}	58	mA	4
I _{CC3N}	No Operating Current (Active State 4bank)	CKE ≥ V _{IH(min)} , t _{CK} = min, C _S = V _{IH(min)}	75	mA	4
I _{CC3P}		CKE ≤ V _{IL(max)} , t _{CK} = min	10	mA	5
I _{CC3NS}		CKE ≥ V _{IL(min)} , t _{CK} = ∞	49	mA	7
I _{CC4}	Operating Current (Burst Mode)	t _{CK} = min, Rea/Write command cycling, Multiple banks active, gapless data, BL=4	120	mA	3 6
I _{CC5}	Auto (CBR) Refresh Current	t _{CK} = min, t _{RC} = t _{RC(min)} , CBR command Cycling	270	mA	
I _{CC6N}	Self Refresh Current	CKE ≤ 0.2V	5	mA	

- ¹ Active-Precharge command cycling without Burst Operation.
- ² These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC(min)}.
- ³ The specified values are obtained with the output open.
- ⁴ Input signals are changed once during three clock cycles.
- ⁵ Active Standby Current will be higher if Clock Suspend is entered during a Burst Read Cycle (add 1mA per DQ).
- ⁶ Input signals are changed once during t_{CK} = min
- ⁷ Input signals are stable

5.4 Input/Output Capacitance

This chapter contains the Input and the Output Capacitance.

Table 19 - Input/Output Capacitance

Symbol	Parameter	Min.	Typ	Max	Unit	Notes
CCK	Input Capacitance, CK	2.5	2.8	3.5	pF	
CI	Input Capacitance, all other Input - only pins	2.5	3.0	3.8	pF	
CIO	Input/Output Capacitance, DQn	4.0	4.5	6.5	pF	

5.5 Clock- and Clock Enable Parameters

This chapter describes the Clock- and Clock Enable Parameters.

Table 20 – Clock and Clock Enable Parameters

Speed Grade		-7 / -7I		-7A / -7AI		Unit	Note
Symbol	Parameter	Min.	Max.	Min.	Max.		
t _{CK3}	Clock Cycle Time, CAS Latency = 3	7.5	1000	7	1000	ns	
t _{CK2}	Clock Cycle Time, CAS Latency = 2	10	1000	7.5	1000	ns	
t _{AC3}	Clock Access Time, CAS Latency = 3	—	5.4	—	5.4	ns	¹
t _{AC2}	Clock Access Time, CAS Latency = 2	—	6	—	5.4	ns	¹
t _{CKH}	Clock High Pulse Width	2.5	—	2.5	—	ns	
t _{CKL}	Clock Low Pulse Width	2.5	—	2.5	—	ns	
t _{CES}	Clock Enable Set-up Time	1.5	—	1.5	—	ns	
t _{CEH}	Clock Enable Hold Time	0.8	—	0.8	—	ns	
t _{SB}	Power Down Mode Entry Time	0	7.5	0	7.5	ns	
t _T	Transition Time (Rise and Fall)	0.5	10	0.5	10	ns	

¹ Access time is measured at 1.4V

5.6 Common Parameters

This chapter describes the Common Parameters.

Table 21 – Common Parameters

Speed Grade		-7 / -7I		-7A / -7AI		Unit	Note
Symbol	Parameter	Min.	Max.	Min.	Max.		
t _{CS}	Command Setup Time	1.5	—	1.5	—	ns	
t _{CH}	Command Hold Time	0.8	—	0.8	—	ns	
t _{AS}	Address and Bank Select Set-up Time	1.5	—	1.5	—	ns	
t _{AH}	Address and Bank Select Hold Time	0.8	—	0.8	—	ns	
t _{RC}	Bank Cycle Time	66	—	60	—	ns	¹
t _{RAS}	Active Command Period	45	100K	37	100K	ns	¹
t _{RP}	Precharge Time	20	—	15	—	ns	¹
t _{RRD}	Bank to Bank Delay Time	15	—	14	—	ns	¹
t _{CCD}	CAS to CAS Delay Time	1	—	1	—	CK	

¹ The Parameters account for the number of Clock Cycle and depend on the operating frequency of the clock as follows:
 Number of Clock Cycles = specified value of timing / clock period (fractions are counted as whole numbers).

6 | AC Timing Parameters

Table 22 – Mode Register Set Cycle

Speed Grade		-7 / -7I		-7A / -7AI		Unit	Note
Symbol	Parameter	Min.	Max.	Min.	Max.		
t _{RSC}	Mode Register Set Cycle Time	15	—	15	—	ns	

Table 23 – Refresh Cycle

Speed Grade		-7 / -7I		-7A / -7AI		Unit	Note
Symbol	Parameter	Min.	Max.	Min.	Max.		
t _{REF}	Refresh Period	—	64	—	64	ms	¹
t _{SREX}	Self Refresh Exit Time	1	—	1	—	CK	

¹ 8192 auto refresh cycles

Table 24 – Read Cycle

Speed Grade		-7 / -7I		-7A / -7AI		Unit	Note	
Symbol	Parameter	Min.	Max.	Min.	Max.			
t _{OH}	Data Out Hold Time	—	—	—	—	ns		
		2.7	—	2.7	—	ns	¹	
t _{LZ}	Data Out to Low Impedance Time	1	—	1	—	ns		
t _{HZ(3)}	Data Out to High Impedance Time	CL = 3	—	5.4	—	5.4	ns	²
t _{HZ(2)}	Data Out to High Impedance Time	CL = 2	—	6	—	5.4		
t _{DQZ}	DQM Data Out Disable Latency	2	—	2	—	CK		

¹ Data Out Hold Time with no load must meet 1.8ns

² Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels

Table 25 – Write Cycle

Speed Grade		-7 / -7I		-7A / -7AI		Unit	Note
Symbol	Parameter	Min.	Max.	Min.	Max.		
t _{DS}	Mode Data In Set-up Time	1.5	—	1.5	—	ns	
t _{DH}	Data In Hold Time	0.8	—	0.8	—	ns	
t _{DPL}	Data Input to Precharge	15	—	15	—	ns	
t _{WR}	Write Recovery Time	15	—	14	—	ns	
t _{DAL}	Data In to Active Delay	5	—	4	—	CK	
t _{DQW}	DQM Write Mask Latency	0	—	0	—	CK	

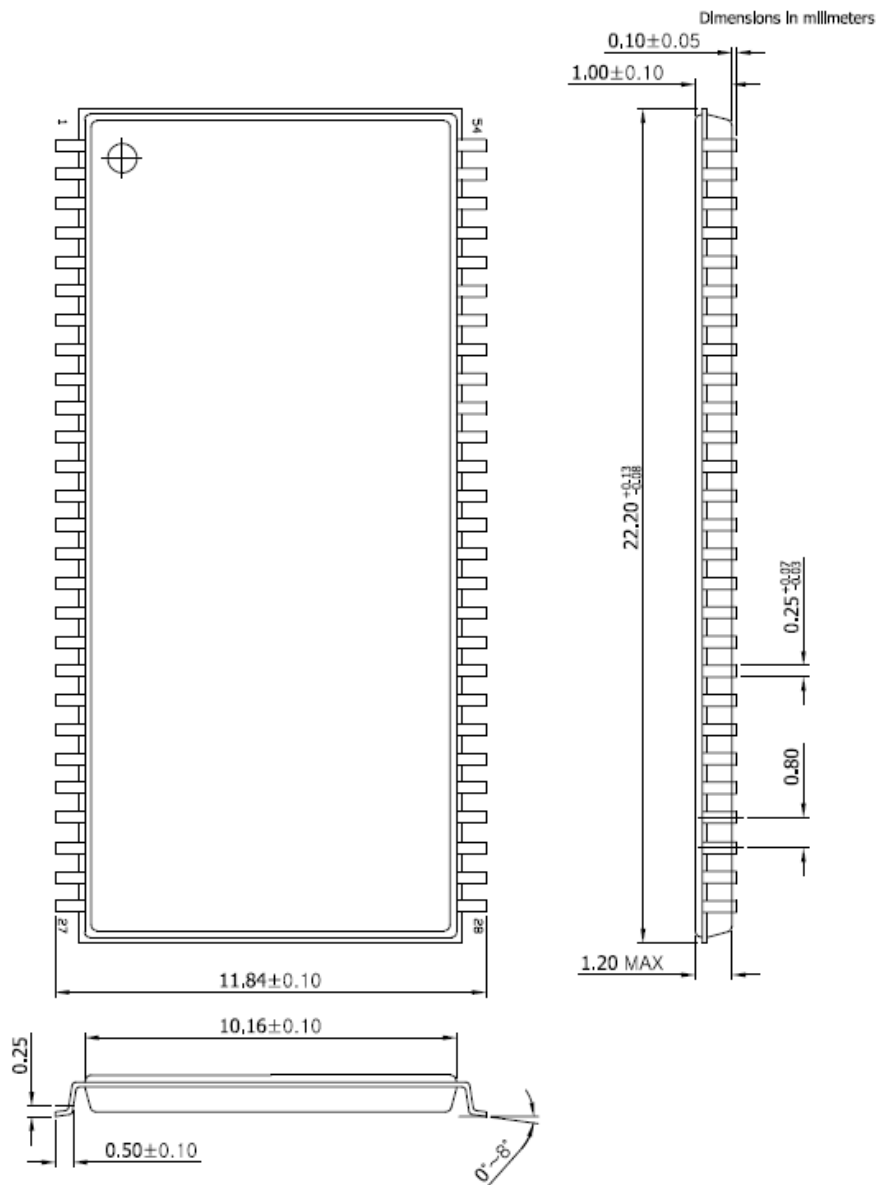
7 | Package Outline

This chapter contains the package dimension figures.

Notes

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15

Figure 3 - Package Outline 54 - Pin Plastic TSOP (400mil)



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