Ordering number : EN7815A

LA6261

Monolithic Linear IC

For Optical Disk Drive
6-Channel Driver
(BTL: 4 channels, H bridge: 2 channels)

ON Semiconductor®

http://onsemi.com

Overview

The LA6261 is a 6-channel driver IC that incorporates 4 channels of BTL output and 2 channels of H-bridge output. It is optimal for the actuator driver for CDs, MDs, and other optical disk drives.

Features

- Six power amplifier channels on a single chip (BTL: 4 channles, H-bridge: 2 channels)
- I_O max: 700mA (Each channel)
- Built-in level shifter circuits (BTL amplifier)
- Built-in thermal protection (thermal shutdown) circuit
- Separate power supply for H-bridge (2 channels)
- Onchip 3.3V regulator controller (uses an external output transistor)
- Adjustment pin for the H-bridge output

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	for each of the channel 1 to 6	0.7	A
Maximum input voltage	$V_{IN}B$		13	V
MUTE pin voltage	V_{MUTE}		13	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Mounted on the specified board *	2	W
Operating ambient temperature	Topr		-30 to +85	°C
Storage ambient temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 76.1mm×114.1mm×1.6mm, glass epoxy.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

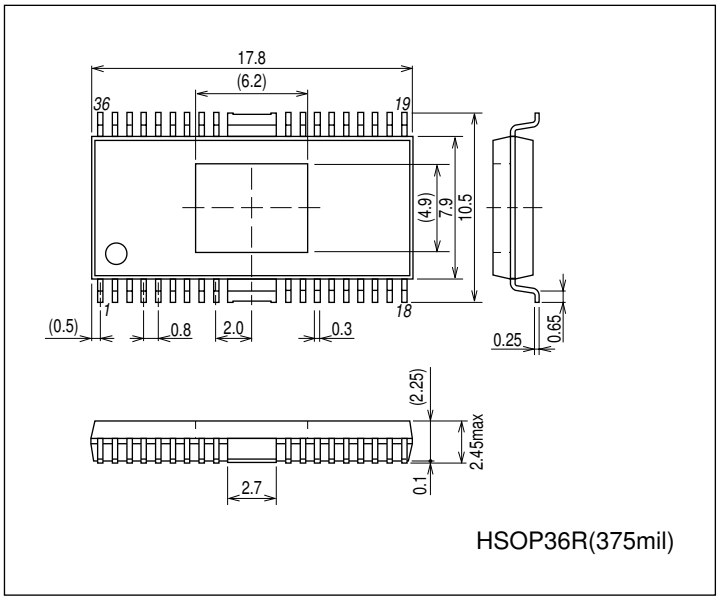
Electrical Characteristics at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8V$, $V_{REF} = 1.65V$

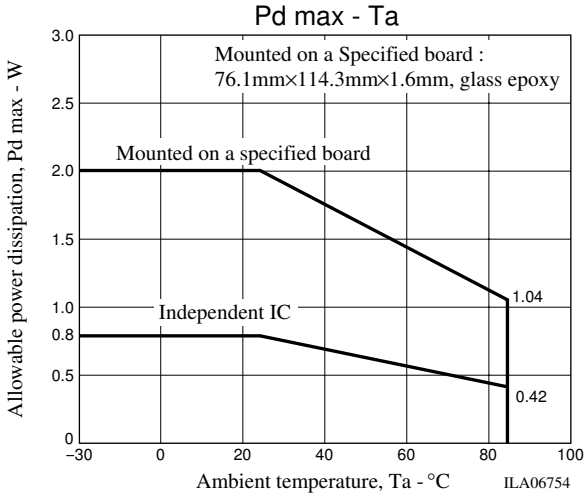
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All Blocks						
No-load current drain ON	I_{CC}-ON	All outputs on *1, FWD=REV=0V		30	50	mA
V_{REF} input voltage range	V_{REF}-IN		0.5		V_{CC}-1.5	V
BTL AMP						
Output offset voltage	V_{OFF}	BTL amplifier, the voltage difference between each channel outputs	-50		+50	mV
Input voltage range	V_{IN}	Applied to pins $V_{IN}1$ to $V_{IN}4$	0		V_{CC}	V
Output voltage	V_O	Voltage between V_O+ and V_O- for each channel when R_L=8Ω *2	4	5		V
Closed-circuit voltage gain	V_G	The gain from the input to the output		4		deg
MUTE ON voltage	V_{MT}ON	*3	2		SV_{CC}	V
MUTE OFF voltage	V_{MT}OFF	*3	0		0.5	V
Slew rate	SR	For the independent amplifier. Times 2 when between outputs *4		0.5		V/μs
H-bridge Block						
Output voltage	V_O-LOAD	Voltage between V_O+ and V_O- for each channel when R_L=10Ω	6.2	6.7		V
Input low level	V_{IN}-L		0		1	V
Input high level	V_{IN}-H		2		SV_{CC}	V
Output setting voltage	VCONT	Voltage between V_O+ and V_O- for each channel when VCONT=3V and R_L=10Ω		2.8		V
Regulator Block						
Output voltage	Vreg	I_L=100mA	3.05	3.3	3.55	V
Output load variation	ΔV_{RL}	I_L=0 to 200mA	-50	0	10	mV
Supply voltage variation	ΔVV_{CC}	V_{CC}=6 to 12V, I_L=100mA	-15	21	60	mV

*1: The total current dissipation for SV_{CC}, $PV_{CC}1$, and $PV_{CC}2$ with no load
*2: Output in the saturated state
*3: When the MUTE pin is high, the BTL output will be on, and when low, the BTL output will be OFF (HI impedance).
*4: Design guarantee value

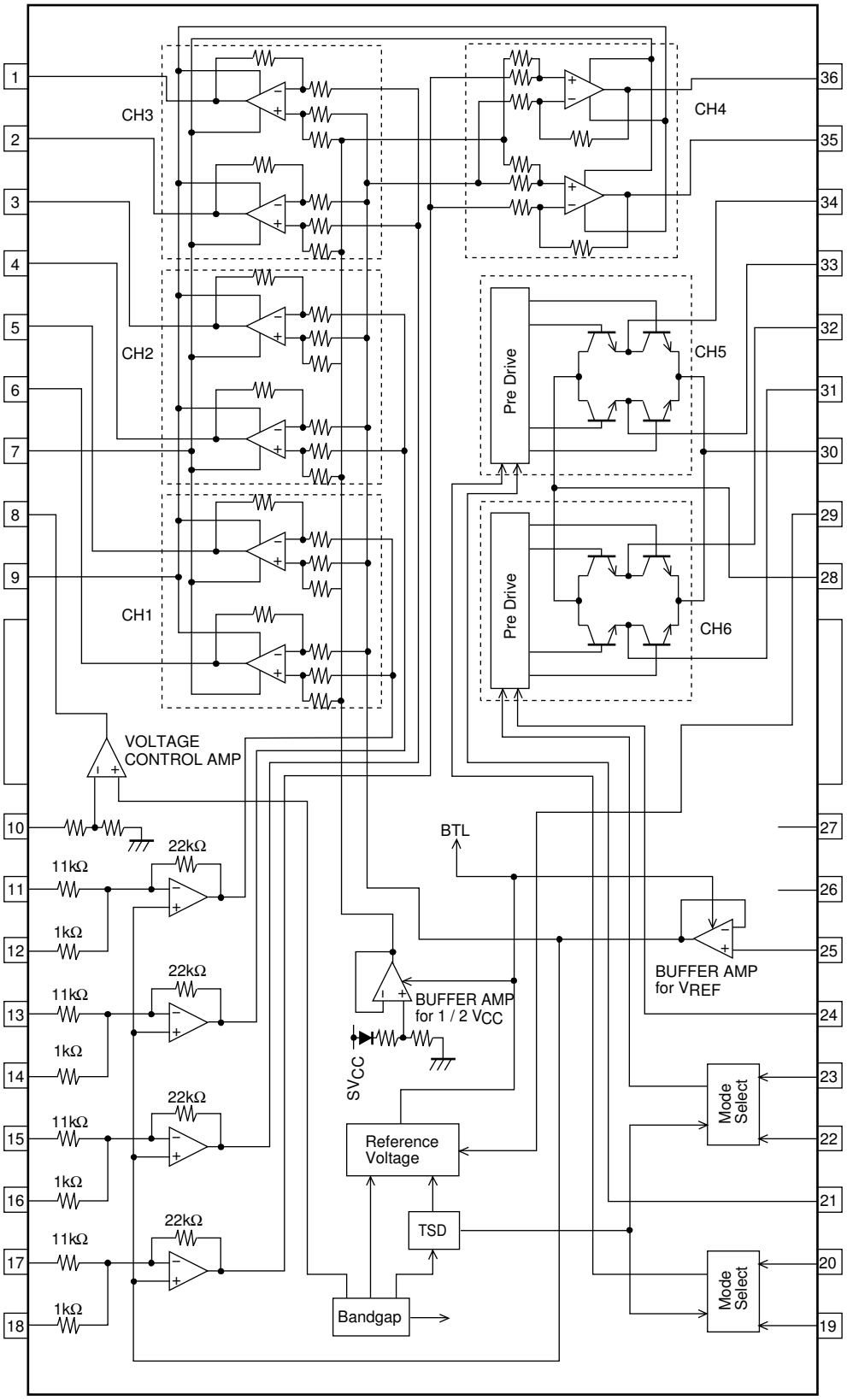
Package Dimensions

unit : mm (typ)
3251



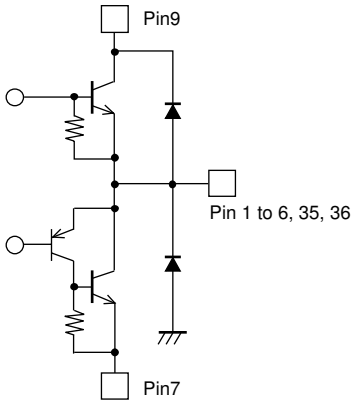
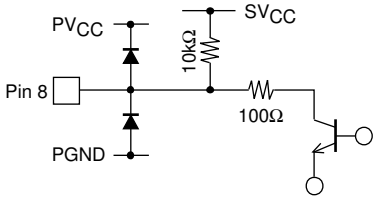
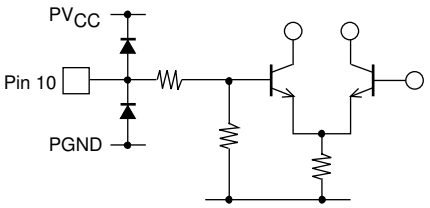
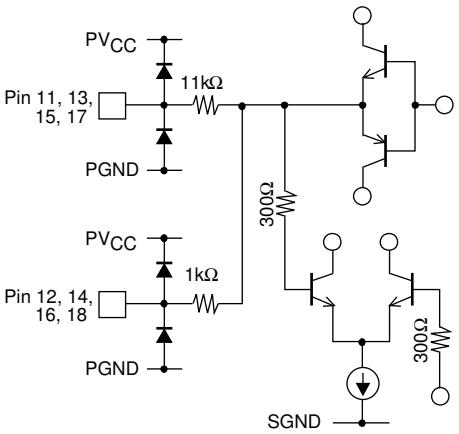
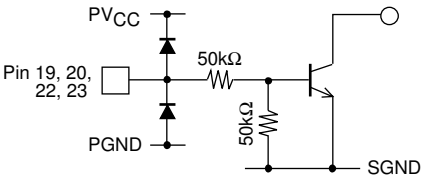


Block Diagram



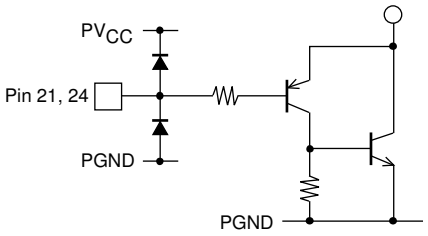
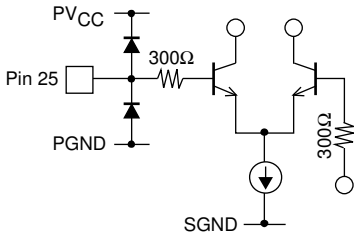
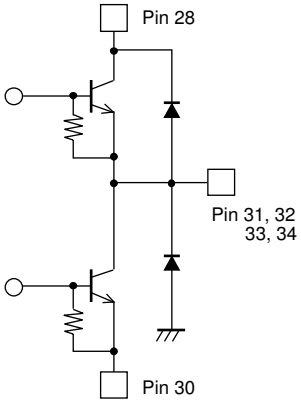
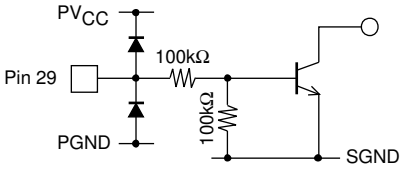
ILA06744

Pin Description

Pin No.	Pin Name	Description	Equivalent Circuit Diagram
1	V_O3+	Channel 3 (BTL) output (+)	
2	V_O3-	Channel 3 (BTL) output (-)	
3	V_O2+	Channel 2 (BTL) output (+)	
4	V_O2-	Channel 2 (BTL) output (-)	
5	V_O1+	Channel 1 (BTL) output (+)	
6	V_O1-	Channel 1 (BTL) output (-)	
7	PGND	Power system ground for channels 1 to 4 (BTL)	
9	$PV_{CC}1$	Power system power supply for channels 1 to 4 (BTL) (shorted to SV_{CC})	
35	V_O4+	Channel 4 (BTL) output (+)	
36	V_O4-	Channel 4 (BTL) output (-)	
8	REGIN	Regulator (to the base of the external PNP transistor)	
10	REGOUT	Regulator (to the collector of the external PNP transistor)	
11	$V_{IN}1$	Channel 1 input	
12	$V_{IN}1G$	Channel 1 input (gain adjustment)	
13	$V_{IN}2$	Channel 2 input	
14	$V_{IN}2G$	Channel 2 input (gain adjustment)	
15	$V_{IN}3$	Channel 3 input	
16	$V_{IN}3G$	Channel 3 input (gain adjustment)	
17	$V_{IN}4$	Channel 4 input	
18	$V_{IN}4G$	Channel 4 input (gain adjustment)	
19	FWD5	Channel 5 output direction switching (FWD), H-bridge logic input	
20	REV5	Channel 5 output direction switching (REV), H-bridge logic input	
22	FWD6	Channel 6 output direction switching (FWD), H-bridge logic input	
23	REV6	Channel 6 output direction switching (REV), H-bridge logic input	

Continued on next page.

Continued from preceding page.

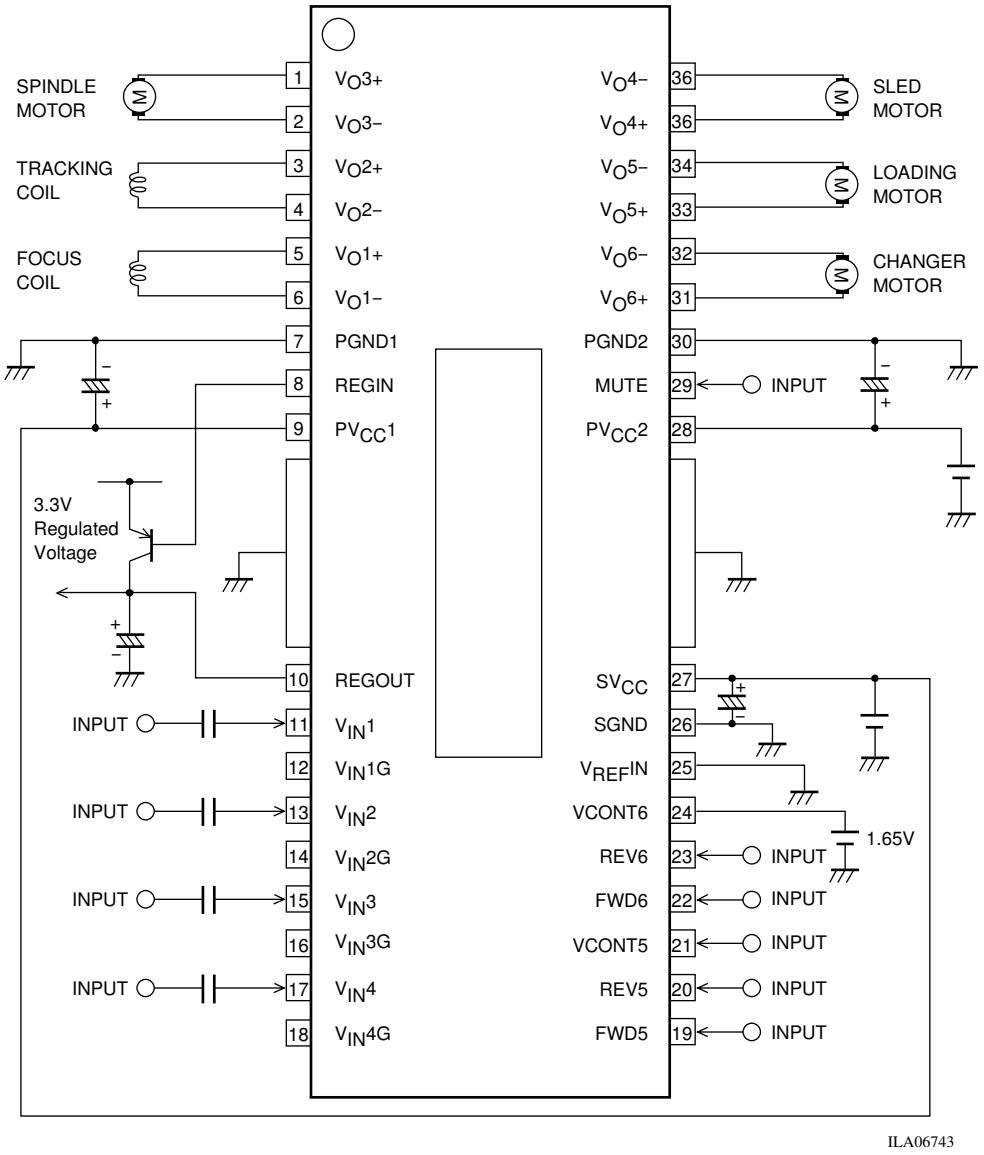
Pin No.	Pin Name	Description	Equivalent Circuit Diagram
21 24	VCONT5 VCONT6	Channel 5 output voltage setting Channel 6 output voltage setting	
25	V_{REF}IN	Reference voltage input	
28 30 31 32 33 34	PV_{CC}2 PGND2 V_O6+ V_O6- V_O5+ V_O5-	Power system power supply for for channels 5 and 6 (H-bridge) Power system ground for channels 5 and 6 (H-bridge) Channel 6 (H-bridge) output (+) Channel 6 (H-bridge) output (-) Channel 5 (H-bridge) output (+) Channel 5 (H-bridge) output (-)	
29	MUTE	BTL mute signal input	
26	SGND	Signal system ground	
27	SV_{CC}	Signal system power supply (shorted to PV_{CC}1)	

Truth Table

INPUT		OUTPUT	
FWD5(6)	REV5(6)	V_O5(6)+	V_O5(6)-
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	L	L

*Z: HI-Impedance

Sample Application Circuit



ILA06743