LA6565



http://onsemi.com

Monolithic Linear IC For CD and DVD players 5-channel Driver (BTL:4ch,H-bridge:1ch)

Overview

The LA6565 is a 4-channel BTL plus 1-channel H-bridge actuator driver developed for use in CD and DVD drives. The BTL driver channels 1 and 2 include built-in operational amplifiers allowing the LA6565 to support a wide range of applications.

Functions

- Five power amplifier channels on a single chip (Bridge connection (BTL): 4-channels, H-bridge: 1-channel)
- IO max: 1A
- Built-in level shifters (except for the H bridge channel)
- Muting circuits (output on/off, two systems)
 (The muting circuits operate for the BTL amplifiers. They do not apply to the H-bridge or regulator circuits.)
- Built-in regulator (Uses an external PNP-transistor and is set with an external resistor.)
- Output voltage setting function (loading driver)
- Built-in independent operational amplifiers
- Thermal shutdown circuit

Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		14	V
Maximum output current	I _O max		1	Α
Maximum input voltage	V _{INB}		13	V
MUTE pin voltage	V _{MUTE}		13	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Mounted on a specified board *	2	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

^{*} Specified board: 114.3mm \times 76.1mm \times 1.6mm, glass epoxy board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc		5.6 to 13	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8V$, $V_{REF} = 2.5V$

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Parameter	Symbol Conditions			Ratings		
	-		min	typ	max	
Overall	T	<u> </u>				
Quiescent current when o	I _{CC} -ON	BTL amplifier output on, loading block off *1		30	50	mA
Quiescent current when off	I _{CC} -OFF	All outputs off *1		10	15	mA
Thermal shutdown circuit	TSD	*7	150	175	200	°C
vref Amplifier						
VREF amplifier offset voltage	VREF-OFFSET		-10		+10	mV
VREF input voltage range	VREF-IN		1		V _{CC} -1.5	V
VREF-OUT output current	I-VREF-OUT		'	1	VCC-1.5	mA
•						IIIA
Operational Amplifier (Indep	· · · · · · · · · · · · · · · · · · ·				V 45	
Input voltage range	V _{IN} (OP)		0		V _{CC} -1.5	V
Output current (sink)	SINK(OP)		2			mA
Output current (source)	SOURCE(OP)		300	500		μA
Output offset voltage	V _{OFF} (OP)		-10		+10	mV
Residual current (sink)	V _{CE} -SINK(OP)	I _O (sink side) = 1mA			0.6	V
BTL Amplifier Block (Channe	els 1 to 4)				ı	
Output offset voltage	VOFF	The voltage difference between each channel outputs *2, *3	-50		+50	mV
Input voltage range	V _{IN}	Input voltage range of the input operational amplifiers			V _{CC} -1.5	٧
Output voltage	V _O	$I_O = 0.5A$, the voltage between V_O^+ and V_O^- in each channel	5.7	6.2		٧
Closed circuit voltage gain	VG	The gain from the input to the output with the input amplifier set to 0dB*2, *3	7.2	8	9	times
Slew rate SR	SR	For the independent amplifier. Times 2 when between outputs.*7		0.5		V/µs
Muting on voltage	V _{MUTE} -ON	The output on voltage, for each mute function *4	2.5			V
Muting off voltage	V _{MUTE} -OFF	The output off voltage, for each mute function *4			0.5	V
Input Amplifier Block (Chann						
Input voltage range	V _{IN} -OP				V _{CC} -1.5	V
Output current (sink)	SINK-OP		2		- 00	mA
Output current (source)	SOURCE-OP	*5	300	500		μΑ
Output offset voltage	V _{OFF} -OP		-10		+10	mV
Loading Block (Channel 5, H					<u>l</u>	1
Output voltage	V _O -LOAD	For forward/reverse operation, $I_O = 0.5A$, VCONT = V_{CC}^*	5.7	6.5		V
Braking output saturation voltage	V _{CE} -BREAK	The output voltage during braking *6			0.3	V
Low-level input voltage	V _{IN} -L				1	V
High-level input voltage	V _{IN-} H		2		-	V
Power Supply Block (Uses a	1	⟨ PNP-transistor)	_			<u> </u>
Power supply output	VOUT	I _O = 200mA	1.260	1.285	1.310	V
REG-IN sink current	REG-IN-SINK	External PNP-transistor base current	5	1.203	1.510	mA
			<u> </u>		100	
Line regulation	ΔV _O LN	$6V \le V_{CC} \le 12V, I_{O} = 200 \text{mA}$		10	100	mV
Load regulation	ΔV _O LD	5mA ≤ I _O ≤ 200mA		10	100	mV

^{*1:} The total current dissipation for V_{CC}P1, V_{CC}P2, and V_{CC}S with no load.

^{*2:} The input amplifier is a buffer amplifier.

^{*3:} The voltage difference between the two sides of the load (12 $\!\Omega\!$).

^{*4:} When the MUTE pin is high, the output will be on, and when low, the output will be off (high-impedance state).

^{*5:} The input operational amplifier source is constant current. Since the 11kΩ resistor between this and the next stage functions as the load, the input operational amplifier gain must be set carefully.

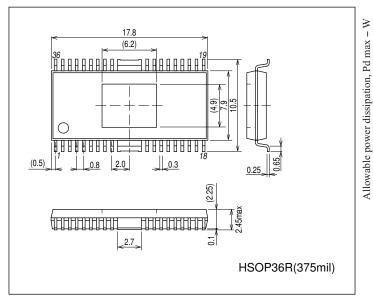
^{*6:} The braking operation is a short (to ground) braking operation. The sink side output is on at this time.

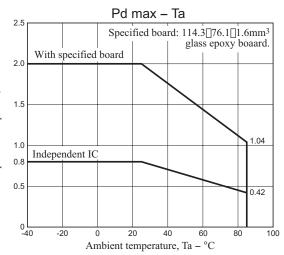
^{*7:} Design guarantee.

Package Dimensions

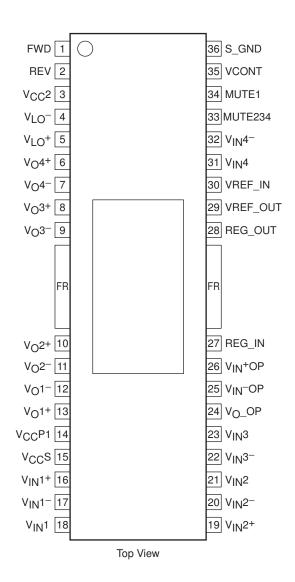
unit : mm (typ)

3251

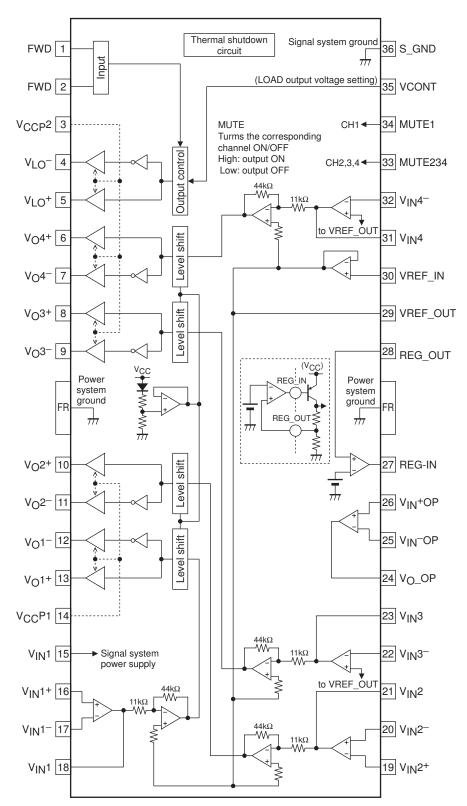




Pin Assignment



Block Diagram



LA6565

Pin Function

Pin No.	Pin name	Pin function			
1	FWD	Loading output direction switching (FWD). Loading system logic input.			
2	REV	Loading output direction switching (REV). Loading system logic input.			
3	V _{CC} ²	Channels 3, 4, and loading power stage power supply.			
4	V _{LO} -	Loading output (-)			
5	V _{LO} +	Loading output (+)			
6	V _O 4+	Channel 4 output (+)			
7	V _O 4 ⁻	Channel 4 output (–)			
8	V _O 3+	Channel 3 output (+)			
9	V _O 3-	Channel 3 output (–)			
10	V _O 2 ⁺	Channel 2 output (+)			
11	V _O 2 ⁻	Channel 2 output (–)			
12	V _O 1 ⁻	Channel 1 output (–)			
13	V _O 1+	Channel 1 output (+)			
14	V _{CC} P1	Channels 1 and 2 power stage power supply.			
15	V _{CC} S	Signal system power supply.			
16	V _{IN} 1+	Channel 1 input. Input operational amplifier + input.			
17	V _{IN} 1 ⁻	Channel 1 input. Input operational amplifier – input.			
18	V _{IN} 1	Channel 1 input. Input operational amplifier output.			
19	V _{IN} 2+	Channel 2 input. Input operational amplifier + input.			
20	V _{IN} 2-	Channel 2 input. Input operational amplifier – input.			
21	V _{IN} 2	Channel 2 input. Input operational amplifier output.			
22	V _{IN} 3-	Channel 3 input. Input operational amplifier – input.			
23	V _{IN} 3	Channel 3 input. Input operational amplifier output.			
24	V _O _OP	Operational amplifier output.			
25	V _{IN} -OP	Operational amplifier – input			
26	V _{IN} +OP	Operational amplifier + input			
27	REG_IN	Regulator error amplifier output. Connect this pin to the base of the external PNP-transistor.			
28	REG_OUT	Regulator error amplifier input (+).			
29	VREF_OUT	VREF amplifier (voltage follower) output.			
30	VREF_IN	VREF input. Apply the external reference voltage to this pin.			
31	V _{IN} 4	Channel 4 input. Input operational amplifier output.			
32	V _{IN} 4 ⁻	Channel 4 input. Input operational amplifier – input.			
33	MUTE234	Controls the on/off state of channels 2, 3, and 4.			
34	MUTE1	Channel 1 output on/off control			
35	VCONT	Loading block output high-level voltage setting.			
36	S_GND	Signal system ground.			

^{*} center frame (FR) becomes GND for the power system, Set this to the minimum potential together with S_GND (signal system ground).

Pin Description

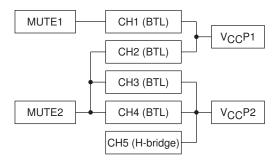
Pin No.	Pin name	Function	Description	Equivalent circuit
				Equivalent circuit
16 17	V _{IN} 1+ V _{IN} 1-	Input (CH1 to 4)	Inputs (channels 1 to 4 and the independent operational	V
18	V _{IN} 1	(CH1 (0 4)	amplifier)	V _{IN*} ()
19	V _{IN} 2+		ampinier)	V _{CC} S O
20	V _{IN} 2-			
21	V _{IN} 2			3000 - 111444 1 1 1
22	V _{IN} 3-			V _{IN*} + 300Ω 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
23	V _{IN} 3			V _{IN*} - 300Ω
32	V _{IN} 4 ⁻			VIN*-
31	V _{IN} 4			
26	V _{IN} +OP			
25	V _{IN} -OP			S-GND ()
24	V _O _OP			3-GIND 0
1 2	FWD REV	Input (H-bridge)	Logic inputs. The IC is set to one of four modes, forward, reverse, brake, and free running by the combination of high and low values applied to	EWD REV
			these pins.	S-GND
12	V _O 1+	Output	Channel 1 to 4 outputs.	- t t VccP
13	V _O 1 ⁻	(BTL-AMP)		₩ ₩ ₩
10 11	V _O 2+ V _O 2-			
8	V _O 2+			∮
9	V _O 3-			\downarrow
6	V _O 4 ⁺			
7	V _O 4 ⁻			
				— GR FR
4	V _{LO} -	Output	H-bridge (loading) output.	V _{CC} P2
5	V _{LO} +	(H-bridge)		
				ikΩ ikΩ ξ
				S_GND \$ \$ \$ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
				VCONI
35	VCONT	Input	Loading output setting.	20kΩ 20kΩ
33	MUTE234	MUTE	BTL amplifier output ON/OFF	v _{cc} s O
34	MUTE1		state setting.	
			High: output ON	MUTE* W
			Low: output OFF	Ğ\$ →w ☐ T
				[
				g
				S-GND
				3-GIND V

Truth Table (Loading (H bridge) block)

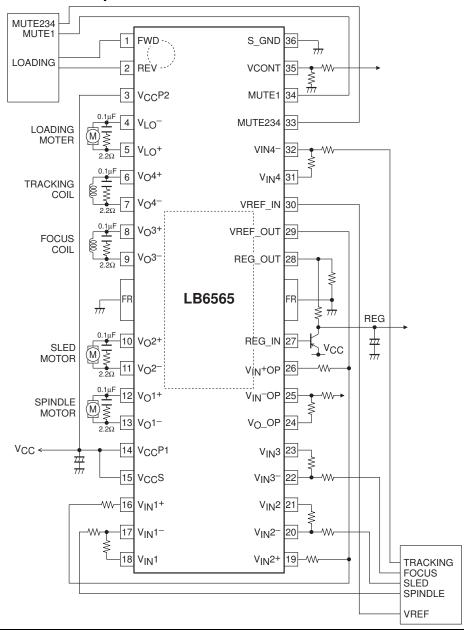
	,			<u> </u>
FWD	REV	V_{LO}^+	V_{LO}^-	Loading output
	L	OFF	OFF	OFF *1
_	Н	Н	L	Forward
Н	L	L	Н	Reverse
	Н	L	L	Short-circuit braking *2

 $^{^{\}star}$ 1. The output goes to the high-impedance state.

Relationship between the MUTE pins and the power supply systems (V_{CC}P*)



Application Circuit Example



 $^{^{\}star}2$. In braking mode, the sink side transistor is turned on (for short-circuit braking). The V_{LO}^{+} and V_{LO}^{-} pins go to a level that is essentially the ground level.

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