Ordering number : ENA1360

SANYO Semiconductors
DATA SHEET

LV5654T — Bi-CMOS IC 4-Channel Switching Regulator Controller

Overview

The LV5654T is a 4-channel switching regulator controller.

Features

- Low-voltage (3V) operation.
- Independent standby functions for each of the four channels.
- Synchronous rectification : channel 1 and channel 2.
- Reference voltage precision : ±1%.
- Is capable of driving MOS transistors.
- Supports inverting step-up operation (channel 3).

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC} max	V_{CC} pin	-0.3 to 16	V
Maximum supply voltage 2	VBVIAS max	VBIAS pin	-0.3 to 18	V
Maximum clock input voltage	VCLKIN max	CLKIN pin	5.5	V
Allowable power dissipation	Pd max	Independent IC	0.4	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}	V_{CC} pin	3 to 15	V
Supply voltage 2	VBIAS	VBIAS pin	3 to 15	V
Clock input voltage	VCLKIN	CLKIN pin	5	V
Timing resistor	RT		7 to 30	kΩ
Timing capacitor	CT		100 to 1000	pF
Triangle wave frequency	f_{OSC}		0.1 to 1.3	MHz

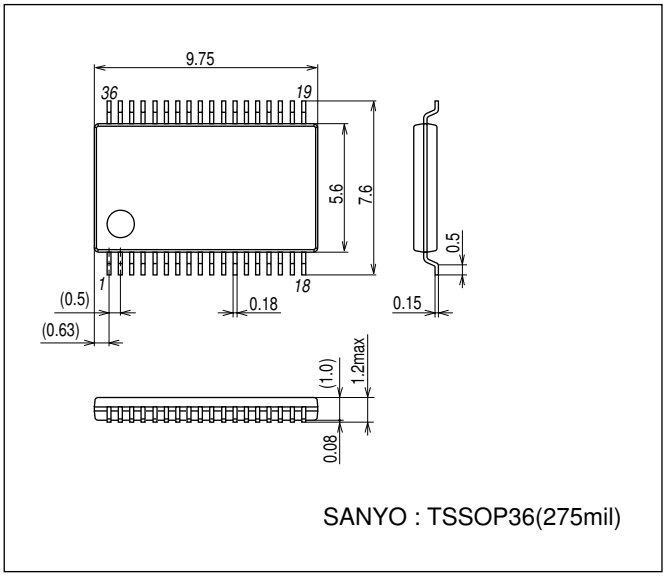
Electrical Characteristics at Ta = 25°C, V_{CC} = VBIAS = 3.6V, SCP = 0V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Error amplifier 1							
IN^+ pin internal bias voltage		VB	Value added to the error amplifier offset at the error amplifier + side voltage	0.504	0.51	0.516	V
Output low voltage	ch1 to ch4	V_{Low} FB	IN^- = 2.0V, IFB = 20μA			0.2	V
Output high voltage	ch1 to ch4	V_{Hi} FB	IN^- = 0V IFB1 = -20μA	2.0			V
Error amplifier 2							
$IN3^-RE$ pin offset voltage		VOF		-6		6	mV
Output low voltage		V_{Low} FB3RE	$IN3^-RE$ = 2.0V, IFB = 20μA			0.2	V
Output high voltage		V_{Hi} FB3RE	$IN3^-RE$ = -10mV, IFB = 500μA	2.0			V
Protection circuit							
Threshold voltage		V_{SCP}		1.1	1.25	1.4	V
SCP pin current		I_{SCP}			4		μA
Short circuit detection signal pin		VSCPOUT	Open collector ISCPOUT = 100μA			0.2	V
Software start block (ch1 to ch4)							
Soft start current	ch1 to ch4	I_{SF}	CSOFT = 0V	3.2	4	4.8	μA
Soft start resistance	ch1 to ch4	R_{SF}		160	200	240	kΩ
Fixed duty							
Maximum on duty 1-2	ch1 to ch2	Duty MAX 1-2	Out monitor, IN^- = 0V	100			%
Maximum on duty 3	ch3	Duty MAX 3	Out monitor, IN^- = 0V	80	85	90	%
Maximum on duty 4	ch4	Duty MAX 4	Out monitor, IN^- = 0V	80	85	90	%
Output block 1 to 6							
OUT pin high side on resistance		R_{OUT} SOUR	I_O = 10mA		25		Ω
OUT pin high side on resistance		R_{OUT} SINK	I_O = 10mA		10		Ω
Triangle wave oscillator block							
Current setting pin voltage		VT RT	RT = 10kΩ		0.57		V
Output current		I_{OH} CT			190		μA
Output current ratio		ΔI_O CT	CT pin, rise/fall		2.5		
Oscillation frequency		$f_{OSC}1$	RT = 10kΩ, CT = 270pF		510		kHz
Reference voltage block							
Reference voltage		VREF			1.240		V
Line regulation		V_{LN} REF	V_{CC} = 3V to 15V			10	mV
Control circuit							
On state voltage		V_{ON} CTL		2.0			V
OFF state voltage		V_{OFF} CTL				0.6	V
Pin input current		I_{IN} CTL				60	μA
Standby circuit							
On voltage		V_{ON} STBY		2.0			V
Off voltage		V_{OFF} STBY				0.6	V
Pin input current		I_{IN} STBY	VSTBY = 2V			60	μA
All circuits							
V_{CC} current consumption		I_{CC}	$IN1^-$ to $IN4^-$ = 1V		4	5	mA
Standby mode current consumption		I_{OFF}	VSTBY = VCTL = 0V $I_{OFF} = I_{CC} + I_{BIAS}$			1	μA

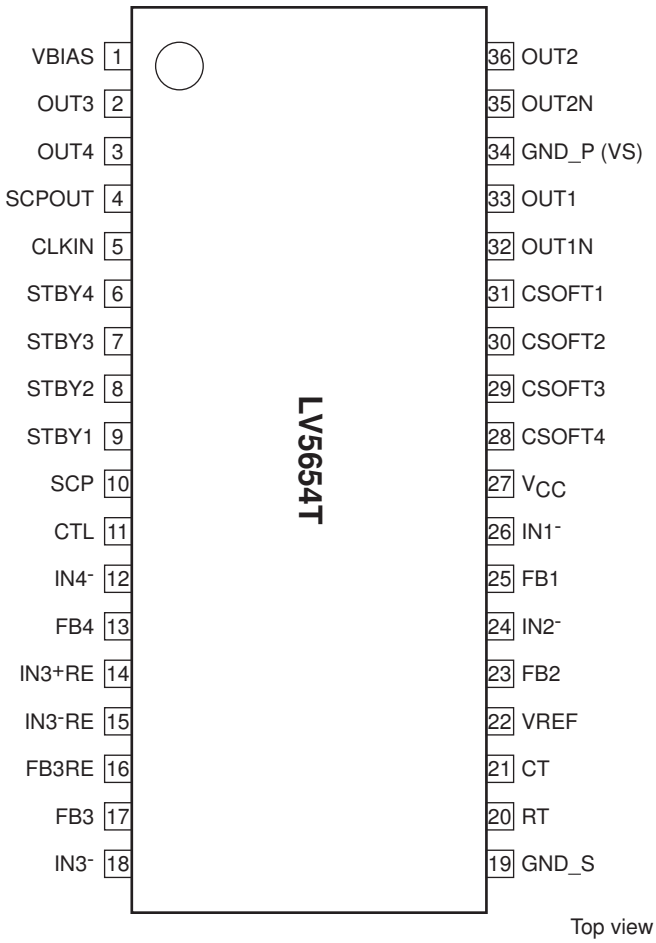
Package Dimensions

unit : mm (typ)

3253B

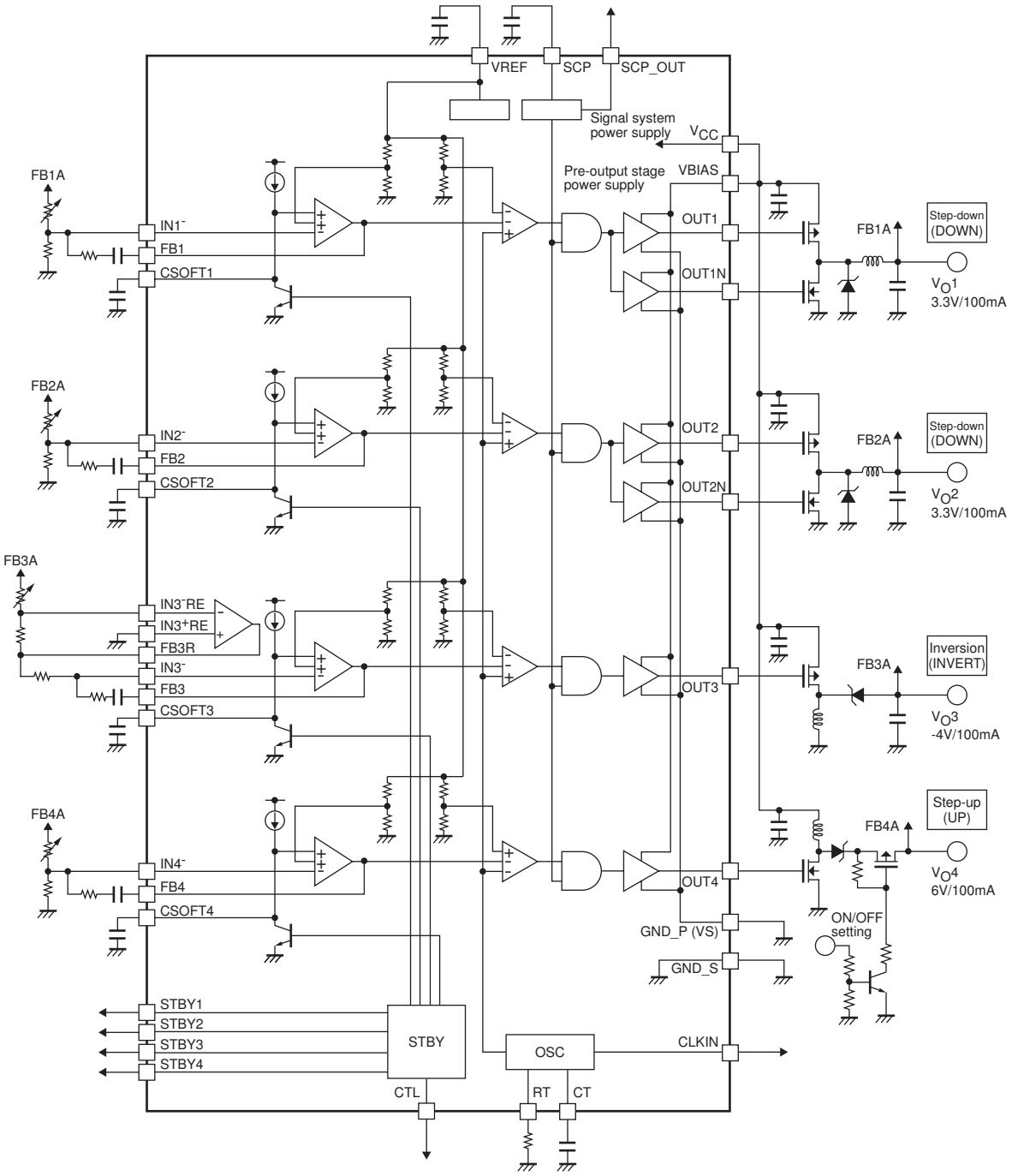


Pin Assignment



Top view

Block Diagram and Sample Application Circuit

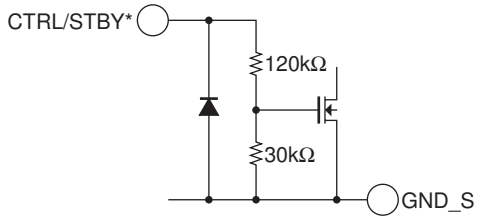
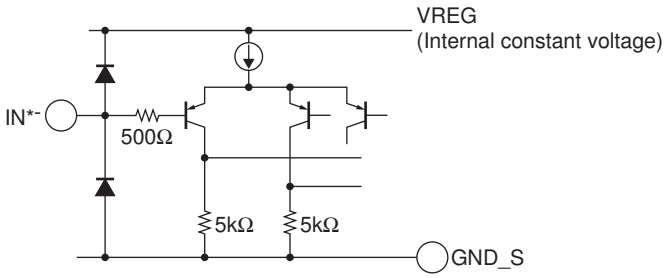
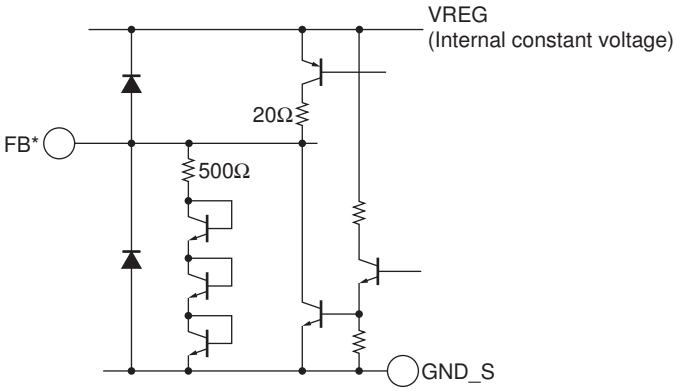
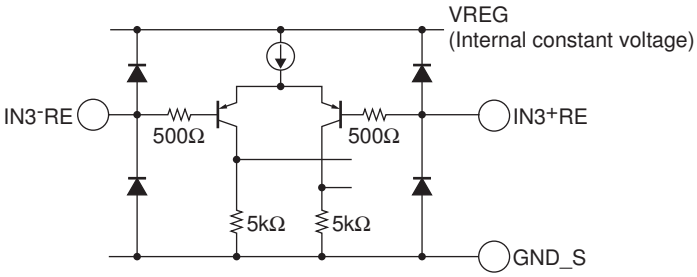
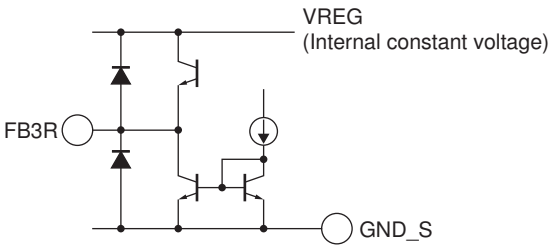
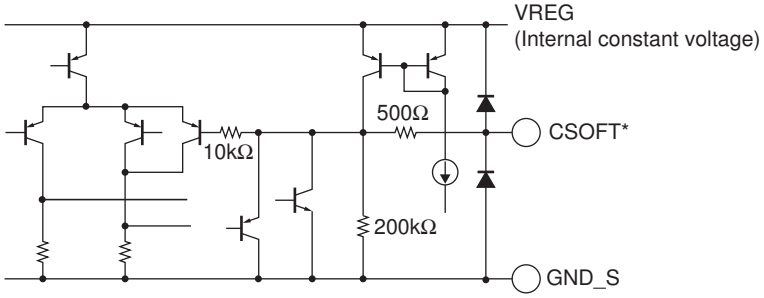


The CLKIN pin must be connected to GND, when the external clock synchronization (CLKIN) is not used.

Pin Function

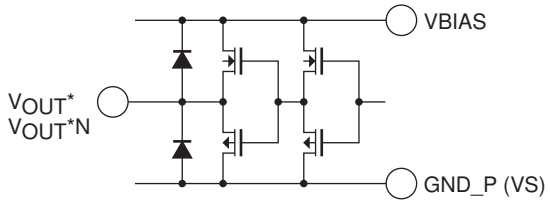
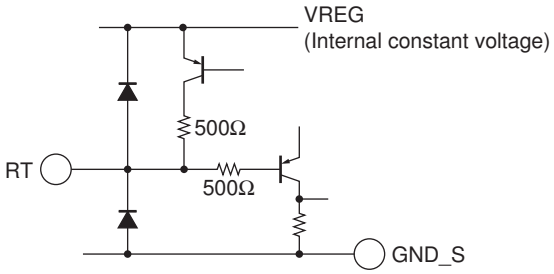
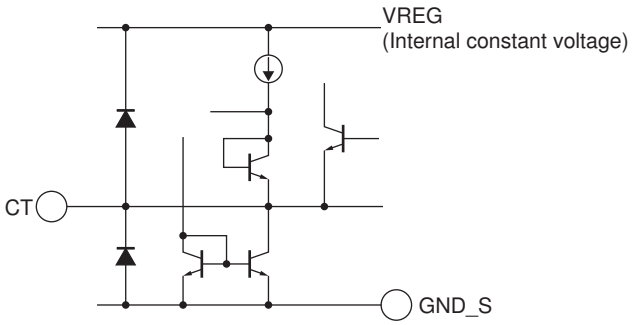
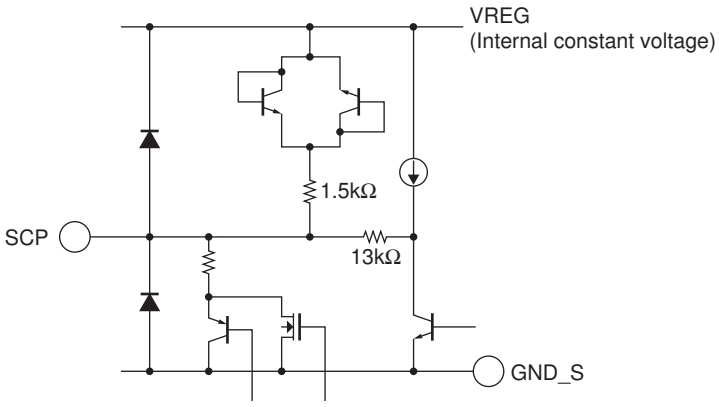
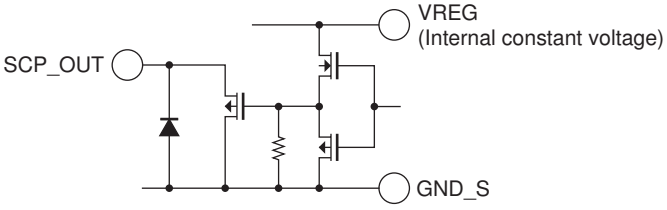
Block	Pin No.	Pin Name	Functions
ch1 DOWN (Step-down)	9	STBY1	Standby input. H/ch1 ; ON, L/ch1 ; OFF.
	26	$IN1^-$	Error amplifier Inverting input.
	25	FB1	Error amplifier output.
	31	CSOFT1	Soft start setting capacitor connection. Connect to GND through a capacitor.
	33	OUT1	Output. External transistor P-channel gate connection.
	32	OUT1N	Output. External transistor N-channel gate connection.
ch2 DOWN (Step-down)	8	STBY2	Standby input. H/ch2 ; ON, L/ch2 ; OFF.
	24	$IN2^-$	Error amplifier Inverting input.
	23	FB2	Error amplifier output.
	30	CSOFT2	Soft start setting capacitor connection. Connect to GND through a capacitor.
	36	OUT2	Output. External transistor P-channel gate connection.
	35	OUT2N	Output. External transistor N-channel gate connection.
ch3 (Inversion)	7	STBY3	Standby input. H/ch3 ; ON, L/ch3 ; OFF.
	14	$IN3^+RE$	Inversion amplifier, + (noninverting) input.
	15	$IN3^-RE$	Inversion amplifier, - (Inverting) input.
	16	FB3RE	Inversion amplifier output.
	18	$IN3^-$	Error amplifier, - (Inverting) input.
	17	FB3	Error amplifier output.
	29	CSOFT3	Soft start setting capacitor connection. Connect to GND through a capacitor.
	2	OUT3	Output. External transistor P-channel gate connection.
ch4 Step-up (UP)	6	STBY4	Standby input. H/ch4 ; ON, L/ch4 ; OFF.
	12	$IN4^-$	Error amplifier Inverting input.
	13	FB4	Error amplifier output.
	28	CSOFT4	Soft start setting capacitor connection. Connect to GND through a capacitor.
	3	OUT4	Output. External transistor N-channel gate connection.
POWER	27	V_{CC}	Power supply input (signal system).
	1	VBIAS	Power supply input (pre-output stage).
	19	GND_S	Ground (signal system).
	34	GND_P (VS)	Ground (pre-output stage).
	22	VREF	Reference voltage output.
CONTROL	11	CTL	Output control.
	10	SCP	Connection pin for the delay time setting capacitor of short circuit detection circuit.
	4	SCPOUT	SCP_OUT pin (SCP output).
OSC	21	CT	Triangle wave oscillation frequency setting capacitor connection.
	20	RT	Triangle wave oscillation frequency setting resistor connection.
	5	CLKIN	External clock input.

Equivalent Circuits

Pin No.	Pin Name	Equivalent Circuit
11 9 8 7 6	CTL STBY1 STBY2 STBY3 STBY4	
26 24 18 12	IN1⁻ IN2⁻ IN3⁻ IN4⁻	
25 23 17 13	FB1 FB2 FB3 FB4	
14 15	IN3⁺RE IN3⁻RE	
16	FB3R	
31 30 29 28	CSOFT1 CSOFT2 CSOFT3 CSOFT4	

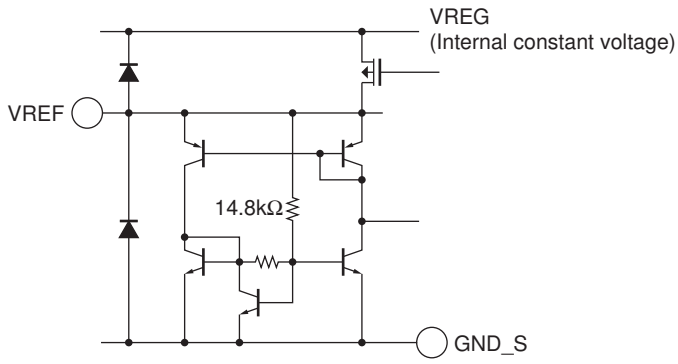
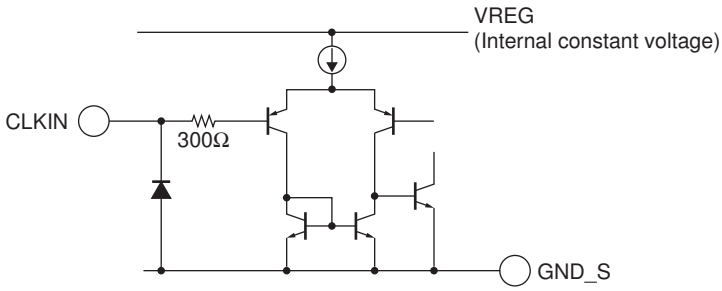
Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Equivalent Circuit
33 32 36 35 2 3	OUT1 OUT1N OUT2 OUT2N OUT3 OUT4	
20	RT	
21	CT	
10	SCP	
4	SCP_OUT	

Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Equivalent Circuit
22	VREF	
5	CLKIN	
27	V_{CC}	
1	VBIAS	
19	GND_S	
34	GND_P (VS)	

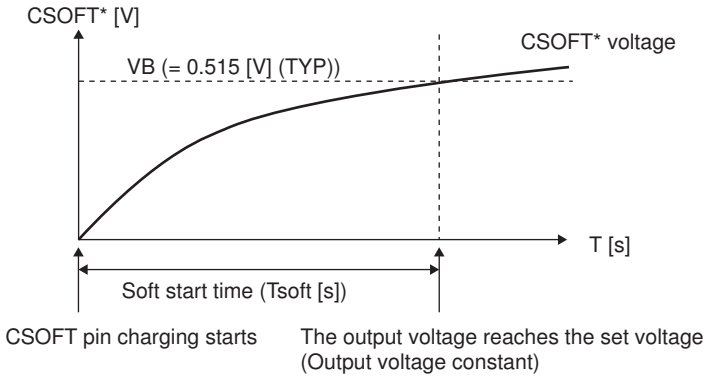
Notes

(1) Soft start time setting method

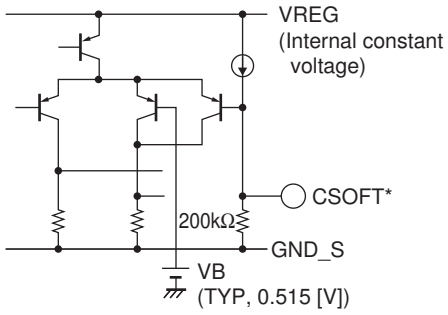
The soft start time is set with the capacitor connected between CSOFT* and GND_S.

This IC has an independent soft start function for each channel, so a capacitor must be connected for each channel to set the soft start (time).

(Description of soft start operation)



(Outline of soft start pin)



(2) Setting the oscillation frequency

The internal oscillation frequency is set by the resistor connected to the RT pin and the capacitor connected to the CT pin. The waveform generated on CT is a triangular wave with the charging/discharging waveform determined by RT and CT.

$$f_{OSC} = 1.32 \times \frac{1}{CT \times RT} \text{ [Hz]}$$

The actual internal oscillation frequency deviates from the calculated value due to overshoot, undershoot and other factors, so the frequency should be confirmed in an actual set.

(3) External input CLK function (CLK_IN)

Switching operation can be synchronized with external clock input (CLK_IN) by using the CLK_IN pin.

- External clock (CLK_IN) frequency and input level

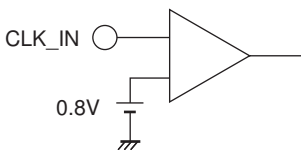
  When using external clock (CLK_IN) input, input a frequency equal to the internal oscillation frequency +20% or more to CLK_IN. In addition, the CLK_IN configuration is shown in the figure “CLK_IN (input) equivalent circuit (outline)” below.

  The 0.8V reference voltage and CLK_IN are compared to determine the edges, so input a signal of 0.8V or more (V_{CC} voltage or less) as the external clock (CLK_IN).
- External/internal clock switching

  Set the CTL pin Low before switching between the external clock and the internal clock. Switching clocks when running may give rise to output voltage fluctuations.
- Maximum ON duty

  The maximum ON duty (Duty_MAX*) of channel 3 to channel 4 is the 85% (typ.) setting. When using the external clock (CLK_IN), the maximum ON duty (Duty_MAX*) becomes smaller, so care must be taken for the set output voltage.

(CLK_IN (input) equivalent circuit (outline))



(4) SCP function

• Description of operation

When any one of FB1 to FB4 goes High due to the load being shorted or other reason, charging to the SCP pin starts. If output does not recover during the set time Tscp and the SCP pin voltage exceeds the threshold voltage, the protection circuit (SCP) operates, and all channel outputs are turned OFF. The SCP_OUT pin set from High to Low. All outputs are latched OFF by the protection circuit (SCP). This latched state (output OFF) is canceled by setting the CTL pin Low or by turning the power supply off.

When not using the protection function (SCP), the SCP pin must be shorted to GND_S with a line that is as short as possible.

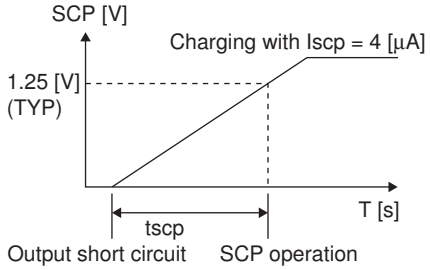
• SCP_OUT

The SCP_OUT pin functions to notify an external microcontroller or other component of the output status (Low when SCP operates). The output configuration is an open drain output, and a pull-up resistor is used. When not used, leave this pin open.

• Switching time

The SCP_OUT switching time is set by the capacitor connected to the SCP pin.

(SCP charging operation)



(SCP and SCP_OUT operation)