



SANYO Semiconductors

DATA SHEET

LV5103LP — Bi-CMOS LSI Cell Phone Power Supply IC

Overview

The LV5103LP is a cell phone power supply IC.

Functions

- Single step-down DC-DC converter channel
- Eight series regulator channels
- Built-in thermal shutdown circuit

Features

- Low power dissipation
- Built-in shorting protection circuit

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		6	V
Allowable power dissipation	Pd max	Mounted on a circuit board.*	1100	mW
Operating temperature	Topr		-30 to +75	°C
Storage temperature	Tstg		-40 to +125	°C

* Specified circuit board : 40×50×0.8mm³ : 4-layer (2S2P) glass epoxy printed circuit board

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		3.2 to 4.5	V

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LV5103LP

Electrical Characteristics

Ta = 25°C, VBAT = 3.7V, VBATL = 2.4V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Analog block] Current drain						
Current drain 1	I _{CC1}	With LD01 and VBATDET operating		8	16	μA
Current drain 2	I _{CC2}	With LD01, LD02, LD05, LD06, LD07, and LD08 operating, PS mode		50	75	μA
Current drain 3	I _{CC3}	With all LD0n channels operating, DC-DC operation		6	10	mA
[Switching Regulator Block] DC/DC1						
Output voltage 1	V _{OSW1}	I _O = 500mA	2.25	2.4	2.55	V
Output current	I _{SW1}		800			mA
Efficiency 1	EF1	I _O = 150mA		86		%
Efficiency 2	EF2	I _O = 500mA		79		%
Oscillator frequency	Fosc1		1	1.2	1.4	MHz
LDO1						
Output voltage	V _{OR1}	I _O = 10mA	1.47	1.5	1.53	V
Output current	I _{M1}		30			mA
Load regulation	V _{L1}	I _O = 1 to 30mA		10	75	mV
Line regulation	V _{R1}	VBAT = 3.1 to 4.5V, I _O = 20mA		10	60	mV
Output voltage temperature coefficient	ΔVT1	Ta = -30 to 75°C, I _O = 10mA		±100		ppm/°C
Ripple rejection ratio	V _{RL1}	I _O = 10mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON1}	I _O = 10mA, 10Hz < f < 100kHz		60		μVrms
LDO2						
Output voltage	V _{OR2}	I _O = 30mA	2.79	2.85	2.91	V
Output current	I _{M2}		200			mA
Load regulation	V _{L2}	I _O = 1 to 200mA		20	75	mV
Line regulation	V _{R2}	VBAT = 3.1 to 4.5V, I _O = 130mA		10	60	mV
Output voltage temperature coefficient	ΔVT2	Ta = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL2}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON2}	I _O = 30mA, 10Hz < f < 100kHz		50		μVrms
LDO2 PS MODE						
Output voltage	V _{OR2P}	I _O = 30mA	2.76	2.85	2.94	V
Output current	I _{M2P}		200			mA
Load regulation	V _{L2P}	I _O = 1 to 200mA		20	75	mV
Line regulation	V _{R2P}	VBAT = 3.1 to 4.5V, I _O = 130mA		10	60	mV
Output voltage temperature coefficient	ΔVT2P	Ta = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL2P}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		60		dB
Output noise voltage	V _{ON2P}	I _O = 30mA, 10Hz < f < 100kHz		60		μVrms
LDO3						
Output voltage	V _{OR3}	I _O = 30mA	2.79	2.85	2.91	V
Output current	I _{M3}		150			mA
Load regulation	V _{L3}	I _O = 1 to 150mA		20	75	mV
Line regulation	V _{R3}	VBAT = 3.1 to 4.5V, I _O = 100mA		10	60	mV
Output voltage temperature coefficient	ΔVT3	Ta = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL3}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON3}	I _O = 30mA, 10Hz < f < 100kHz		50		μVrms
LDO3B SW						
Switch on-resistance	RSW3	I _O = 50mA, SWCTL : HIGH		1.5	2.5	Ω
Switch leakage current	ISW3	SWCTL : LOW		0	3	μA

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LV5103LP

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LDO4						
Output voltage 1	V _{OR41}	I _O = 30mA	3.03	3.1	3.17	V
Output voltage 2	V _{OR42}	I _O = 200mA	3	3.1	3.2	V
Output current 1	I _{M41}		450			mA
Output current 2	I _{M42}	V _{BAT} = 3.4V, V _{OUT} ≥ 3V	300			mA
Load regulation 1	V _{L4}	I _O = 1 to 300mA		30	100	mV
Load regulation 2	V _{L4L}	V _{BAT} = 3.4V, I _O = 1 to 250mA		50	100	mV
Line regulation 1	V _{R4}	V _{BAT} = 3.4 to 4.5V, I _O = 200mA		10	60	mV
Output voltage temperature coefficient	ΔVT4	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL4}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON4}	I _O = 30mA, 10Hz < f < 100kHz		50		μVrms
LDO5						
Output voltage	V _{OR5}	I _O = 30mA	3.23	3.3	3.37	V
Output current 1	I _{M51}		150			mA
Output current 2	I _{M52}	V _{BAT} = 3.4V, V _{OUT} ≥ 3V	150			mA
Load regulation 1	V _{L5}	I _O = 1 to 150mA		75	150	mV
Load regulation 2	V _{L5L}	V _{BAT} = 3.4V, I _O = 1 to 50mA		75	150	mV
Line regulation 1	V _{R5}	V _{BAT} = 3.4 to 4.5V, I _O = 100mA		10	60	mV
Output voltage temperature coefficient	ΔVT5	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL5}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON5}	I _O = 30mA, 10Hz < f < 100kHz		50		μVrms
LDO5 PS MODE						
Output voltage	V _{OR5P}	I _O = 30mA	3.2	3.3	3.4	V
Output current	I _{M5P}		150			mA
Load regulation 1	V _{L5P1}	I _O = 1 to 150mA		75	150	mV
Load regulation 2	V _{L5P2}	V _{BAT} = 3.4V, I _O = 1 to 50mA		75	150	mV
Line regulation 1	V _{R5P}	V _{BAT} = 3.4 to 4.5V, I _O = 100mA		10	60	mV
Output voltage temperature coefficient	ΔVT5P	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL5P}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		60		dB
Output noise voltage	V _{ON5P}	I _O = 30mA, 10Hz < f < 100kHz		60		μVrms
LDO6						
Output voltage	V _{OR6}	I _O = 30mA	1.47	1.5	1.53	V
Output current	I _{M6}		200			mA
Load regulation	V _{L6}	I _O = 1 to 200mA		20	75	mV
Line regulation 1	V _{R6}	V _{BAT} = 3.1 to 4.5V, I _O = 130mA		10	60	mV
Output voltage temperature coefficient	ΔVT6	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL6}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON6}	I _O = 30mA, 10Hz < f < 100kHz		50		μVrms
LDO6 PS MODE						
Output voltage	V _{OR6P}	I _O = 30mA	1.45	1.5	1.55	V
Output current	I _{M6P}		10			mA
Load regulation	V _{L6P}	I _O = 1 to 10mA		10	75	mV
Line regulation 1	V _{R6P}	V _{BAT} = 3.1 to 4.5V, I _O = 10mA		10	60	mV
Output voltage temperature coefficient	ΔVT6P	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL6P}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		60		dB
Output noise voltage	V _{ON6P}	I _O = 30mA, 10Hz < f < 100kHz		60		μVrms

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LV5103LP

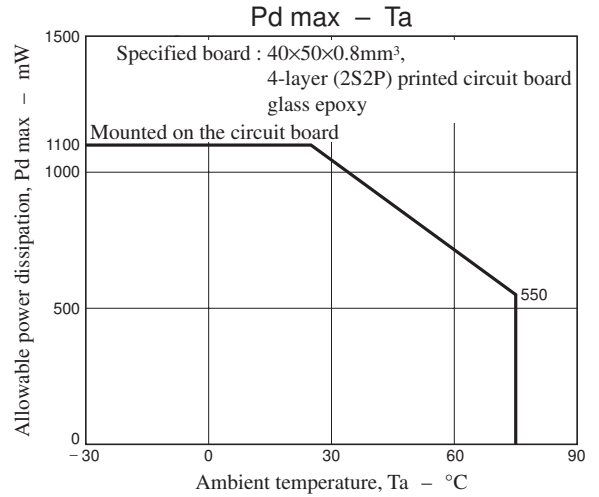
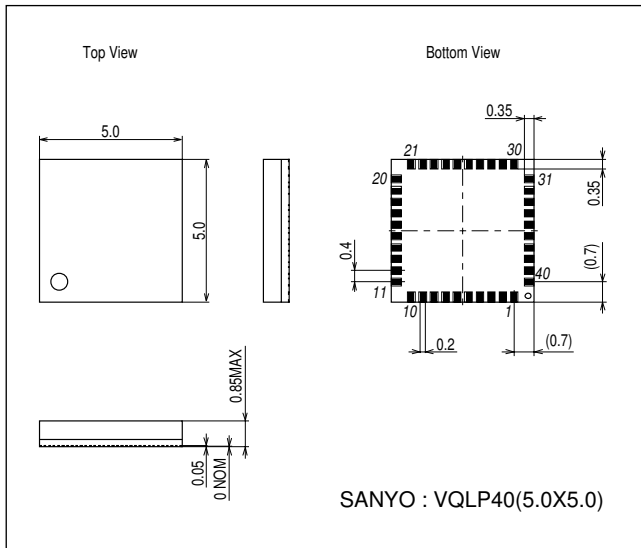
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LDO7						
Output voltage	V _{OR7}	I _O = 30mA	1.76	1.8	1.84	V
Output current	I _{M7}		150			mA
Load regulation	V _{L7}	I _O = 1 to 150mA		75	150	mV
Line regulation 1	V _{R7}	V _{BAT} = 3.1 to 4.5V, I _O = 100mA		10	60	mV
Output voltage temperature coefficient	ΔV _{T7}	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL7}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON7}	I _O = 30mA, 10Hz < f < 100kHz		50		μVrms
LDO7 PS MODE						
Output voltage	V _{OR7P}	I _O = 30mA	1.74	1.8	1.86	V
Output current	I _{M7P}		10			mA
Load regulation	V _{L7P}	I _O = 1 to 10mA		75	150	mV
Line regulation 1	V _{R7P}	V _{BAT} = 3.1 to 4.5V, I _O = 10mA		10	60	mV
Output voltage temperature coefficient	ΔV _{T7P}	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL7P}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		60		dB
Output noise voltage	V _{ON7P}	I _O = 30mA, 10Hz < f < 100kHz		60		μVrms
LDO8						
Output voltage 1	V _{OR81}	I _O = 30mA	1.17	1.2	1.23	V
Output voltage 2	V _{OR82}	I _O = 200mA	1.13	1.2	1.27	V
Output current 1	I _{M81}		500			mA
Output current 2	I _{M82}	V _{BAT} = 3.4V, V _{OUT} ≥ 1.1V	500			mA
Load regulation	V _{L8}	I _O = 1 to 500mA		30	70	mV
Line regulation 1	V _{R8}	V _{BAT} = 3.1 to 4.5V, I _O = 330mA		10	60	mV
Output voltage temperature coefficient	ΔV _{T8}	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL8}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		65		dB
Output noise voltage	V _{ON8}	I _O = 30mA, 10Hz < f < 100kHz		50		μVrms
LDO8 PS MODE						
Output voltage	V _{OR8P}	I _O = 30mA	1.16	1.2	1.24	V
Output current	I _{M8P}		10			mA
Load regulation	V _{L8P}	I _O = 1 to 10mA		30	100	mV
Line regulation 1	V _{R8P}	V _{BAT} = 3.1 to 4.5V, I _O = 10mA		10	60	mV
Output voltage temperature coefficient	ΔV _{T8P}	T _a = -30 to 75°C, I _O = 30mA		±100		ppm/°C
Ripple rejection ratio	V _{RL8P}	I _O = 30mA, VRR = -20dBV, fRR = 120Hz		60		dB
Output noise voltage	V _{ON8P}	I _O = 30mA, 10Hz < f < 100kHz		60		μVrms
DET24						
Low-level detection voltage	V _{DL1}		2.35	2.4	2.45	V
High-level detection voltage	V _{DH1}		2.62	2.7	2.78	V
VBATDET						
Low-level detection voltage	V _{DL2}		2.3	2.4	2.5	V
High-level detection voltage	V _{DH2}		3.1	3.2	3.3	V
BVLT Switch						
BVLT switch on-resistance	RSWBV	I _O = 3mA, BVLTON : HIGH		300	400	Ω
BVLT switch leakage current	ISWBV	BVLTON : LOW		0	1	μA
Control Pins						
High level 1	VH1	RFPDN, ADPTDETIN, PWRHOLD, POWERSAVE, SWCTL, BVLTON, STCLR	1.5		V _{BAT}	V
Low level 1	VL1	RFPDN, ADPTDETIN, PWRHOLD, POWERSAVE, SWCTL, BVLTON, STCLR	0		0.3	V
High level 2	VH2	PWRKEY	V _{BAT} ×0.8		V _{BAT}	V
Low level 2	VL2	PWRKEY	0		V _{BAT} ×0.2	V

LV5103LP

Package Dimensions

unit : mm (typ)
3302A



Control Pin Functions

Power Supply Control

RFPDN	ADPTDET	PWRKEY	PWRHOLD	LDO1	LDO2, 5, 6, 7, 8	LDO3, 4
Low	Low	Low	Low	On	Off	Off
Low	High			On	On	Off
Low		High		On	On	Off
Low			High	On	On	Off
High	Low	Low	Low	On	Off	Off
High	High			On	On	On
High		High		On	On	On
High			High	On	On	On

(ON/OFF1)

(ON/OFF2)

PS Mode

PWRSAVE	Mode
Low	PS mode
High	Normal mode

LDO3 Output Switch

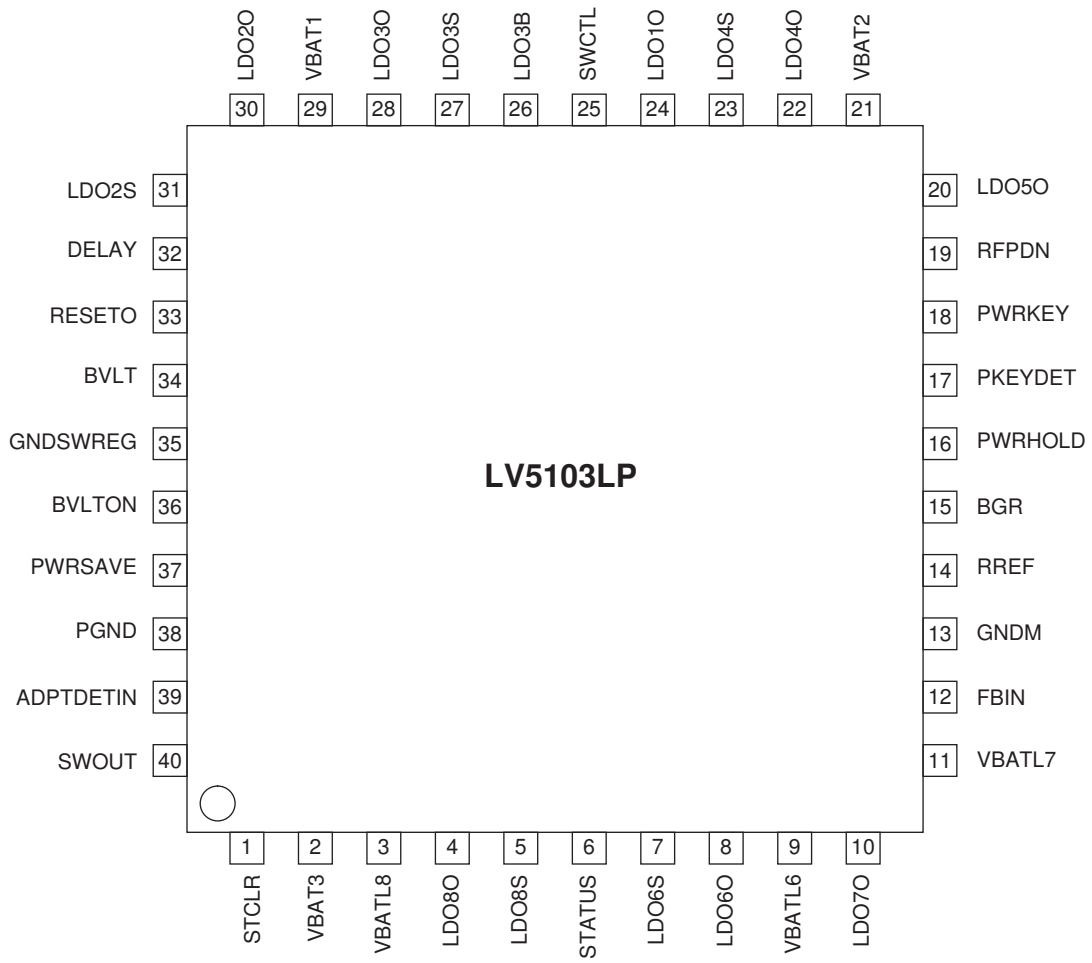
SWCTL	Mode
Low	Switch off
High	Switch on

BVLT Output

BVLTON	Mode
Low	Switch off
High	Switch on

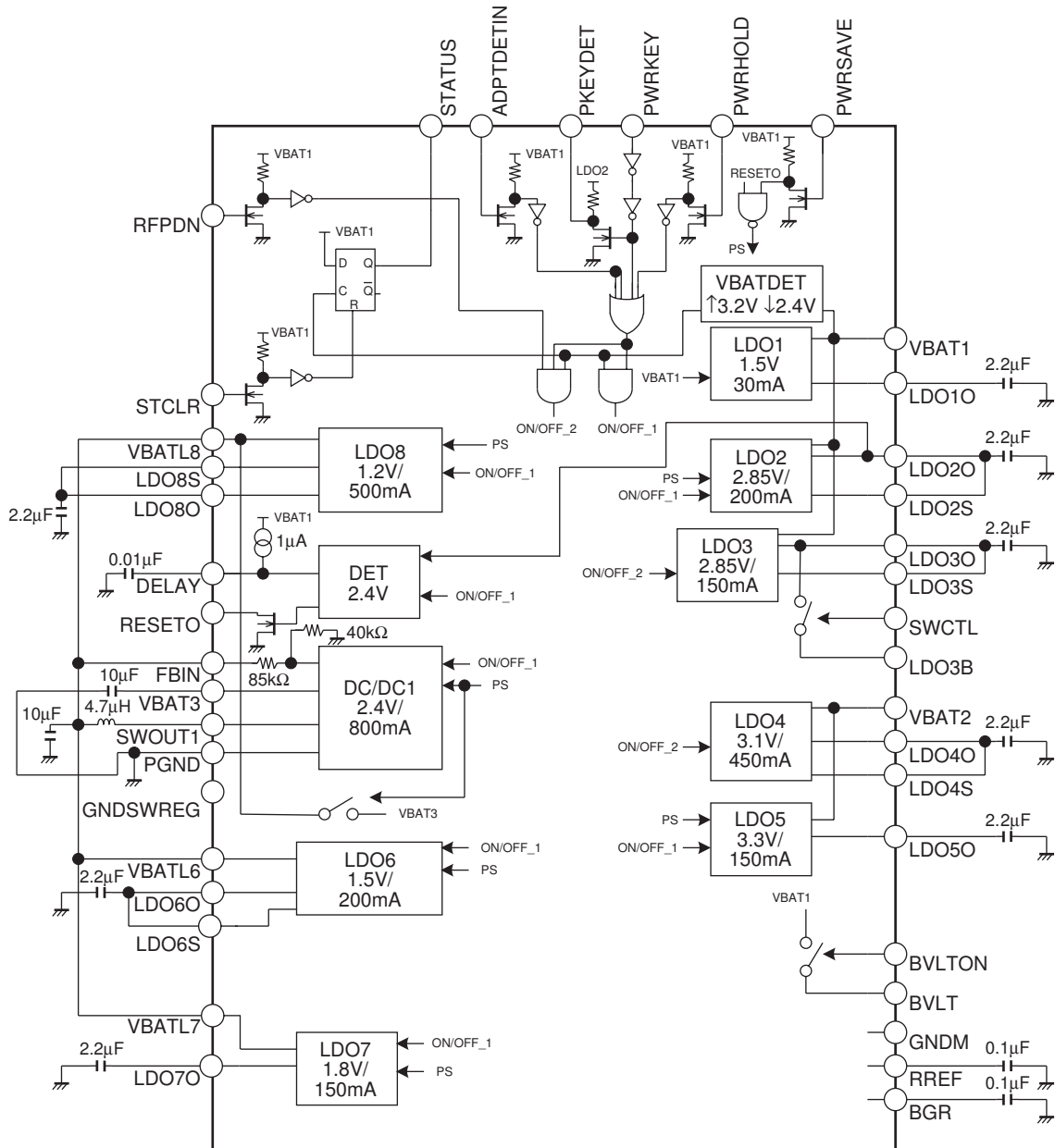
LV5103LP

Pin Assignment



LV5103LP

Block Diagram



The three power supply pins VBAT1, VBAT2, and VBAT3 must be shorted together externally. The three ground pins GNDM, PGND, and GNDSWREG must be shorted together externally and must always be at a potential that is the lowest potential in the system.

LV5103LP

Equivalent Circuit Block Diagram

Pin No.	Pin	Functions	Equivalent Circuit
1 16 19 37 39	STCLR PWRHOLD RFPDN PWRSAVE ADPTDETIN	Input pins	
29 21 2	VBAT1 VBAT2 VBAT3	Power supply pins	
3 9 11	VBATL8 VBATL6 VBATL7	VBATL pins The M1 transistor is only present in the VBATL8 circuit.	
4 5 7 8 10 20 22 23 24 27 28 30 31	LDO8O LDO8S LDO6S LDO6O LDO7O LDO5O LDO4O LDO4S LDO1O LDO3S LDO3O LDO2O LDO2S	LDO output pins The LDO*O pins for LDO1, LDO5, and LDO7 are shorted internally in the IC to the corresponding LDO*S pin.	
6	STATUS	STATUS pin	

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LV5103LP

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Pin No.	Pin	Functions	Equivalent Circuit
12	FBIN	Feedback resistor connection for the switching regulator block	
14	RREF	RREF reference voltage	
15	BGR	BGR reference voltage	
17	RKEYDET	PKEYDET pin	
18	PWRKEY	PWRKEY pin	

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LV5103LP

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Pin No.	Pin	Functions	Equivalent Circuit
25 26	SWCTL LDO3B	SWCTL pin LDO3B pin	
32	DELAY	DELAY pin	
33	RESET	RESET pin	
34 36	BVLT BVLTON	BVLT and BVLTON pins	
40	SWOUT	SWREG output block	

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