Ordering number: EN3892B

Monolithic Linear IC

L88R05 Series

5 V, 1 A Voltage-regulator ICs with Reset Function

Overview

The L88R05 Series is a series of low-saturation voltage regulator ICs that are equipped with a function that generates a reset signal when the power supply for a microcontroller system is turned on or off.

Applications

- Prevents malfunction when the microcontroller power supply is turned on or off.
- Designed to handle malfunction caused by momentary power interruptions.
- Suited for portable electronic equipment, mobile electronic equipment, and other battery-powered equipment with little capacity to handle fluctuation in input voltage; also suited for equipment with large fluctuations in the primary power supply.

Functions

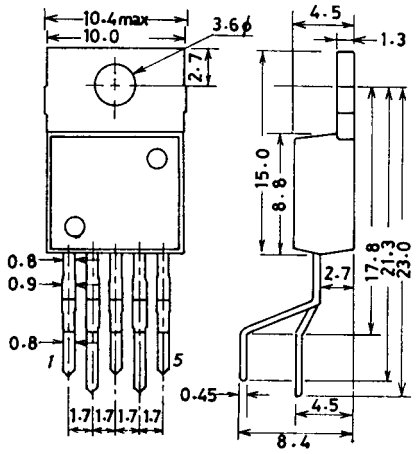
- Power supply reset generation function; the reset threshold voltages are ranked.
  ~~L88R05C: V_{RT} = 4.5 V~~
  L88R05D: V_{RT} = 4.2 V
  ~~L88R05E: V_{RT} = 3.9 V~~
- 5 V, 1 A output characteristics

Package Dimensions

unit : mm

3079-T0220-5H

[L88R05 Series]



SANYO : TO220-5H

Features

- Minimum I/O voltage difference is small (0.5 V typ.), making power conservation possible, and makes smaller heatsink and transformers possible.
- External capacitor for reset signal output delay time adjustment.
- Sink/source reset output provides compatibility with logic circuitry that has an internal pull-down resistor. Active pull-up facilitates noise suppression.
- Various types of protective circuits on chip (fold back current limiting, thermal protection).
- The package is the TO220-5H; this package facilitates designs for the radiation of heat during the mounting process.

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input voltage	V_{IN} max		18	V
Reset pin voltage	$V_{\overline{RES}}$ max		18	V
Allowable power dissipation	Pd max	Ta % 25°C, independent IC	1.75	W
		Tc % 50°C, ideal radiation of heat	20	W
Junction-to-ambiet thermal resistance	Uj-a		71.4	°C/W
Junction-to-case thermal resisitance	Uj-c		5	°C/W
Operating temperature	Topr		–40 to +85	°C
Storge temperature	Tstg		–55 to +150	°C

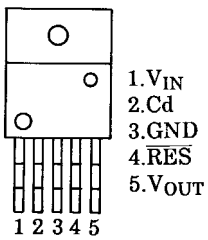
Operating Conditions at Ta = 25 °C

Parament	Symbol	Conditions	Ratings	Unit
Input voltage	V_{IN}		5.6 to 17	V
Output current	I_{OUT}		0 to 1	A
Reset output source current	I_{ORH}		0 to 200	μA
Reset output sink current	I_{ORL}		0 to 2	mA

Operating Characteristics at Tj = 25 °C, V_{IN} = 8 V, I_{OUT} = 1 A, C_{OUT} = 47 μA for specified circuits

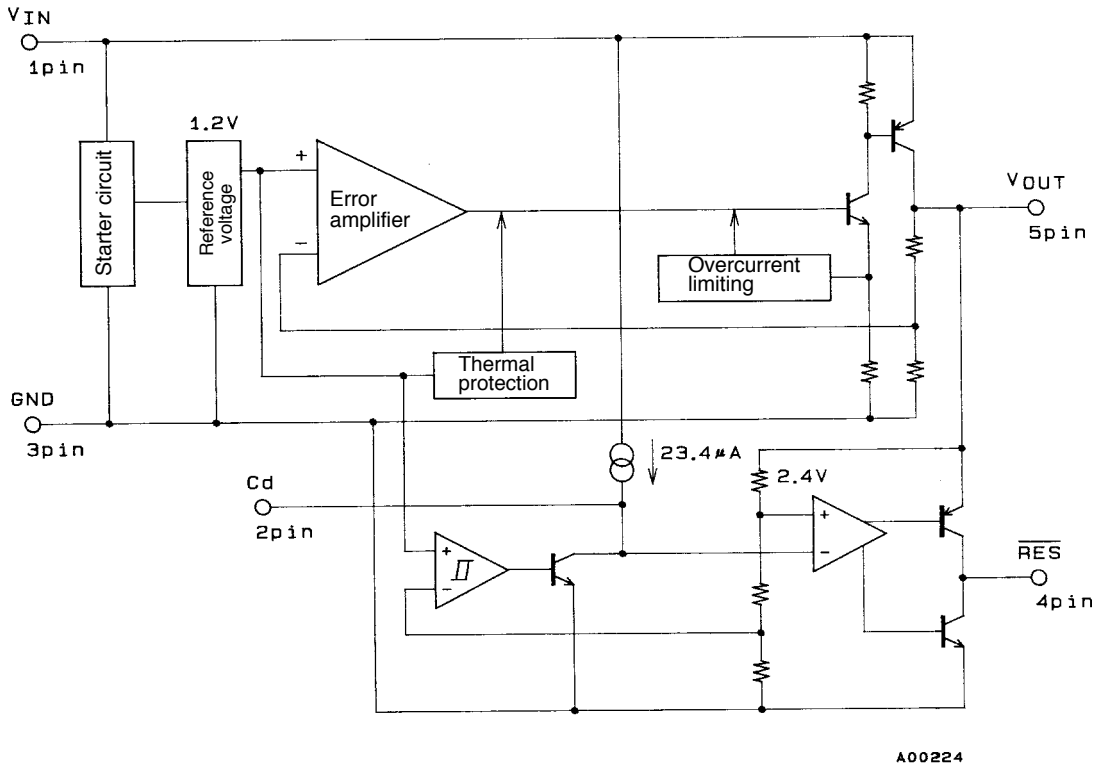
Parameter	Symbol	Condition	min	typ	max	Unit
[Power Supply]						
Output voltage	V_{OUT}		4.85	5.0	5.15	V
Dropout voltage	V_{DROP1}			0.5	1.0	V
	V_{DROP2}	I_{OUT} = 300 mA		0.25	0.50	V
Line regulation	ΔV_{OLN}	5.6 V % V_{IN} % 17 V		10	70	mV
Load regulation	ΔV_{OLD}	5 mA % I_{OUT} % 1 A		50	150	mV
Peak output current	I_{OP}		1	1.8		A
Output short-circuit current	I_{OSC}			0.3	1.2	A
Current drain	I_{Q1}	I_{OUT} = 0		2.1	4	mA
	I_{Q2}			32	80	mA
Output noise voltage	V_{NO}	10 Hz % f % 100 kHz		70		μVrms
Output voltage temperature coefficient	ΔVo/ΔTa	Tj =25 to 125 °C		–0.5		mV/°C
Ripple rejection ratio	Rrej	f = 120 Hz, 6 V % V_{IN} % 17 V		60		dB
[Reset]						
High-level reset output voltage	V_{ORH}	I_{ORH} = 200 μA, CD open	4.83	4.98	5.13	V
Low-level reset output voltage	V_{ORL}	I_{ORL} = 2 mA, CD grounded		100	200	mV
Reset threshold voltage	V_{RT}	~~C-rank~~	~~4.3~~	~~4.5~~	~~4.7~~	~~V~~
		D-rank	4.0	4.2	4.4	V
		~~E-rank~~	~~3.7~~	~~3.9~~	~~4.1~~	~~V~~
Reset hysteresis voltage	V_{hys}		50	100	200	mV
Output delay time	t_d	Cd = 0.1 μF	7.5	10	12.5	ms

Pin Assignments

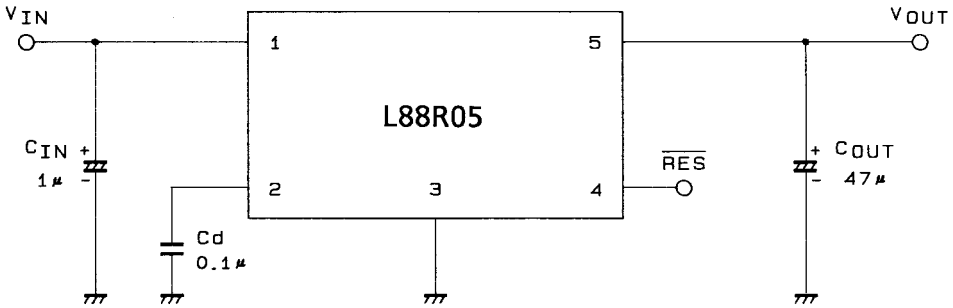


Top view

Equivalent Circuit Block Diagram



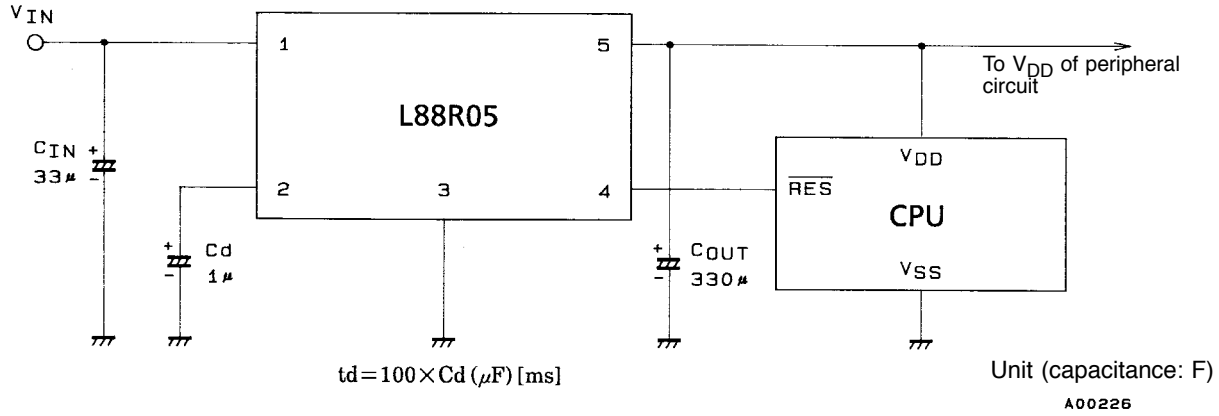
Measurement Circuit



Unit (capacitance: F)

A00225

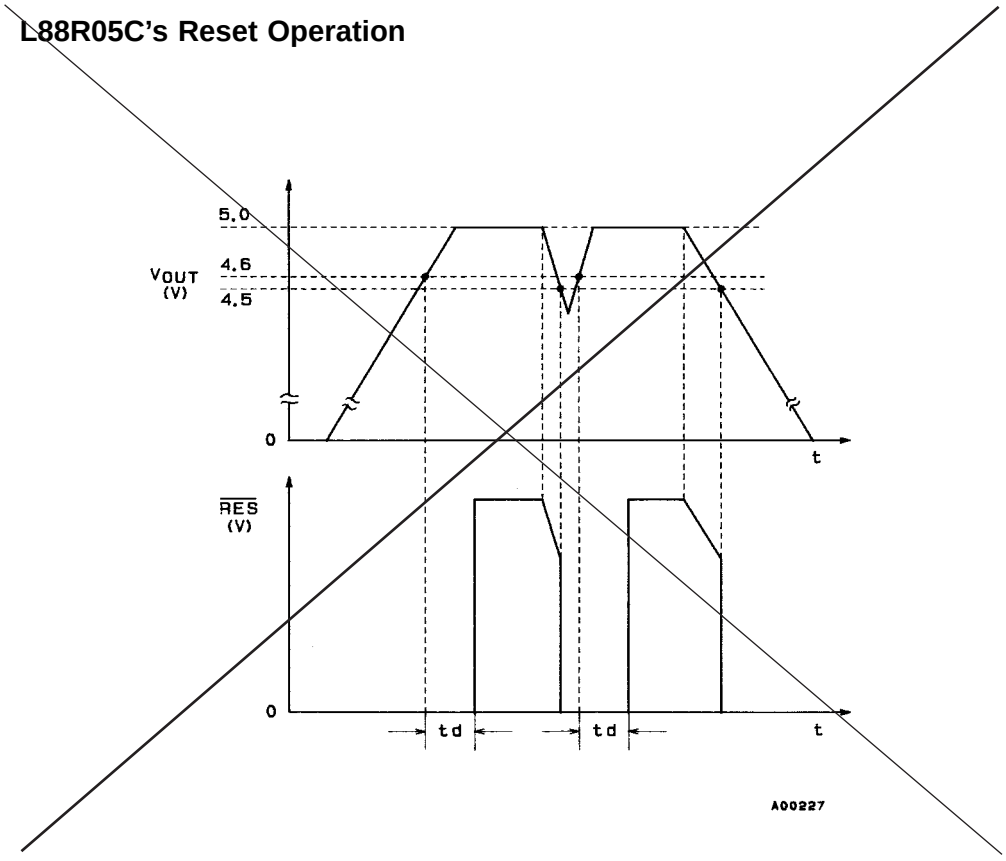
Sample Application Circuit



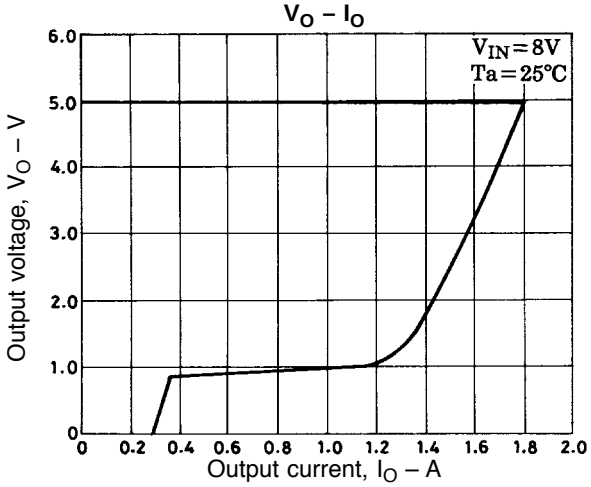
Notes:

1. Set C_{OUT} to be 47 μF or greater and select it according to the applications.
2. Use the capacitators for C_{OUT} and Cd with high-temperature stability.

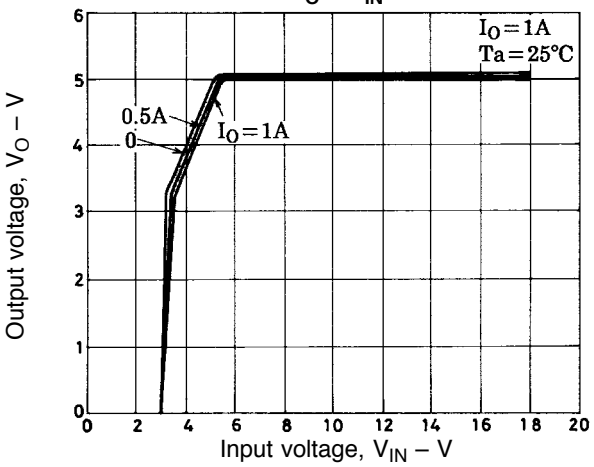
L88R05C's Reset Operation



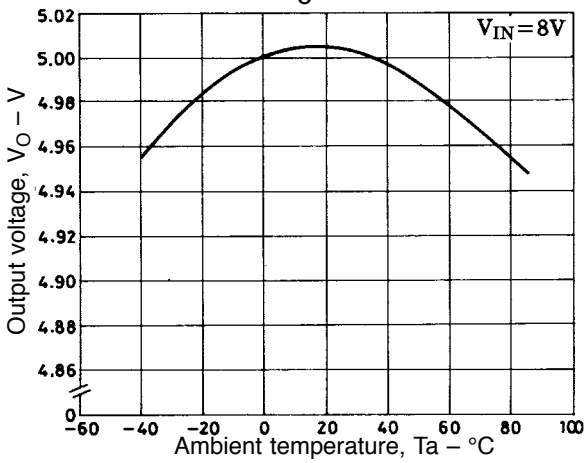
$V_O - I_O$



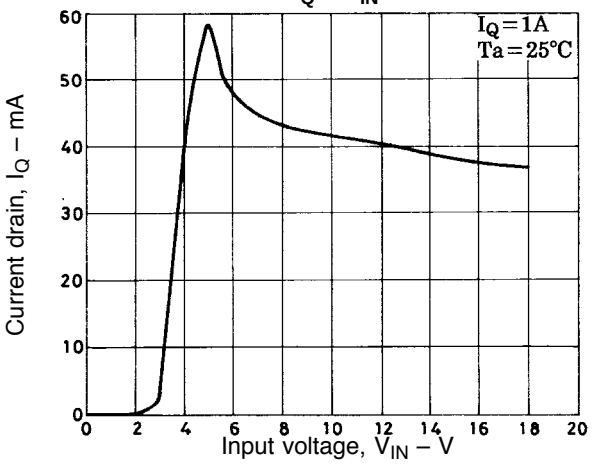
$V_O - V_{IN}$



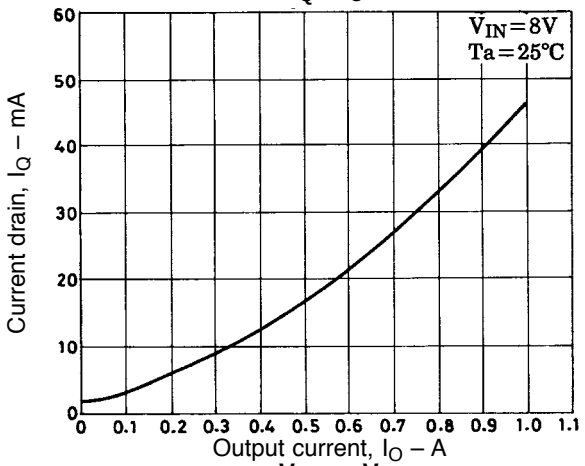
$V_O - Ta$



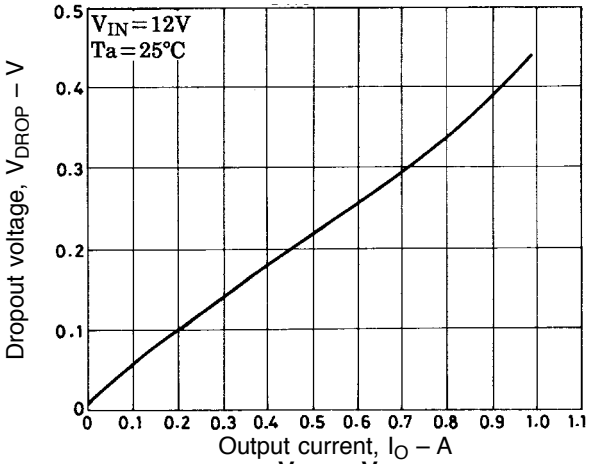
$I_Q - V_{IN}$



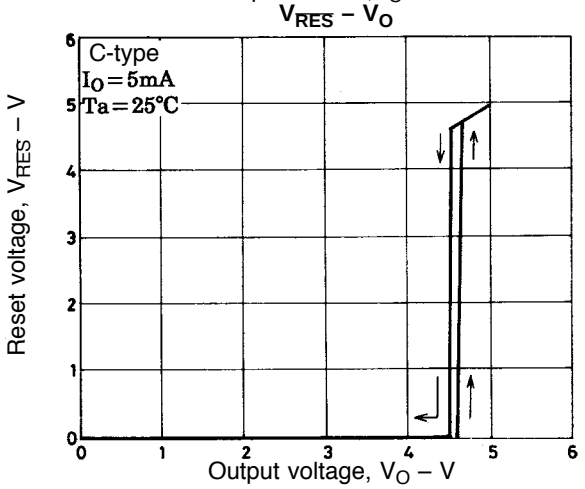
$I_Q - I_O$



$V_{DROP} - I_O$



$V_{RES} - V_O$



$V_{RES} - V_O$