


SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LA72702NV — Monolithic Linear IC For US TV BTSC Decoder

Overview

The LA72702NV is a US TV BTSC Decoder.

Features

- With SIF circuit, alignment-free* STEREO channel separation.
- * When base band signal input, separation is adjusted by input level.
- Dual slave address(80h, 84h).

Functions

- SIF FM-Demodulator
- STEREO decoder
- dbx Noise Reduction
- STEREO detection
- STEREO detection sensitivity change function
- SAP demodulator
- SAP detection
- SAP output select 2-levels
- SAP detection sensitivity change function

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V _{CCH} max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ 85°C, Mounted on a specified board*	290	mW
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 114.3mm×76.1mm×1.6mm, glass epoxy board

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	vacate		5.0	V
Allowable operating voltage range	V _{CCH} op		4.5 to 5.5	V

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.
<http://www.sanyosemi.com/en/network/>

LA72702NV

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation	I _{CC}	No signal Inflow current at pin 19, default condition	30	40	50	mA
SIF input level (Reference)	V _{LIM}	f _c = 4.5MHz Deviation MONO (300Hz, Mod = 100%, Pre-emphasis ON) → ±25kHz	(80)	(90)	(100)	dBμV
Base band input level (Reference)	V _{LIMB}	100% Modulation MONO(L+R) : 530mVp-p (300Hz, Pre-emphasis ON) SUB(L-R) : 380mVp-p (300Hz, dbx-NR ON), Pilot : 110mVp-p SAP : 300mVp-p (300Hz, dbx-NR ON)				
MONO output level	V _{OMON}	f _m =1kHz, 100% Mod, 15kHz LPF	-7.0	-5.5	-4.5	dBV
MONO distortion	THDMON	f _m =1kHz, 100% Mod, 15kHz LPF		0.15	0.6	%
MONO frequency characteristics	FCM1	f _m =3kHz, 30% Mod, Pre-emphasis ON * Measure ratio from f _m =1kHz level.	-2	0	2	dB
MONO S/N ratio	SNM	S=V _{OMON} , N=0% Mod, 15kHz LPF	55	65		dB
STEREO output level	V _O ST	f _m =1kHz, 100% Mod, 15kHz LPF	-7.0	-5.5	-4.5	dBV
STEREO distortion	THDS	f _m =1kHz, 100% Mod, 15kHz LPF		0.5	1.0	%
STEREO frequency characteristics	FCS1	f _m =3kHz, 30% Mod, 15kHz LPF * Measure ratio from f _m =1kHz level.	-2	0	2	dB
STEREO S/N ratio	SNS	S=V _O ST, N=0% Mod, 15kHz LPF	50	60		dB
STEREO separation 1	STSE1	f=300Hz (R/L), 30% Mod, 15kHz LPF	20	25		dB
STEREO separation 2	STSE2	f=3kHz (R/L), 30% Mod, 15kHz LPF	20	25		dB
STEREO Detection level-1	V _{IN} SD1	Except Stereo Detection → Stereo Detection * Serial control "SENS HI" Pilot (fH)=15.73kHz * Measure pilot level.	30	38	45	%
STEREO Detection level-2	V _{IN} SD2	Except Stereo Detection → Stereo Detection * Serial control "SENS LO"	38	47	53	%
STEREO Detection hysteresis	HYST	Input Mod. Difference at Stereo/Except Stereo Det. * Serial control "SENS HI"	10	20	30	%
SAP output level-1	V _O SA1	f _m =1kHz, 100% Mod, 15kHz LPF * SAP-1 (serial control)	-14.0	-11.0	-8.0	dBV
SAP output level-2	V _O SA2	f _m =1kHz, 100% Mod, 15kHz LPF * SAP-2 (serial control)	-7.5	-5.5	-3.5	dBV
SAP distortion	THDSA	f _m =1kHz, 100% Mod, 15kHz LPF		0.7	1.5	%
SAP S/N ratio	SNSA	S=V _O SA2, N=0% Mod, 15kHz LPF	50	60		dB
SAP detection level-1	V _{IN} SA1	Except SAP → SAP Det. * Serial control "SENS HI" SAP Carrier=5fH only * Measure output level.	10	17	24	%
SAP detection level-2	V _{IN} SA2	Except SAP → SAP Det. * Serial control "SENS LO" * Measure output level.	17	24	31	%
SAP detection hysteresis	HYSA	Input Mod. Difference at SAP/Except SAP Det. * SAP carrier only. * Serial control "SENS HI"	2	5	10	%
MODE output MONO	MODMO	Input=MONO : f=1kHz, 0% Mod	0.7	1	1.3	V
MODE output SAP	MODSA	Input=SAP : Carrier	1.6	1.9	2.2	V
MODE output STEREO	MODST	Input=STEREO : Pilot	2.5	2.8	3.1	V
MODE output ST + SAP	MODSS	Input=STEREO : Pilot, SAP : Carrier	3.5	3.8	4.2	V
Stereo detect speed (Reference)	STDT	Input=STEREO : Pilot I ² C data no-send Measure pin 20 voltage change to 2.8V timing from Power ON		(480)	(1000)	ms
SAP detect speed (Reference)	SAPDT	SAP : Carrier I ² C data no-send Measure pin 20 voltage change to 1.9V timing from Power ON		(350)	(1000)	ms

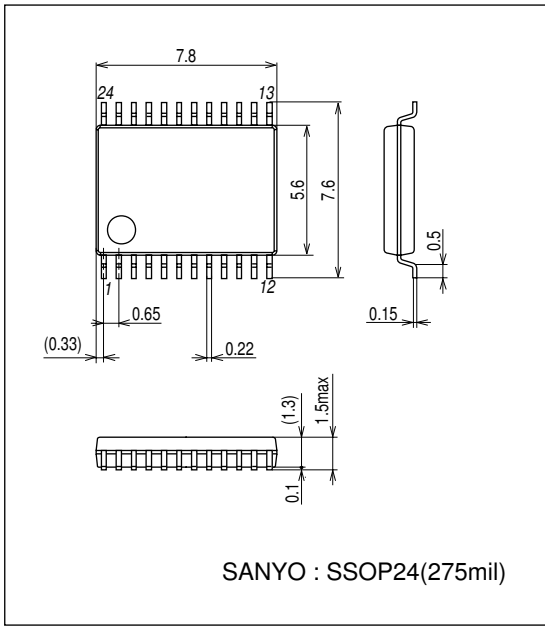
* Normally measurement condition is Input = SIF mode (90dBμV)

* " Reference " Items are reference levels, their specs are no-guarantee.

LA72702NV

Package Dimensions

unit : mm (typ)
3175C



Mode Condition

Signal	I ² C data in									Output mode			I ² C out		Mode pin20
	D8	D7	D6	D5	D4	D3	D2	D1	Lch pin18	Rch pin17	Mode condition	D8	D7		
Stereo + SAP	(0)	(0)	*	(0)	(0)	0	0	0	L	R	Stereo	1	1	3.8V	
	FIX	SIF (1) BASE band	0	STEREO	SAP	0	0	1	SAP	SAP	SAP-1	1	1		
			1	SENS	SENS	0	0	1	SAP	SAP	SAP-2				
			0	Lo	Lo	0	1	0	L+R	SAP	MULTI-1				
			1	(1)	(1)	0	1	0	L+R	SAP	MULTI-2				
			*	Hi	Hi	1	0	0	L+R	L+R	F-MONO				
			*			1	0	1	L+R	L+R	F-MONO				
			*			1	1	0	L+R	L+R	F-MONO				
			*			*	1	1	Off	Off	MUTE				
			*												
Stereo			*			0	0	0	L	R	Stereo	1	0	2.8V	
			*			0	0	1	L	R	Stereo				
			*			0	1	0	L	R	Stereo				
			*			1	0	0	L+R	L+R	F-MONO				
			*			1	0	1	L+R	L+R	F-MONO				
			*			1	1	0	L+R	L+R	F-MONO				
			*			*	1	1	Off	Off	MUTE				
			*												
Mono + SAP			*			*	0	0	L+R	L+R	MONO	0	1	1.9V	
			0			0	0	1	SAP	SAP	SAP-1				
			1			0	0	1	SAP	SAP	SAP-2				
			0			0	1	0	L+R	SAP	MULTI-1				
			1			0	1	0	L+R	SAP	MULTI-2				
			*			*	1	1	Off	Off	MUTE				
			*												
MONO			*			*	0	0	L+R	L+R	MONO	0	0	1.0V	
			*			*	0	1	L+R	L+R	MONO				
			*			*	1	0	L+R	L+R	MONO				
			*			*	1	1	Off	Off	MUTE				

* : no care

LA72702NV

I²C Control Table

Grp-1 (Normally use : group-1 only)

D8	D7	D6	D5	D4	D3	D2	D1	Condition
*						0	0	Stereo
						0	1	SAP
						1	0	Both
						1	1	MUTE
*					0			Normal (Auto DET)
					1			Forced Mono
*				0				SAP SENS LO
				1				SAP SENS HI
*			0					Stereo SENS LO
			1					Stereo SENS HI
*		0						SAP Level-1
		1						SAP Level-2
*	0							SIF mode
	1							Base Band mode
*	0							Fix
	1							Prohibit (TEST MODE)

* : Shows Initial condition

Read out data

D8	D7	D6	D5	D4	D3	D2	D1	Condition
		0	0	0	0	0	0	Fixed
	0							Normal
	1							SAP det
0								Normal
1								Stereo det

Test mode condition(Reference)

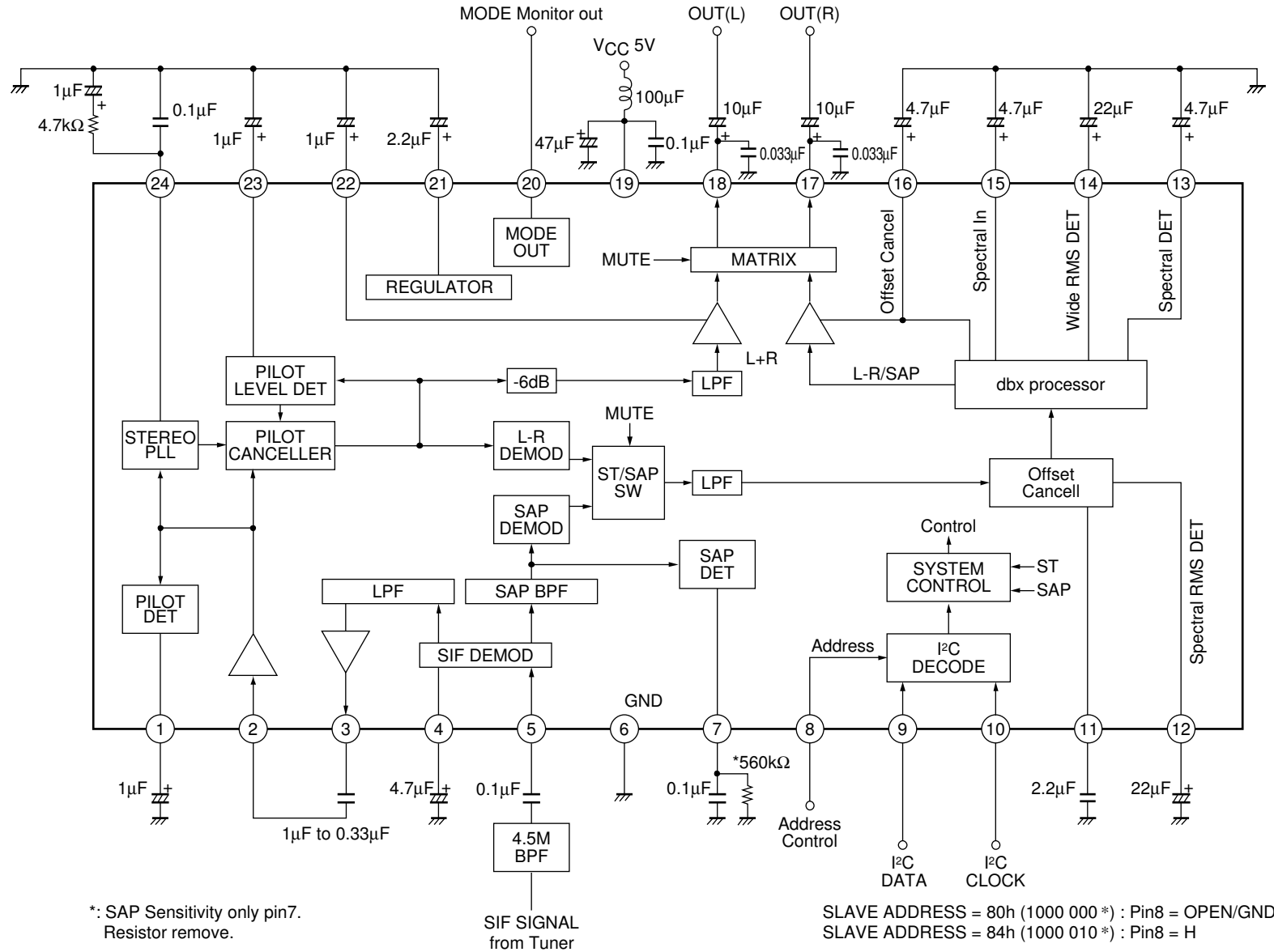
When STOP condition transform at Grp-1 data-end, controlled NORMAL mode.

Grp-2 is only test condition. Usually, these data are no-need. Their data are no guarantee, except all L condition.

D8	D7	D6	D5	D4	D3	D2	D1	Condition/Monitor position
0	0	0	0	0	0	0	0	Normal (Usually, Fixed)
				0	0	0	1	TEST-1 SIF output
				0	0	1	0	TEST-2 SAP BPF
				0	0	1	1	TEST-3 (reserved)
				0	1	0	0	TEST-4 ST VCO
				0	1	0	1	TEST-5 (reserved)
				0	1	1	0	TEST-6 SAP monitor
				0	1	1	1	TEST-7 ST monitor
				1	0	0	0	TEST-8 Pilot cancel monitor
				1	0	0	1	TEST-9 dbx 2.19k LPF
				1	0	1	0	TEST-10 dbx 408 LPF
				1	0	1	1	TEST-11 dbx DET 10k LPF
				1	1	0	0	TEST-12 dbx SPEC 7.6k LPF
				1	1	0	1	TEST-13 dbx SPEC output
				1	1	1	0	TEST-14 L+R/IL-R monitor
				1	1	1	1	TEST-15 dbx 2.09k LPF

Blank Bits are no-care

Slave addresses are 80h (1000 000*, at pin8 Open/GND) and 84h (1000 010*, at pin8 H).



LA72702NV

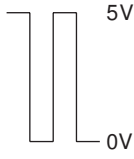
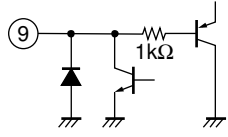

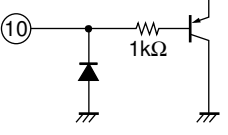
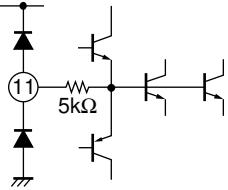
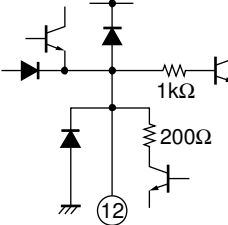
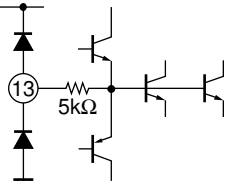
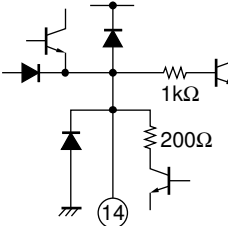
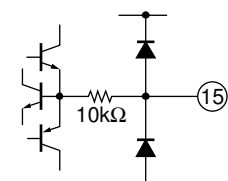
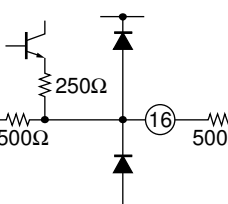
Pin Functions

Pin No.	Pin Name	Function	DC: voltage AC: level	Equivalent Circuit
1	PCPLDET	Pilot level detect for stereo detection	DC : 2.4V	
2	PC_DC_IN	AC coupling (Input)	DC : 2.4V AC : 2.4Vp-p	
3	PC_DCOUT	AC coupling (Output)	DC : 2.4V AC : 2.4Vp-p	
4	PC FIL	SIF offset cancel	DC : 2.6V	
5	PISIF	Signal input Common input at SIF, Base band	DC : 3.7V	
6	GND			
7	CSAPDET	SAP carrier level detect for SAP detection	DC : 2.8V	
8	ADDSEL	Slave address change control OPEN/GND : 80h 5V : 84h	DC : 0V	

Continued on next page.

LA72702NV

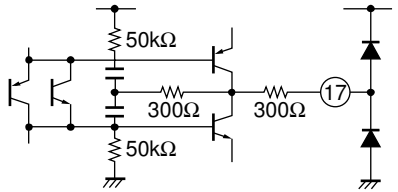
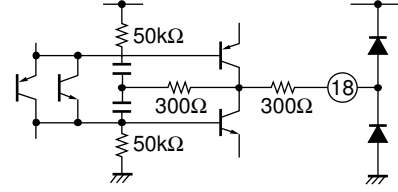
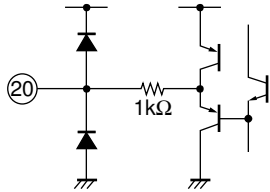
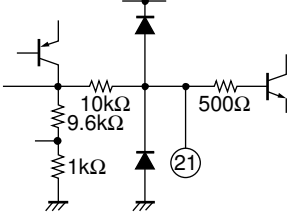
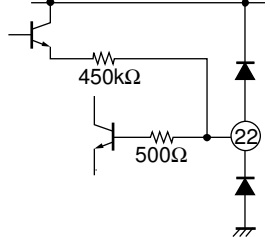
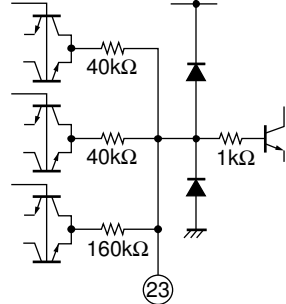
Continued from preceding page.

Pin No.	Pin Name	Function	DC: voltage AC: level	Equivalent Circuit
9	SDA	Serial data input	 5V 0V	
10	SCL	Serial clock input	 5V 0V	
11	PC DBXIN	Offset cancel feedback filter	DC: 2.4V	
12	PCDETSPE	Spectral band RMS detect	DC: 2.3V	
13	PCTIMSPE	dbx spectral detect	DC: 2.4V	
14	PCTNWID	Wide band RMS detect	DC: 2.4V	
15	PCSPECIN	dbx main signal V/I convert filter	DC: 2.4V	
16	PC KE6B	Offset cancel feedback filter	DC: 2.4V AC: 220mVp-p	

Continued on next page.

LA72702NV

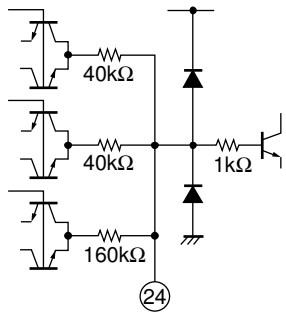
Continued from preceding page.

Pin No.	Pin Name	Function	DC: voltage AC: level	Equivalent Circuit
17	PORCH	Line out R	DC: 2.4V AC: 1.4Vp-p	
18	POLCH	Line out L	DC: 2.4V AC: 1.4Vp-p	
19	V _{CC}			
20	POLED	Mode out MONO = 0.9V SAP = 2.0V STEREO = 3.0V STEREO + SAP = 3.8V	DC: See Right AC: Test only	
21	PCREG	Reference voltage	DC: 2.4V	
22	PMAINOUT	Offset cancel feedback filter	DC: 1.6V	
23	PCPLC	Pilot level detect for pilot canceller	DC: 2.4V	

Continued on next page.

LA72702NV

Continued from preceding page.

Pin No.	Pin Name	Function	DC: voltage AC: level	Equivalent Circuit
24	PCPTFLT	Pilot level detect for ST PLL filter	DC: 2.4V	

I²C BUS Serial Interface Specification

(1) Data transfer manual

This IC adopts control method (I²C-BUS) with serial data, and controlled by two terminals which called SCL (serial clock) and SDA (serial data). At first, set up ^{*1} the condition of starting data transfer, and after that, input 8 bit data to SDA terminal with synchronized SCL terminal clock. The order of transferring is first, MSB (the Most Scale of Bit), and save the order. The 9th bit takes ACK (Acknowledge) period, during SCL terminal takes 'H', this IC pull down the SDA terminal. After transferred the necessary data, two terminals lead to set up and of ^{*2} data transfer stop condition, thus the transfer comes to close.

*1 Defined by SCL rise down SDA during 'H' period.

*2 Defined by SCL rise up SDA during 'H' period.

(2) Transfer data format

After transfer start condition, transfers slave address (1000 000*) to SDA terminal, control data, then, stop condition (See figure 1).

Slave address is made up of 7bits, ^{*3}8th bit shows the direction of transferring data, if it is 'L' takes write mode (As this IC side, this is input operation mode), and in case of 'H' reading mode (As this IC side, this is output operation mode). Data works with all of bit, transfer the stop condition before stop 8bit transfer, and to stop transfer, it will be canceled the transfer dates.

*3 It is called R/W bit.

Fig.1 DATA STRUCTURE "WRITE" mode

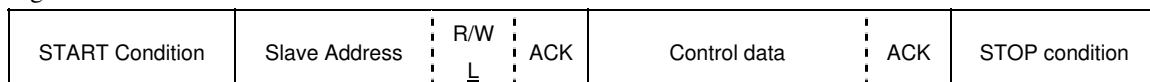
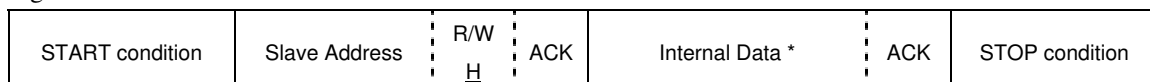


Fig.2 DATA STRUCTURE "READ" mode



* The output data synchronizes with the clock of SCL pin. Then, the ACK output is made after the output data.

bit8 is result of STERO DET (H : STEREO)

bit7 is result of SAP DET (H : SAP)

bit6 to bit1 are fixed to 'L'

(3) Initialize

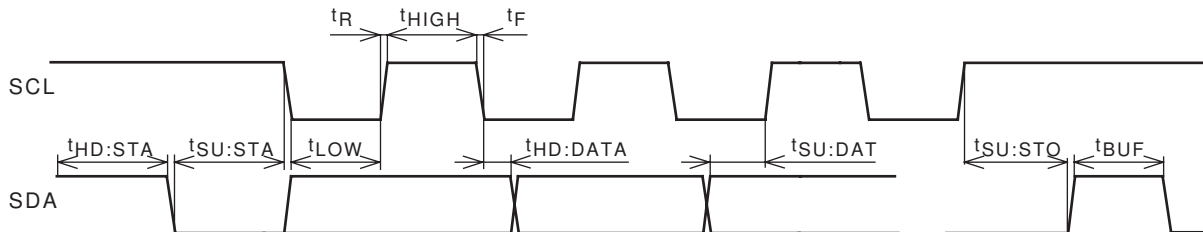
This IC is initialized for circuit protection. Initial condition is "0 (All bits)".

LA72702NV

Reference

Parameter	Symbol	min	max	unit
LOW level input voltage	V_{IL}	-0.5	1.5	V
HIGH level input voltage	V_{IH}	2.5	5.5	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}	0	100	kHz
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7		μs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4.0		μs
LOW period of the SCL clock	t_{LOW}	4.7		μs
Rise time of both SDA and SDL signals	t_R	0	1.0	μs
HIGH period of the SCL clock	t_{HIGH}	4.0		μs
Fall time of both SDA and SDL signals	t_F	0	1.0	μs
Data hold time	$t_{HD:DAT}$	0		μs
Data set-up time	$t_{SU:DAT}$	250		ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0		μs
BUS free time between a STOP and START condition	t_{BUF}	4.7		μs

Definition of timing



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of November, 2007. Specifications and information herein are subject to change without notice.