Ordering number : EN7955A

SANYO Semiconductors
DATA SHEET

LA72680M — Monolithic Linear IC JAPAN TV Sound Multiplex Demodulation HiFi Sound Signal Processor

Overview

The LA72670BM is a HiFi sound signal processor with a built-in SIF demodulation and JAPAN TV sound multiplex demodulation on a single chip.
Full adjustment free operation is realized by the IC's internal automatic adjustment and trimming function, etc.

Functions

- HiFi sound signal processor
- HiFi head amp
- SIF modulation
- JAPAN multiplex modulation

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage 1	$V_{CC}H$ max		9.6	V
Maximum power supply voltage 2	$V_{CC}L$ max		6	V
Always power supply voltage	$V_{CC}A$ max		6	V
Allowable power dissipation	Pd max	Ta=70°C *	1300	mW
Operating ambient temperature	Topr		-10 to +70	°C
Storage ambient temperature	Tstg		-55 to +150	°C

* On board: 114.3mm×76.1mm×1.6mm, glass epoxy board.

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Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage 1	$V_{CC}H$		9	V
Recommended operating voltage 2	$V_{CC}L$		5	V
Recommended always voltage	$V_{CC}A$		5	V
Allowable operating voltage 1	$V_{CC}H$ op1		8.5 to 9.5	V
Allowable operating voltage 2	$V_{CC}L$ op2		4.8 to 5.3	V
Allowable operating always voltage	$V_{CC}A$ op3		4.5 to 5.5	V

Electrical Characteristics at Ta = 25°C, $V_{CC}H$=9V, $V_{CC}L$=5V, $V_{CC}A$=5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation REC&EE 9V	$I_{CC}R1$	No signal, Inflow current at Pin 3/54 G1D8D7:00	42	50	58	mA
Current dissipation EE 5V	$I_{CC}E1$	No signal, Inflow current at Pin 15/32/36/46 G1D8D7:00	63	75	87	mA
Current dissipation REC 5V	$I_{CC}R2$	No signal, Inflow current at Pin 15/32/36/46 G1D8D7:00, G1D4:1	89	105	121	mA
Current dissipation PB 9V	$I_{CC}P1$	No signal, Inflow current at Pin 3/54 G1D8D7:01	9	11	13	mA
Current dissipation PB 5V	$I_{CC}P2$	No signal, Inflow current at Pin 15/32/36/46 G1D8D7:01	76	90	104	mA
Current dissipation always power supply	$I_{CC}AL$	No signal, Inflow current at Pin 5, Mute H at Pin 49	0.8	1.0	1.2	mA
EE through (LINE IN to LINE OUT), EE mode, f=1kHz, L/R-ch						
Output level 1	V_O1	V_{IN}=-28.2dBV, Gain=1 (G3 D4:0)	-10.5	-9	-7.5	dBV
Output level 2	V_O2	V_{IN}=-28.2dBV, Gain=2 (G3 D4:1)	-9.5	-8	-6.5	dBV
Output distortion	THD	V_{IN}=-28.2dBV, Gain1, 2		0.05	0.15	%
Channel gain difference	ΔV_O	V_{IN}=-28.2dBV, Gain1, 2	-1	0	1	dB
Maximum output level	V_OM	THD=1%, Gain1, 2	7	8.5		dBV
Output noise level	VNO	Rg=1kΩ, JIS-A filter, Gain1		-89	-85	dBV
Mute attenuation value	MU	V_{IN}=-18.2dBV		-91	-80	dB
Input switch cross-talk	CT	V_{IN}=-18.2dBV		-75	-68	dB
Normal output (LINE IN to NORMAL OUT), EE mode, f=1kHz						
Output level for Normal	V_ONOR	V_{IN}=-28.2dBV	-22.5	-21.5	-20.5	dBV
RFC output (NORMAL IN to RFC OUT), f=1kHz						
Output level	V_OR	V_{IN}=-21.2dBV, G2D4D3:10	-11.0	-9.5	-8.0	dBV
Output distortion	THDR	V_{IN}=-21.2dBV, G2D4D3:10		0.05	0.2	%
ALC level (1)	V_OAR1	VIN=-11.2dBV, G2D4D3:10	-7.0	-5.5	-4.0	dBv
ALC distortion (1)	THDAR1	V_{IN}=-11.2dBV, G2D4D3:10		0.3	0.5	%
ALC level (2)	V_OAR2	V_{IN}= -11.2dBV, G2D4D3:10, G4D2:1	-3.0	-1.5	0	dBv
ALC distortion (2)	THDAR2	V_{IN}= -11.2dBV, G2D4D3:10, G4D2:1		0.1	0.3	%
LINE AMP (NORMAL IN to LINE OUT), EE mode, f=1kHz, Left channel and Right channel						
Line amp gain	GVL	V_{IN}=-21dBV, Gain=1 mode (G2D4:0)	11	12	13	dB
REC system (LINE IN to VCO OUT), f=1kHz						
Free-running frequency L	f_OL	Input no signal	1.294	1.300	1.306	MHz
Free-running frequency R	f_OR	Input no signal	1.694	1.700	1.706	MHz
Standard frequency deviation L&R	DEV	V_{IN}=-28.2dBV	±46	±50	±54	kHz
Carrier output level Lch	VfoL	Non modulation	380	440	500	mVp-p
FM R/Lch MIX ratio 1	MIX1	Non modulation, VfoR/VfoL, G3D7D6;01	7.1	7.6	8.1	dB
FM R/Lch MIX ratio 2	MIX2	Non modulation, VfoR/VfoL, G3D7D6;00	8.1	8.6	9.1	dB
FM R/Lch MIX ratio 3	MIX3	Non modulation, VfoR/VfoL, G3D7D6;10	9.1	9.6	10.1	dB
FM R/Lch MIX ratio 4	MIX4	Non modulation, VfoR/VfoL, G3D7D6;11	10.1	10.6	11.1	dB

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FM modulation system (PB FM IN to LINE OUT), PB mode, FM standard input=300mVp-p(R/Lch ratio=1:1)						
Output level Lch	V_OPL	fc=1.3±50kHz, fm=1kHz, Gain=1 (G3D4:0)	-11	-9	-7	dBV
Output level Rch	V_OPR	fc=1.7MHz±50kHz, fm=1kHz, Gain=1 (G3D4:0)	-11	-9	-7	dBV
Output level difference	VDEM	fc=1.3MHz±50kHz, fm=1kHz fc=1.7MHz±50kHz, fm=1kHz Lch-Rch, Gain=1 (G3D4:0)	-1.5	0	1.5	dB
Output distortion Lch	THDPL	fc=1.3MHz±50kHz, fm=1kHz,DIN		0.3	0.5	%
Output distortion Rch	THDPR	fc=1.7MHz±50kHz, fm=1kHz, DIN		0.3	0.5	%
DO detector / **HiFi detector** PB mode(DO DET : fc=1.3MHz / HiFi DET : fc=1.3MHz & 1.7MHz),						
DO detection level	DOC	The ratio with Standard input pin 31=300mVp-p		-26	-23	dB
DO detection hysteresis	DOCH		0.5	3	5	dB
HiFi recovery delay time	HIDEL	The delay time that is changed from NORMAL to HiFi.	110	125	140	ms
HiFi detection DC output 1	VTRS1	Pin 34 input level=100mVp-p	2.1	2.6	3.1	V
HiFi detection DC output 2	VTRS2	Pin 34 input level=300mVp-p	3.3	3.8	4.3	V
HiFi detection DC output 3	VTRS3	Pin 34 input level=1Vp-p	4.3	4.8	5.3	V
NORMAL detection DC output	NORDC	Pin 34 input level=0mVp-p			0.4	V
Hold pulse occurrence PB mode						
Hold pulse delay time	HPD	AUDIO HEAD PULSE IN	0.8	1.0	1.2	µs
Hold pulse width	HPW	AUDIO HEAD PULSE IN	7.2	9.0	10.8	µs
Band pass filter PB mode, PB IN = 150mVp-p(R/L MIX ratio 1:1)						
1.3MHz BPF monitor level	V13	34pin input level =60mVp-p,G2D2D1:01	80	100	120	mVp-p
1.7MHz BPF monitor level	V17	34pin input level =60mVp-p,G2D2D1:01	60	80	100	mVp-p
1.3MHz BPF frequency characteristics 1	L115N	Level difference between 1.15M/1.3MHz G2D2D1;01	-13	-5		dB
1.3MHz BPF frequency characteristics 2	L145N	Level difference between 1.45M/1.3MHz G2D2D1;01	-13	-5		dB
1.3MHz BPF frequency characteristics 3	L155N	Level difference between 1.55M/1.3MHz G2D2D1;01		-20	-10	dB
1.7MHz BPF frequency characteristics 1	R145N	Level difference between 1.45M/1.7MHz G2D2D1;10		-15	-5	dB
1.7MHz BPF frequency characteristics 2	R155N	Level difference between 1.55M/1.7MHz G2D2D1;10	-9	-3		dB
1.7MHz BPF frequency characteristics 3	R185N	Level difference between 1.85M/1.7MHz G2D2D1;10	-9	-3		dB
Playback head amp system (PB HEAD AMP IN to OUT), PB mode						
Voltage gain	GVP	V_{IN}=100µVp-p, f=1.5MHz, CH1&2	66	69	72	dB
Voltage gain difference CH1/CH2	ΔGVP		-2	0	2	dB
EP gain boost value	ΔGEP	V_{IN}=100µVp-p, f=1.5MHz	1	2	3.2	dB
Frequency characteristics	ΔfP	V_{IN}=100µVp-p, f=1.8M/1.0MHz, CH1&2	-3	-1	1	dB
Input conversion noise voltage	VNINP	The value(1 / GVP) of 1.1MHz LPF output level		1.7	2	µVrms
Output DC offset	ΔV_ODC	CH1/CH2	-30	0	30	mV
REC AMP system REC mode, The external resistor at pin 28 = 2.7kΩ						
REC current	I_OR	Inflow current at pin 26	34	37	40	mA
Cross modulation distortion 0.4MHz component	CMDO4	Rch carrier level standard		-48	-40	dB
Cross modulation distortion 0.9MHz component	CMDO9	Rch carrier level standard		-55	-40	dB
current ratio +2dB	I_OR+2dB	P23:0V,G4D6D5:01	1.6	2.0	2.4	dB
current ratio -2dB	I_OR-2dB	P23:0V,G4D6D5:10	-2.4	-2.0	-1.6	dB
Mute attenuation value	I_ORMU	REC MUTE ON(pin 17:5V)			-40	dB

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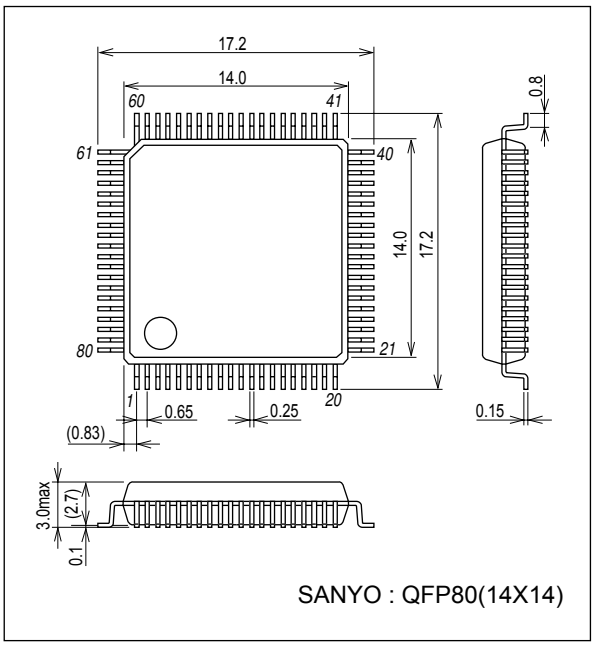
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SIF system (SIF IN to SIF OUT), EE/REC mode						
Input level	V_ILIM	fc=4.5MHz	80	90	100	dBμV
TV multiplex demodulation system EE/REC mode, L/Rch, LINE AMP GAIN(1) Deviation of SIF input MONO: 100%→±25kHz (fm=400Hz) Pre-Emphasis ON						
MONO output level	V_OMN	fm=1kHz,100% modulation, Pre-emphasis OFF	-7	-5.5	-4	dBV
Output L/R level difference	ΔV_OMN	fm=1kHz,100% modulation, Pre-emphasis OFF	-1.5	0	1.5	dB
MONO distortion	THDM	fm=1kHz,100% modulation, Pre-emphasis OFF		0.2	0.5	%
MONO frequency characteristics 1	FCM1	fm=10kHz,100% modulation, Pre-emphasis OFF	-17	-14	-11	dB
MONO S/N	SNM	Non modulation,15kHz LPF	50			dB
TEREO output level	V_OST	fm=1kHz, 100% modulation, 15kHz LPF	-7.5	-5.5	-3.5	dBV
STEREO distortion	THDS	fm=1kHz, 100% modulation, 15kHz LPF		0.3	1.0	%
STEREO S/N	SNS	Sub carrier (Non modulation) + Cue(Stereo) ,15kHz LPF	45			dB
MAIN output level	VOMA	fm=1kHz, 100% modulation, Cue(Bilingual), 15kHz LPF	-7	-5.5	-4	dB
MAIN distortion	THDMA	fm=1kHz, 100% modulation, Cue(Bilingual), 15kHz LPF		0.2	0.5	%
MAIN S/N	SNMA	Sub Carrier(Non modulation) + Cue(Bilingual), 15kHz LPF	50			dB
SUB output level	V_OSU	fm=1kHz, 100% modulation, Cue(Bilingual), 15kHz LPF	-7.5	-5.5	-3.5	dBV
SUB S/N	SNSU	Sub carrier (Non modulation) + Cue(Bilingual) ,15kHz LPF	45			dB
SUB frequency characteristics	FCSU2	fm=10kHz, 60% modulation, Cue(Bilingual), 15kHz LPF	-20	-16	-12	dB
SUB distortion	THDSU	fm=1kHz, 100% modulation, Cue(Bilingual), 15kHz LPF		0.5	2.0	%
STEREO separation L→R	SEPR	L:fm=1kHz, 60%modulation, Cue(Stereo), 15kHz-LPF	25	30		dB
STEREO separation R→L	SEPL	R:fm=1kHz, 60%modulation, Cue(Stereo), 15kHz-LPF	25	30		dB
Cross-talk MAIN→SUB	CTSUB	Main:fm=1kHz, 100%modulation, Cue(Bilingual), 15kHz LPF	35	50		dB
Cross-talk SUB→MAIN	CTMA	Sub:fm=1kHz, 100%modulation, Cue(Bilingual), 15kHz LPF	45	55		dB
Stay behind carrier level (S)	CLSU	Main=0%, Sub:0%(Carrier), Cue(Bilingual)		-55	-45	dBV
Stay behind carrier level (M)	CLMA	Main=0%, Sub:0%(Carrier), Cue(Bilingual)		-55	-45	dBV
Mode detection volt(mono)	VLEDM	Input=Monaural signal	0.7	1.0	1.3	V
Mode detection volt(st)	VLEDM	Input=Stereo signal	1.7	2.0	2.3	V
Mode detection volt(bil)	VLEDM	Input=Bilingual signal	2.7	3.0	3.3	V
Just clock output High volt	VJCH	f=400Hz(mono),40%Mod.	4.0			V
Just clock output Low volt	VJCL	f=400Hz(mono),10%Mod.			1.0	V

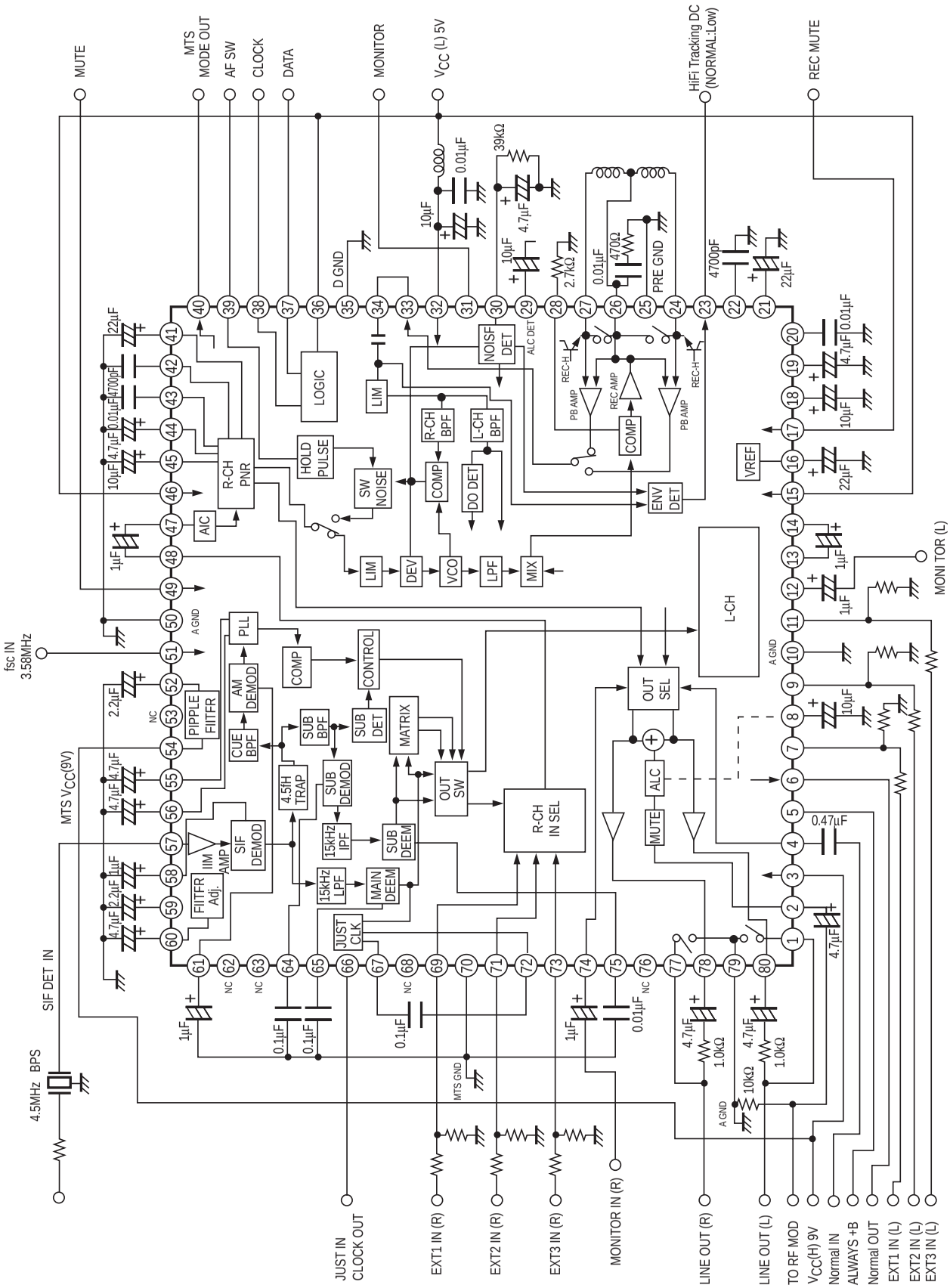
Package Dimensions

unit : mm (typ)

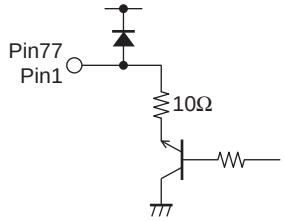
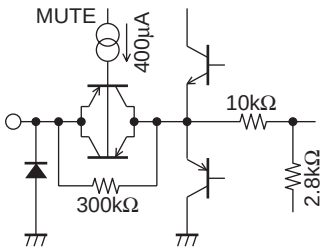
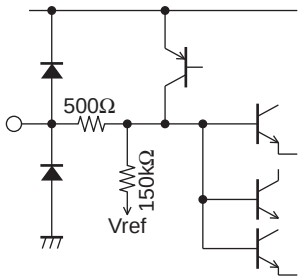
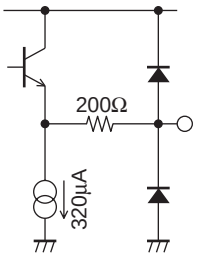
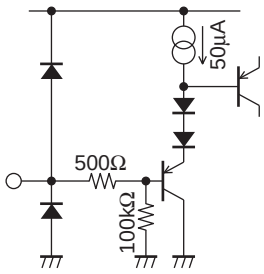
3255



Block Diagram



Pin Description

Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
1 77	Line Mute terminal(L) Line Mute terminal(R)		When the power supply V_{CC} is on, the switch of Pin 77 and Pin 1 is turned to ON to reduce the line out noise. In this case, it is necessary to apply 5 fixed DC to Pin 5.	
2	Output terminal for RF modulator	DC; 4.2V	Output terminal for RF modulator. ALC level can be settled to -1dBV and OFF by serial control.	
3	V_{CC} 9V		Power supply of Line Out.	
5	ALWAYS VCC		Power supply for the noise elimination mute control when power is on.	
15	V_{CC} 5V(Lch)		5V power supply of Lch.	
32	V_{CC} 5V		5V power supply of HEAD AMP.	
36	Power supply for Logic		Power supply for Logic.	
46	V_{CC} 5V(Rch)		5V power supply of Rch.	
54	9V power supply for MTS		9V power supply of MTS.	
4	NORMAL input terminal	DC; 2.5V AC; -28.2dBV	NORMAL IC output signal is entered and output to Line Out through output changeover. G4D7/0:0dB 1:3dB	
6	NORMAL output terminal	DC; 2.5V AC; -21.2dBv	This is connected to input of NORMAL AUDIO IC.	
7 9 11 69 71 73	Audio input terminal EXT1_IN(L) EXT2_IN(L) EXT3_IN(L) EXT1_IN(R) EXT2_IN(R) EXT3_IN(R)	DC ; 0V AC; -28.2dBV	Audio input terminal.	

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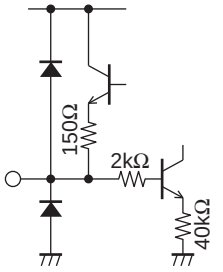
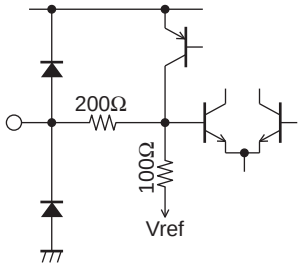
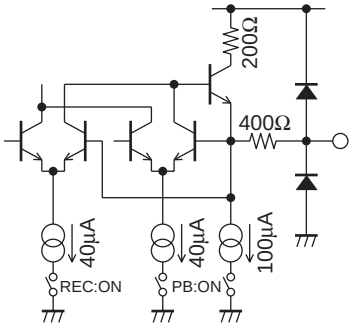
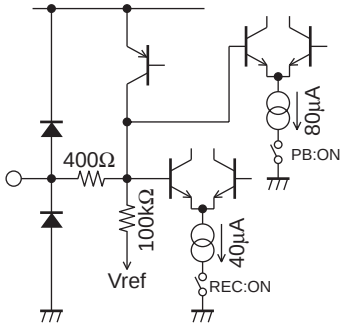
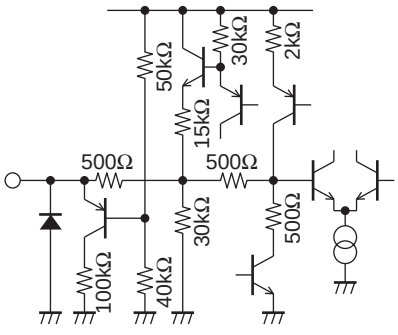
Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
8	ALC detection terminal for RF converter	DC;	This is ALC detector terminal for RF converter and always ready for operation.	
10 25 35 50 70 79	L-GND HEADAMP-GND LOGIC-GND R-GND MTS-GND AUDIO-GND			
12 74	Monitor input terminal(L) Monitor input terminal(R)	DC ; 2.5V	Monitor input terminal	
13 48	Input changeover switch output(L) Input changeover switch output(L)	DC ; 2.2V AC; -21.2dBv	PB/REC switch output to transform REC and PB signals into DC through a coupling capacitor.	
14 47	ALC input terminal(L) ALC input terminal(R)	DC; 2.5V AC; -21dBv	ALC input terminal after passing through a coupling capacitor.	
16	1/2 V_{CC} terminal	DC; 2.5V	1/2 V_{CC} terminal.	

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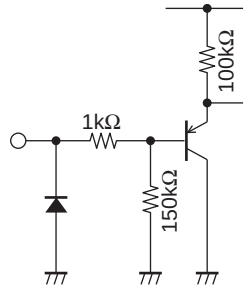
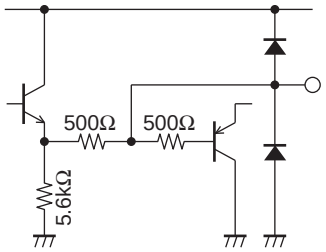
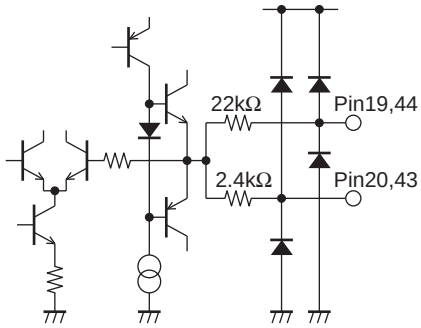
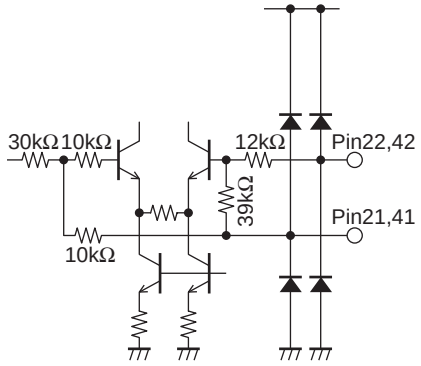
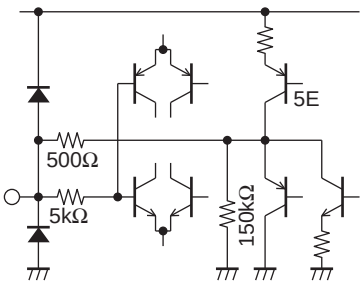
Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
17	REC mute terminal	DC; Unsettled	Two levels control terminal. Hi ; 3.0V to Vcc Low ; 0V to 1.5V	
18 45	NR waiting DET terminal(L) NR waiting DET terminal(R)		Terminal for waiting detector. The recommended external capacity is 10μF.	
19 44 20 43	NR waiting filter terminal1(L) NR waiting filter terminal1(R) NR waiting filter terminal2(L) NR waiting filter terminal2(R)	DC; 2.5V AC;	(Pin 19,Pin 44)between GND;4.7μF (Pin 20,Pin 43)between GND;0.01μF	
21 22 42 41	CCA reference terminal(L) NR emphasis terminal(L) NR emphasis terminal(R) CCA reference terminal(R)	DC; 2.5V	By connecting 22μF between Pin 21, Pin 41 and GND, 4700pF between Pin 22, Pin 42 and GND, form the NR emphasis.	
23	HiFi/Nor selecting terminal (PB) (2)Monitor control terminal at Pin 34 (EE)		In PB mode, Pin 23 becomes “TRACKING_DC” when inputting HiFi audio signal and becomes “L” when inputting Normal signal. In EE mode, this is used as the terminal for monitor control of Pin 34. Low(0 to 0.8V) ; VCO MIX Middle(1.4V to 3.6V) ; Lch VCO High(4.2V to V_{CC}) ; Rch VCO	

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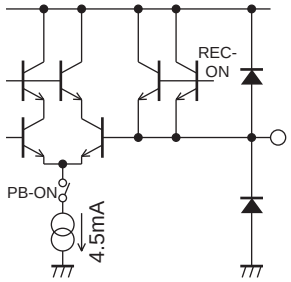
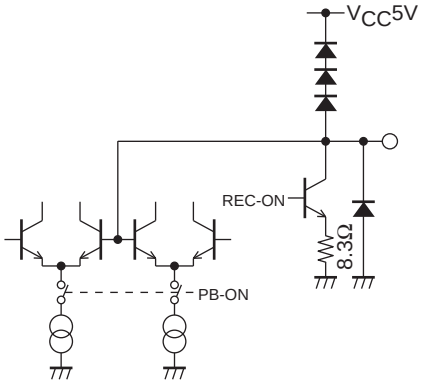
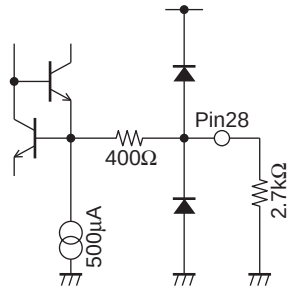
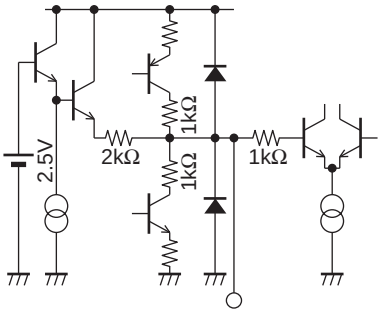
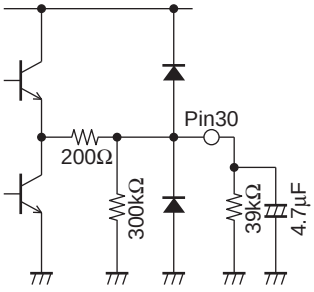
Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
24 27	HEAD AMP input terminal (Hch) HEAD AMP input terminal (Lch)	DC PB; 2.0V REC; 4.1V	HEAD AMP inputs (CH1 and CH2) is PB mode.	
26	REC CURRENT AMP output terminal		CURRENT AMP output in REC mode. Common input terminal in PB mode.	
28	CURRENT AMP ADJUST terminal	DC; 2.4V	Terminal for adjusting the recording current.	
29	ALC detection terminal		This is ALC detector terminal. ALC becomes through switch when Pin29 pull up V_{CC}.	
30	HiFi/NORMAL detection terminal		This terminal is for detecting demodulation noise and output which has passed through the primary HPF(fc=140kHz).	

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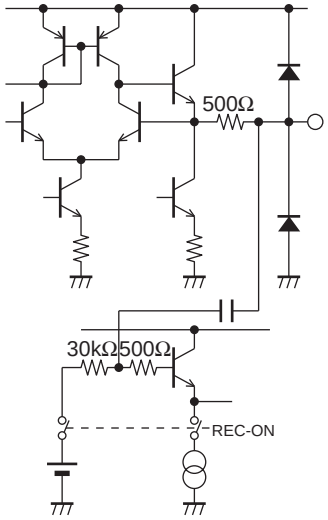
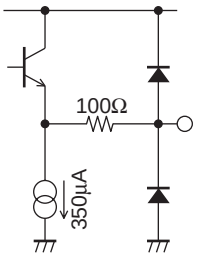
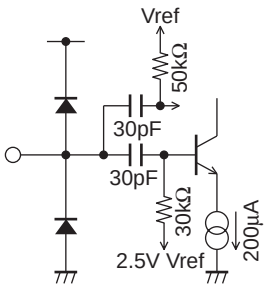
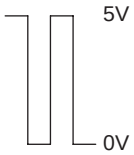
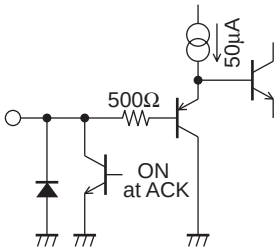
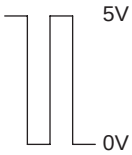
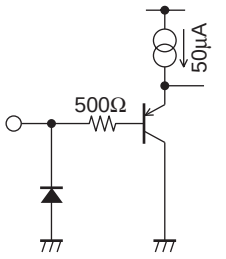
Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
31	Monitor terminal	DC ; 2.5V	FM MIX output(Low), Lch VCO(middle), Rch VCO(High) can be monitored by controlling Pin 23 in REC mode. HOLD and DO pulses can be monitored by Pin 17 in PB mode. BPF of Lch and Rch can be monitored by serial control in PB mode.	
33	PB AMP output	DC; 2.5V	Output of HEAD AMP in PB mode.	
34	PB FM input terminal	DC; Unsettled AC; 350mVp-p (L/R MIX)	Input pin of FM in PB mode.	
37	Serial data input terminal		Hi ; 3.5V to 5V Low ; 0V to 1.5V	
38	CLK input terminal		Hi ; 3.5V to 5V Low ; 0V to 1.5V	

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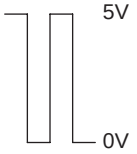
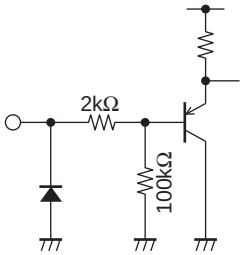
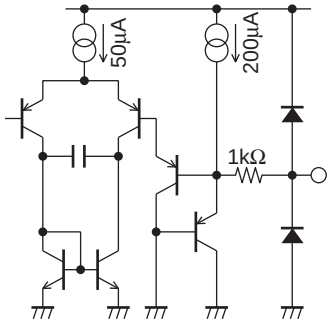
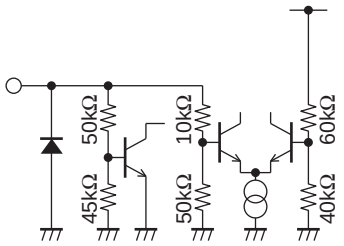
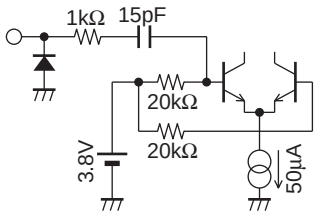
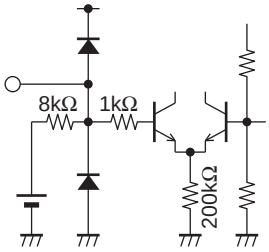
Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
39	AF SW pulse input terminal	50Hz/60Hz 	Input terminal of AF SW pulse. Hi ; 3.5V to 5V Low ; 0V to 1.5V	
40	MTS MODE OUT	DC;	Detection result output for M.T.S. signal. BILINGAL : 3.0V STEREO : 2.0V MONO : 1.0V	
49	MUTE control terminal	DC;	Mute control terminal.	
51	FSC IN		Input terminal for FSC (3.58MHz).	
52	PCREG76	DC; 1.2V	Band gap power supply terminal of M.T.S block. This power supply does not operate in PB mode.	
53 62 63 68 76	NC pin			

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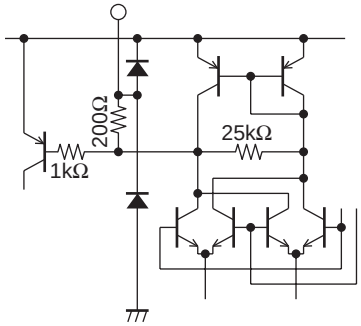
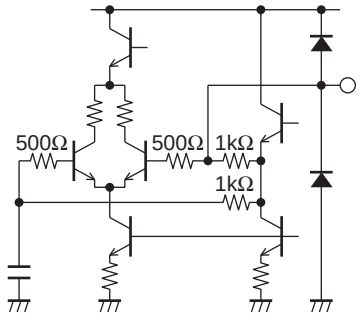
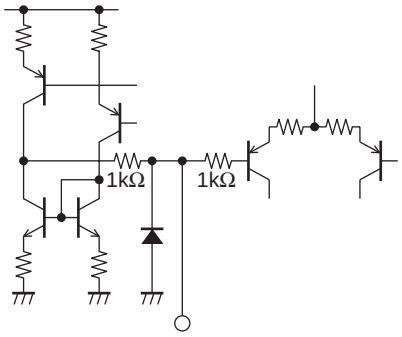
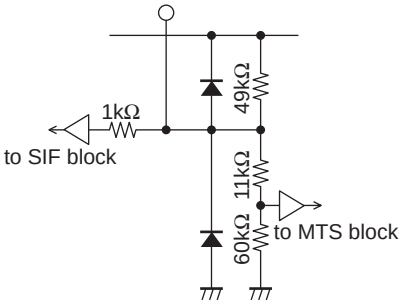
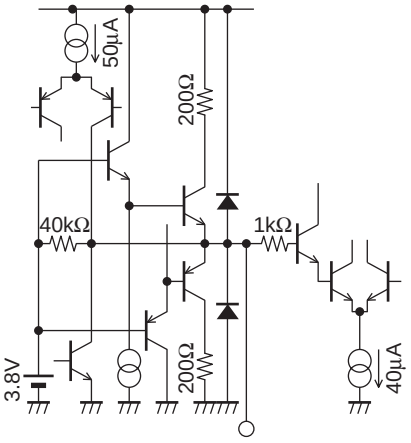
Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
55	PHASE COMPARATOR(BIL.)		This detection pin becomes High(4.0V or more) because of detecting BIL, when BIL signal is input.	
56	PHASE COMPARATOR(ST.)		This detection pin becomes High(4.0V or more) because of detecting ST, when ST signal is input.	
57	SIF INPUT		Input terminal for SIF. The input impedance is about 1kΩ. Be care for about pattern layout of the input circuit, because of causing buzz-beat and buzz by leaking noise signal into the input terminal.(The noise signal depending on sound is particularly video signal and chroma signal and so on. VIF carrier becomes noise signal.) Composite signal of MTS can be input by adding 5V to this terminal directly.(For test)	
58	FM FILTER		Filter terminal for making stable DC voltage of FM detection output in SIF part. Normally, use a condenser of 1μF. Increase the capacity value with concerning frequency characteristics of low level. This terminal becomes composite signal input terminal of MTS by changing to 5V at Pin57.	
59	REG FILT	DC; 4.5V	Filter terminal of reference voltage source	
60	FILTER AUTO ADJ	DC; 3.8V	Loop filter terminal for automatic adjusting.	

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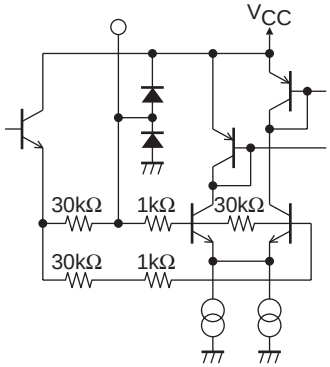
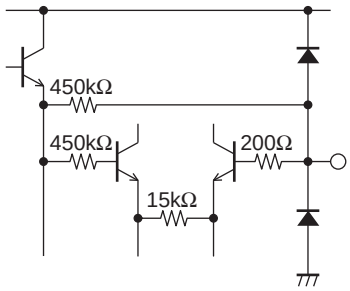
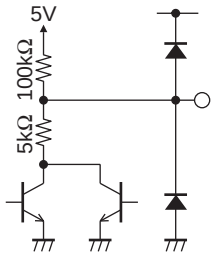
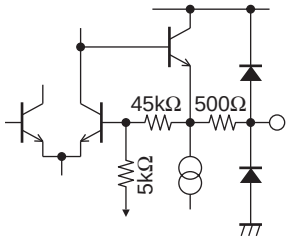
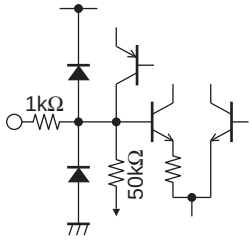
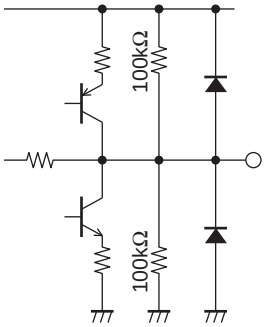
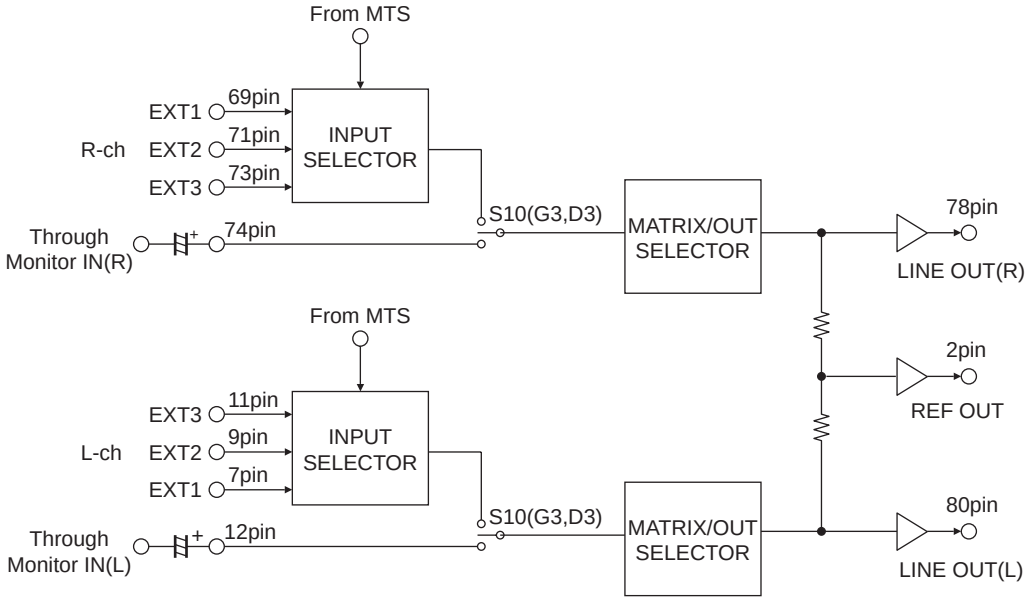
Pin No.	Pin Function Name	DC voltage / AC level	Function	Equivalent circuit
61	AM DETECTOR		Reference terminal of AM detection.	
64 65 75	DC FILTER	DC ; 3.8V	Absorbing the DC offset of signal line by external capacity.	
66	JUST CLOCK OUT		Rectangle wave output for JUST CLOCK.	
67	JUST CLOCK AMP OUT	DC ; 3.8V	20dB amplifire output for JUST CLOCK.	
72	COMPARATOR Input Terminal	DC ; 3.8V	Comparator input for JUST CLOCK.	
78 80	Line Out(R) terminal Line Out(L) terminal	DC; 4.15V		

Through Monitor Signal Path Description

1. The Through Monitor signal path is as follows.
   When Serial Data G3D3 is set to "1", signal is output to LINE OUT and REC OUT.
2. reference input signal level.
   EXT1,2,3 pin : -28.2dBV
   Through Monitor pin : -21.2dbV



Through Monitor Switch Mode Table

	Through Monitor G3D3	Auto HiFi Det G2D6	HiFi/Mix/Nor G2D4D3	Line Out Lch	Line Out Rch	RFC Out
EE	0	-	0 0	Insel L	Insel R	Insel Mix
	1	-	0 0	Monitor L	Monitor R	Monitor Mix
PB	0	0	0 0	PB L	PB R	PB Mix
(HiFi Tape)	0	1	0 0	PB L	PB R	PB Mix
	1	0	0 0	Monitor L	Monitor R	Monitor Mix
	1	1	0 0	Monitor L	Monitor R	Monitor Mix
PB	0	0	0 0	Normal	Normal	Normal
(Nor. Tape)	0	1	0 0	Noise	Noise	Noise
	1	0	0 0	Normal	Normal	Normal
	1	1	0 0	Monitor L	Monitor R	Monitor Mix

* When output Monitor signal to RFC OUT at Normal Tape replayed (G3D3:1), set G2D6 (HiFi auto Distinction) to 1 and select G2D4D3:0 (HiFi).

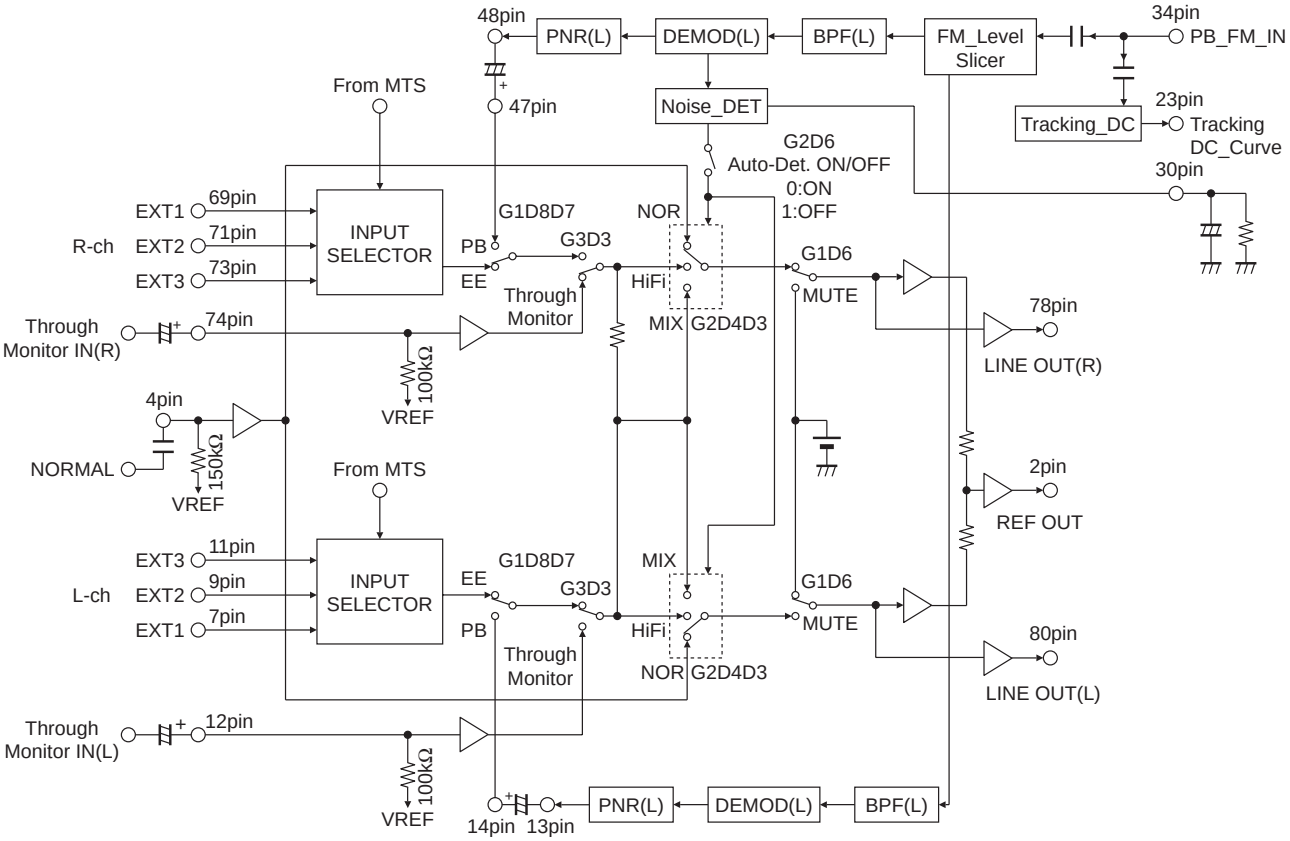
Through Monitor Signal Path Supplementary Explanation

When output Monitor signal to RFC OUT at the time of replay (especially Normal Tape), care must be taken as described below.

This IC has a function to auto distinguish HiFi and Normal by the presence or absence of Rch envelope, which can be turned ON/OFF by using G2D6.

When output Monitor signal to REF OUT at the time of replay, turn off this function and make the following settings.

1) G2D6:1 (Auto detection OFF)
2) G3D3:1 (Select Through Monitor)
3) G2D4D3:00 (Select HiFi) Refer to the Through Monitor Switch Table above for each switch mode.



Input Selecting Switch Mode Table (Switch output signal)

Sub address	0 1					0 2		HiFi Lch Input	HiFi Rch Output	NORMAL OUT	Reference
Data byte	D8	D7	D3	D2	D1	D8	D7				
1	0	0	0	0	1	0	0	TU L	TU R	TU L+TU R	
2	0	0	0	1	0	0	0	EXT1 L	EXT1 R	EXT1 L+EXT1 R	
3	0	0	1	0	0	0	0	EXT2 L	EXT2 R	EXT2 L+EXT2 R	
4	0	0	1	1	0	0	0	EXT3 L	EXT3 R	EXT3 L+EXT3 R	
5	0	0	0	0	1	0	1	TU L	TU R	TU L	
6	0	0	0	1	0	0	1	EXT1 L	EXT1 R	EXT1 L	
7	0	0	1	0	0	0	1	EXT2 L	EXT2 R	EXT2 L	
8	0	0	1	1	0	0	1	EXT3 L	EXT3 R	EXT3 L	
9	0	0	0	0	1	1	0	TU L	TU R	TUR	
10	0	0	0	1	0	1	0	EXT1 L	EXT1 R		
11	0	0	1	0	0	1	0	EXT2 L	EXT2 R		
12	0	0	1	1	0	1	0	EXT3 L	EXT3 R		
13	0	1	0	0	0	0	0	PB L	PB R		
14	0	1	0	1	0	0	0	PB L	PB R	EXT1 L+EXT1 R	
15	0	1	1	0	0	0	0	PB L	PB R	EXT2 L+EXT2 R	
16	0	1	1	1	0	0	0	PB L	PB R	EXT3 L+EXT3 R	
17	0	1	0	0	0	0	1	PB L	PB R		
18	0	1	0	1	0	0	1	PB L	PB R	EXT1 L	
19	0	1	1	0	0	0	1	PB L	PB R	EXT2 L	
20	0	1	1	1	0	0	1	PB L	PB R	EXT3 L	
21	0	1	0	0	0	1	0	PB L	PB R		
22	0	1	0	1	0	1	0	PB L	PB R		
23	0	1	1	0	0	1	0	PB L	PB R		
24	0	1	1	1	1	1	0	PB L	PB R		
25	0	1	0	0	0	1	0	PB L	PB R		
26	1	1	*	*	*	*	*	PB L	PB R	PB L+PB R	Audio-dubbing correspond

NOTE : * is option.(1 or 0)

Input selecting switch mode table (Switch output signal)

Sub address	0 1				0 2		HiFi(80Pin Lch Output	HiFi(78Pin) Rch Output	NORMAL OUT (6Pin)	Reference
Data byte	D8	D7	D3	D2	D8	D7				
1	0	0	0	0	0	0	TU L	TU R	TU L+TU R	
2	0	0	0	1	0	0	EXT1 L	EXT1 R	EXT1 L+EXT1 R	
3	0	0	1	0	0	0	EXT2 L	EXT2 R	EXT2 L+EXT2 R	
4	0	0	1	1	0	0	EXT3 L	EXT3 R	EXT3 L+EXT3 R	
5	0	0	0	0	0	1	TU L	TU R	TU L	
6	0	0	0	1	0	1	EXT1 L	EXT1 R	EXT1 L	
7	0	0	1	0	0	1	EXT2 L	EXT2 R	EXT2 L	
8	0	0	1	1	0	1	EXT3 L	EXT3 R	EXT3 L	
9	0	0	0	0	1	0	TU L	TU R	TU R	
10	0	0	0	1	1	0	EXT1 L	EXT1 R	TU R	
11	0	0	1	0	1	0	EXT2 L	EXT2 R	TU R	
12	0	0	1	1	1	0	EXT3 L	EXT3 R	TU R	
13	0	1	0	0	0	0	PB L	PB R	TU L+TU R	
14	0	1	0	1	0	0	PB L	PB R	EXT1 L+EXT1 R	
15	0	1	1	0	0	0	PB L	PB R	EXT2 L+EXT2 R	
16	0	1	1	1	0	1	PB L	PB R	EXT3 L	
17	0	1	0	0	0	1	PB L	PB R	TU L	
18	0	1	0	1	0	1	PB L	PB R	EXT1 L	
19	0	1	1	0	0	1	PB L	PB R	EXT2 L	
20	0	1	1	1	0	1	PB L	PB R	EXT3 L	
21	0	1	0	0	1	0	PB L	PB R	TU R	
22	0	1	0	1	1	0	PB L	PB R	-	
23	0	1	1	0	1	0	PB L	PB R	-	
24	0	1	1	1	1	0	PB L	PB R	-	
25	1	0	*	*	*	*	PB L	PB R	PB L+PB R	Audio-dubbing correspond

NOTE : * is option.(1 or 0)

Serial data specification (I^2C BUS communication)

Address	Data Byte (An underline is the first condition.)							
	MSB D8	D7	D6	D5	D4	D3	D2	LSB D1
(01) 00000001	EE/PB/Audio-dubbing 00:EE 01:PB 10:Audio-dubbing		LINE OUT MUTE 0:OFF 1:ON	Power Save 0:ON 1:OFF	EE/REC 0:EE 1:REC	Input Source Select 001:TUNER 010:EXT1 100:EXT2 110:EXT3		
(02) 00000010	Normal Input Source Select 00:L/R MIX 01:Lch 10:TU(R)		Auto_HiFi Det 0:ON 1:OFF	Just In Clock 0:OFF 1:ON	OUTPUT MODE SELECT 00:HiFi 01:MIX (HiFi+NOR) 10:NORMAL		OUTPUT SOURCE SELECT 00:STEREO 01:L-ch 10:R-ch	
(03) 00000011	VCO carrier (MHz) 0:1.3/1.7 1:1.4/1.8	REC FM MIX 00:9dB 01:8dB 10:10dB 11:11dB		DO ON/OFF 0:ON 1:OFF	LINE OUT signal level 0:-9dBV 1:-8dBV	THROUGH MONITOR 0:OFF 1:ON	HiFi DET LEVEL SELECT 0:TYP 1:+10%	HiFi DET LEVEL SELECT 0:TYP 1:-10%
(04) 00000100	Fixed 0	Normal Input gain 0:0dB 1:3dB	REC current level select 00:CENTER 01:-1.5dB 10:-5.5dB		NORMAL OUT MUTE 0:OFF 1:ON	Fixed 0	RF MOD ALC level 0:-5dBV 1:-1dBV	INPUT ALC 0:ON 1:OFF
(05) 00000101	MULTIPLEX mode select 00:BILINGUAL 01:MAIN 10:SUB		Forced MONO 0:OFF 1:ON	Fixed 0	EP/SP 0:SP 1:EP	Fixed 0	Fixed 0	Fixed 0
(06) 00000110	Fixed 0 / Use in investigating the shipment.							
(07) 00000111	Fixed 0 / Use in investigating the shipment.							

Note: Address 00000110 and 00000111 are used in investigating the shipment, please send “0” data to all bits at refreshing the data.

I²C BUS serial interface specification

(1) DATA TRANSFER MANUAL

This IC adopts control method(I²C-BUS) with serial data, and controlled by two terminals which called SCL(serial clock) and SDA (serial data).At first, set up the condition of starting data transfer*1, and after that, input 8 bit data to SDA terminal with synchronized SCL terminal clock. The order of transferring is first, MSB (the Most Scale of Bit),and save the order. The 9th bit takes ACK (ACKnowledge) period, during SCL terminal takes "H", this IC pull down the SDA terminal. After transferred the necessary data, two terminals lead to set up and of data transfer stop condition*2, thus the transfer comes to close.

As a part of transfer data write down to internal memory (V latch system), internal control doesn't change just after the transfer.

*1 Defined by SCL rise down SDA during 'H' period.

*2 Defined by SCL rise up SDA during 'H' period.

(2) TRANSFER DATA FORMAT

After transfer start condition, transfers slave address(1110100*) to SDA terminal, next, sub address(0000****), control data*3, then, stop condition(See figure 1). And this LSI have a auto address increment function, then, next of slave address transfer, transfer sub address(n)*4, group (n) data, after that, group (n+1) and so on.

Data works with all of the bit, transfer the stop condition before stop 8bit transfer, and to stop transfer, it will be canceled only the data of group.

*3 There are 1 to 5 groups.

*4 Pointed date by sub address becomes group No. of next control data.

Fig.1 DATA STRUCTURE "WRITE" mode

START Condition	Slave Address	R/$\overline{W}$ *5	ACK	Sub Address(n)	ACK	Control data(n)	ACK	control data(n+1)	ACK	·····	STOP condition

*5 It is called R/W bit.

data-1 means data for group-1, data-2 means data for group-2.

(3) INITIALIZE

This IC is initialized for circuit protection.

The initialization period is decided Pin 16 capacity value by internal impedance 15kΩ, and shown with $t = -CR \times Ln(0.2)$. Data cannot be accepted for this period.

$t = 530ms$ at $C = 22\mu F$, In this case, Please transmit data in consideration of the uneven after about 700ms.

(4) SERIAL INPUT SIGNAL FORMAT

Parameter	Symbol	min	max	unit
LOW level input voltage	VIL	-0.5	1.5	V
HIGH level input voltage	VIH	3.0	5.5	V
LOW level output current	IOL	-	3.0	mA
SCL clock frequency	fSCL	0	100	kHz
Set-up time for a repeated START condition	tSU:STA	4.7		μs
Hold time START condition. After this period, the first clock pulse is generated	tHD:STA	4.0		μs
LOW period of the SCL clock	tLOW	4.7		μs
Rise time of both SDA and SDL signals	tR	0	1.0	μs
HIGH period of the SCL clock	tHIGH	4.0	-	μs
Fall time of both SDA and SDL signals	tF	0	1.0	μs
Data hold time:	tHD:DAT	0	-	μs
Data set-up time	tSU:DAT	250	-	ns
Set-up time for STOP condition	tSU:STO	4.0	-	μs
BUS free time between a STOP and START condition	tBUF	4.7	-	μs

(5) Definition of timing