



# CCB LV23015T

Monolithic Linear IC

ON Semiconductor®

<http://onsemi.com>

## For Mini Component, receiver 1-chip Tuner IC Incorporating PLL

### Overview

The LV23015T is a Single-chip tuner IC with built-in PLL for mini component, receiver.

### Function

- AM tuner
- FM tuner
- MPX stereo decoder
- PLL frequency synthesizer

### Specifications

**Absolute Maximum Ratings** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max	V <sub>CC</sub>	7.0	V
Maximum input voltage	V <sub>IN1</sub> max	CE, CI, CL	7.0	V
	V <sub>IN2</sub> max	XIN	*1 V <sub>reg2</sub> +0.3	V
Maximum output voltage	V <sub>O1</sub> max	DO	7.0	V
	V <sub>O2</sub> max	XOUT, PD	V <sub>reg2</sub> +0.3	V
	V <sub>O3</sub> max	BO1, AOOUT	12.0	V
Allowable power dissipation	P <sub>d</sub> max	Ta ≤ 70°C *2	400	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

\*1 V<sub>reg2</sub> : 21 pin output voltage (Reference voltage of PLL) Reference value (3.0V±0.2V)

\*2 Specified board : 114.3mm×76.1mm×1.6mm, glass epoxy board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Operating Condition** at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V <sub>CC</sub>		5.0	V
Operating supply voltage range	V <sub>CC</sub> op		4.0 to 6.0	V

- CCB is ON Semiconductor® 's original format. All addresses are managed by ON Semiconductor® for this format.

- CCB is a registered trademark of Semiconductor Components Industries, LLC.

# LV23015T

## PLL block Allowable Operating Range at Ta = -20°C to +70°C, V<sub>SS</sub> = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage	V <sub>IH</sub>	CE, CL, DI	0.7V <sub>reg2</sub>		6.0	V
Input low level voltage	V <sub>IL</sub>	CE, CL, DI	0		0.3V <sub>reg2</sub>	V
Output voltage	V <sub>O1</sub>	DO	0		6.0	V
	V <sub>O2</sub>	BO1, AOUT	0		10	V
Operating frequency	f <sub>IN1</sub>	XIN ; V <sub>IN1</sub>		75		kHz
	f <sub>IN2</sub>	FMIN ; V <sub>IN2</sub>	10		160	MHz
	f <sub>IN3</sub>	AMIN (SNS = 1) ; V <sub>IN3</sub>	2		40	MHz
	f <sub>IN4</sub>	AMIN (SNS = 0) ; V <sub>IN4</sub>	0.5		10	MHz

Note : The XIN pin has extremely high input impedance, so that due care must be taken to prevent leakage.

## Operating Characteristics at Ta = 25°C, V<sub>CC</sub> = 5.0V, for the specified test circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>FM-FE characteristics</b> : fc = 98MHz, fm = 1kHz, 22.5kHzdev.						
3dB sensitivity	-3dB LS	60dB <sub>μV</sub> , 22.5kHzdev output reference, -3dB input		5	(12) Reference value	dB <sub>μV</sub> EMF
Practical sensitivity	QS	S/N = Input at S/N = 30dB		8	(15) Reference value	dB <sub>μV</sub> EMF
FM oscillation voltage	V <sub>Osc</sub>	No input, Pin 32 output, FET probe used	30	40	50	mVrms
<b>FM-EF stereo characteristics</b> : fc = 98MHz, fm = 1kHz, 75kHzdev, L+R = 90%, Pilot = 10%, V <sub>IN</sub> = 60dB <sub>μV</sub> EMF						
Stereo ON bandwidth	ST-BW	ST-ON frequency bandwidth, 18pin (DO) output		(300) Reference value		kHz
<b>FM-IF monaural characteristics</b> : fc = 10.7MHz, fm = 1kHz, 75kHzdev.						
Demodulation output	V <sub>O</sub>	100dB <sub>μV</sub> , 12pin output	750	1000	1200	mVrms
Channel balance	CB	100dB <sub>μV</sub> , 12pin output	-1.0	0	+1.0	dB
Signal to noise ratio	S/N	100dB <sub>μV</sub> , 12pin output	68	74		dB
AM suppression ratio	AMR	70dB <sub>μV</sub> input 12pin output reference, FM = no-mod, AM = 1kHz-30%mod, 12pin output	40	50		dB
Total harmonic distortion (monaural)	THD	100dB <sub>μV</sub> , 12pin output		0.6	1.5	%
3dB sensitivity	3dB LS	100dB <sub>μV</sub> , 75kHzdev output reference, -3dB input		38	44	dB <sub>μV</sub>
IF count sensitivity	IF-C3	SDC0 = 1, SDC1 = 0, 18pin (DO) output	39	46	53	dB <sub>μV</sub>
Mute attenuation	Mute-Att	100dB <sub>μV</sub> , 12pin output	60	70		dB
<b>FM-IF stereo characteristics</b> : fc = 10.7MHz, fm = 1kHz, Pilot = 10%						
Separation	SEP	100dB <sub>μV</sub> , L+R = 90%, L-mod, 12pin output/13pin output	28	38		dB
Total harmonic distortion (main)	THD-ST	100dB <sub>μV</sub> , L+R = 90%, Main-mod, 12pin output		1.0	2.0	%
Total harmonic distortion (L only)	THD-L	100dB <sub>μV</sub> , L+R = 90%, L-mod, 12pin output		0.6	2.0	%
Stereo ON sensitivity	ST-ON	100dB <sub>μV</sub> , L+R = 90%, Pin 18(DO) output	0.6		6.5	%
Capture range	CR	Pilot = 10% modulated, Pin 18(DO) output	-0.4		+0.4	kHz
<b>AM characteristics</b> : fc = 1000kHz, fm = 1kHz, 30%mod						
Detection output 1	V <sub>O1</sub>	23dB <sub>μV</sub> , 12pin output	60	120	240	mVrms
Detection output 2	V <sub>O2</sub>	80dB <sub>μV</sub> , 12pin output	220	330	440	mVrms
Signal to noise ratio 1	S/N1	23dB <sub>μV</sub> , 12pin output	15	20		dB
Signal to noise ratio 2	S/N2	80dB <sub>μV</sub> , 12pin output	47	54		dB
Total harmonic distortion	THD	80dB <sub>μV</sub> , 12pin output		1.2	2.5	%
IF count sensitivity	IF-C	18pin (DO) output	16	26	36	dB <sub>μV</sub>
Mute attenuation	Mute-Att	80dB <sub>μV</sub> , 12pin output	54	64		dB

Continued on next page.

# LV23015T

Continued from preceding page.

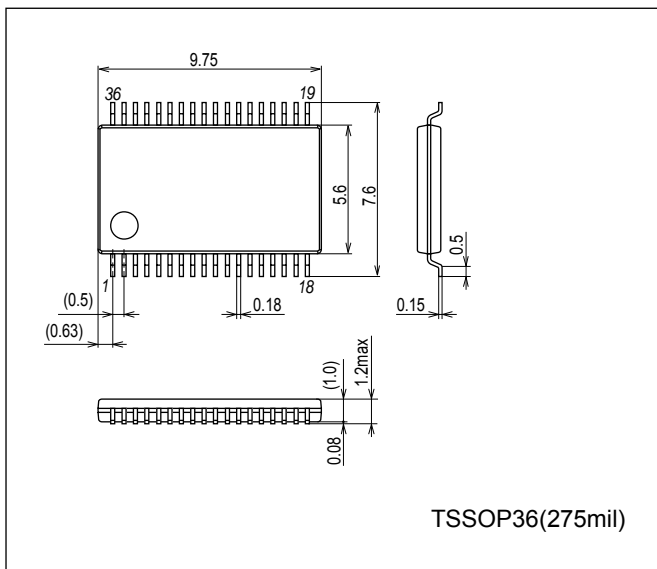
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Current drain</b>						
FM tuner	$I_{CCFM}$	No input at FM	25	35	45	mA
AM tuner	$I_{CCAM}$	No input at AM	11	22	33	mA
<b>PLL characteristics</b>						
Built-in return resistor	$R_f$	XIN		8		$M\Omega$
Built-in output resistor	$R_d$	XOUT		250		$k\Omega$
Hysteresis width	$V_{HIS}$	CE, CL, DI		$0.1V_{reg2}$		V
Output high level voltage	$V_{OH}$	PD ; $I_O = -1mA$	$V_{reg2}-1.0$			V
Output low level voltage	$V_{OL2}$	BO1 ; $I_O = 1mA$			0.25	V
		BO1 ; $I_O = 5mA$			1.25	V
	$V_{OL3}$	DO ; $I_O = 1mA$			0.25	V
	$V_{OL4}$	AOUT ; $I_O = 1mA, A_{IN} = 2.0V$			0.5	V
Input high level current	$I_{IH1}$	CE, CL, DI ; $V_I = 6.0V$			5.0	$\mu A$
	$I_{IH2}$	XIN ; $V_I = V_{DD}$	0.16		0.9	$\mu A$
	$I_{IH3}$	AIN ; $V_I = 6.0V$			200	nA
Input low level current	$I_{IL1}$	CE, CL, DI ; $V_I = 0V$			5.0	$\mu A$
	$I_{IL2}$	XIN ; $V_I = 0V$	0.16		0.9	$\mu A$
	$I_{IL3}$	AIN ; $V_I = 0V$			200	nA
Output off-leak current	$I_{OFF1}$	AOUT, BO1 ; $V_O = 10V$			5.0	$\mu A$
	$I_{OFF2}$	DO ; $V_O = 6.0V$			5.0	$\mu A$

Note : The reference value is calculated from more than one data and does not ensure conformance to the specifications. No data control by selection is implemented.

## Package Dimensions

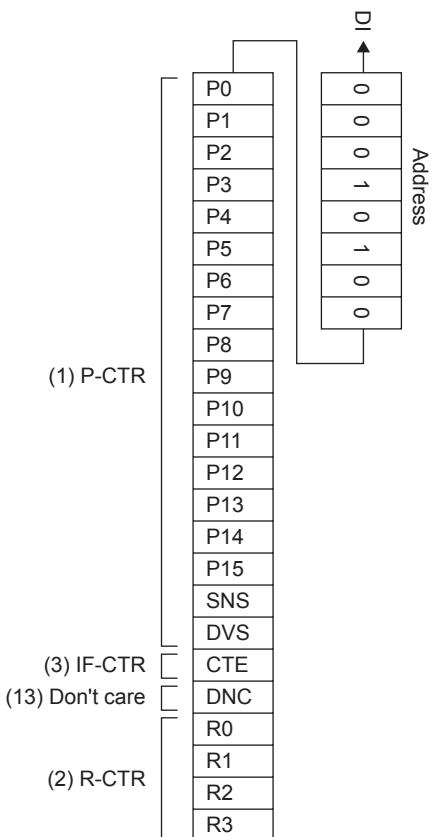
unit : mm (typ)

3253B

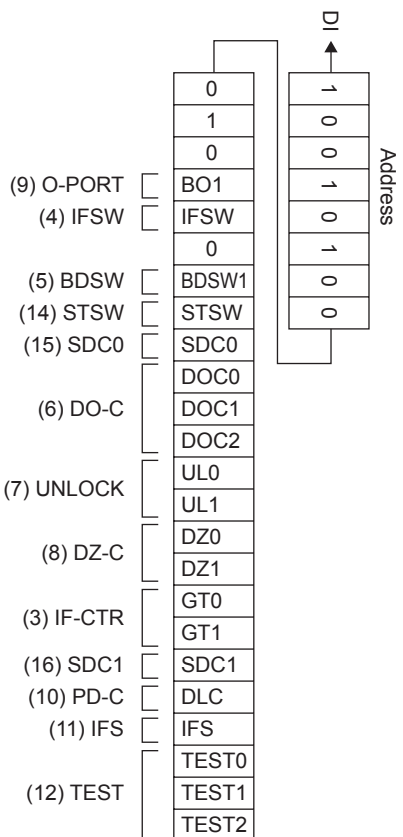


Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode



# LV23015T

## Description of DI control Data

No.	Control/data	Description	Related data																																																																																					
(1)	Programmable divider data  P0 to P15 DVS, SNS	<ul style="list-style-type: none"> <li>Data to set the number of divisions of programmable divider Binary value using P15 as MSB. LSB varies depending on DVS and SNS.                 (* : don't care)  <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>LSB</th> <th>Set number of divisions (N)</th> <th>Actual number of divisions</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>P0</td> <td>272 to 65535</td> <td>Twice the set value</td> </tr> <tr> <td>0</td> <td>1</td> <td>P0</td> <td>272 to 65535</td> <td>Set value</td> </tr> <tr> <td>0</td> <td>0</td> <td>P4</td> <td>4 to 4095</td> <td>Set value</td> </tr> </tbody> </table> </li> <li>* LSB : P0 to P3 invalid when LSB is P4.</li> <li>Selection of the signal input (FMIN, AMIN) to the programmable divider and switching of the input frequency.                 (* : don't care)  <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>Input</th> <th>Operation frequency range</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>FMIN</td> <td>10 to 160MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>AMIN</td> <td>2 to 40MHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>AMIN</td> <td>0.5 to 10MHz</td> </tr> </tbody> </table> </li> </ul>	DVS	SNS	LSB	Set number of divisions (N)	Actual number of divisions	1	*	P0	272 to 65535	Twice the set value	0	1	P0	272 to 65535	Set value	0	0	P4	4 to 4095	Set value	DVS	SNS	Input	Operation frequency range	1	*	FMIN	10 to 160MHz	0	1	AMIN	2 to 40MHz	0	0	AMIN	0.5 to 10MHz																																																		
DVS	SNS	LSB	Set number of divisions (N)	Actual number of divisions																																																																																				
1	*	P0	272 to 65535	Twice the set value																																																																																				
0	1	P0	272 to 65535	Set value																																																																																				
0	0	P4	4 to 4095	Set value																																																																																				
DVS	SNS	Input	Operation frequency range																																																																																					
1	*	FMIN	10 to 160MHz																																																																																					
0	1	AMIN	2 to 40MHz																																																																																					
0	0	AMIN	0.5 to 10MHz																																																																																					
(2)	Reference divider data  R0 to R3	<ul style="list-style-type: none"> <li>Data to select the reference frequency.   <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>R3</th> <th>R2</th> <th>R1</th> <th>R0</th> <th>Reference frequency</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC STOP</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr> </tbody> </table> </li> <li>* PLL INHIBIT</li> <li>Programmable divider and IF counter blocks stop, FMIN, AMIN, and IFIN inputs enter the pull-down state (GND), and the charge pump has high impedance.</li> </ul>	R3	R2	R1	R0	Reference frequency	0	0	0	0	25kHz	0	0	0	1	25kHz	0	0	1	0	25kHz	0	0	1	1	25kHz	0	1	0	0	12.5kHz	0	1	0	1	6.25kHz	0	1	1	0	3.125kHz	0	1	1	1	3.125kHz	1	0	0	0	5kHz	1	0	0	1	5kHz	1	0	1	0	5kHz	1	0	1	1	1kHz	1	1	0	0	3kHz	1	1	0	1	15kHz	1	1	1	0	PLL INHIBIT+X'tal OSC STOP	1	1	1	1	PLL INHIBIT	
R3	R2	R1	R0	Reference frequency																																																																																				
0	0	0	0	25kHz																																																																																				
0	0	0	1	25kHz																																																																																				
0	0	1	0	25kHz																																																																																				
0	0	1	1	25kHz																																																																																				
0	1	0	0	12.5kHz																																																																																				
0	1	0	1	6.25kHz																																																																																				
0	1	1	0	3.125kHz																																																																																				
0	1	1	1	3.125kHz																																																																																				
1	0	0	0	5kHz																																																																																				
1	0	0	1	5kHz																																																																																				
1	0	1	0	5kHz																																																																																				
1	0	1	1	1kHz																																																																																				
1	1	0	0	3kHz																																																																																				
1	1	0	1	15kHz																																																																																				
1	1	1	0	PLL INHIBIT+X'tal OSC STOP																																																																																				
1	1	1	1	PLL INHIBIT																																																																																				
(3)	IF counter control data  CTE GT0, GT1	<ul style="list-style-type: none"> <li>IF counter measurement start data                CTE = 1 : Count start                = 0 : Count reset</li> <li>Determines the universal counter measurement time.   <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>GT1</th> <th>GT0</th> <th>Measurement time</th> <th>Wait time</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>4ms</td> <td>3 to 4ms</td> </tr> <tr> <td>0</td> <td>1</td> <td>8ms</td> <td>3 to 4ms</td> </tr> <tr> <td>1</td> <td>0</td> <td>16ms</td> <td>3 to 4ms</td> </tr> <tr> <td>1</td> <td>1</td> <td>32ms</td> <td>3 to 4ms</td> </tr> </tbody> </table> </li> </ul>	GT1	GT0	Measurement time	Wait time	0	0	4ms	3 to 4ms	0	1	8ms	3 to 4ms	1	0	16ms	3 to 4ms	1	1	32ms	3 to 4ms	IFS																																																																	
GT1	GT0	Measurement time	Wait time																																																																																					
0	0	4ms	3 to 4ms																																																																																					
0	1	8ms	3 to 4ms																																																																																					
1	0	16ms	3 to 4ms																																																																																					
1	1	32ms	3 to 4ms																																																																																					
(4)	MUTE IF count output SD time constant changeover control data  IFSW	<ul style="list-style-type: none"> <li>Data to determine the output of the output port IFSW, controlling the MUTE function, IF count output (*1), and SD time constant changeover circuit (*2).                "Data" = 0 : MUTE, IF count output, SD time constant changeover circuit-OFF                (during normal reception)                1 : MUTE, IF count output, SD time constant changeover circuit-ON                (during search of the desired station)</li> <li>*1 : IF counter buffer output entered in the IF counter circuit of the PLL logic block</li> <li>*2 : The rise time of AM-AGC voltage is shortened through rapid charge to the pin-25 external capacity when IFSW has been set to 1.</li> </ul>																																																																																						
(5)	FM/AM BAND switch control data BDSW	<ul style="list-style-type: none"> <li>Data to determine the output of the output port BDSW, controlling switching of BAND.                "Data" = 0 : AM                1 : FM</li> </ul>																																																																																						

Continued on next page.

# LV23015T

Continued from preceding page.

No.	Control/data	Description	Related data																																				
(6)	DO pin control data  DOC0 DOC1 DOC2	<ul style="list-style-type: none"> <li>Data to determine the output of the DO pin.</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>DOC2</th> <th>DOC1</th> <th>DOC0</th> <th>DO pin state</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td>Open</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td>Low detection of unlock</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td>end-UC (See below)</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td>Open</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td>Open</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td>Low at SD ON</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td>Low at stereo</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td>Open</td></tr> </tbody> </table> <ul style="list-style-type: none"> <li>Open selected with power ON reset</li> <li>* IF counter measurement end check</li> </ul> <div style="text-align: center;"> <p style="font-size: small;">(1) Count start      (2) Count end      (3) CE : Hi</p> </div> <p>(1) DO pin open automatically when end-UC is set and the IF counter starts (CTE = 0→1).                      (2) DO pin becomes low, enabling check of the counter end when the IF counter measurement is over.                      (3) DO pin open with serial data input/output (CE pin : Hi)</p> <p>Note) DO pin open regardless of the DO pin control data (DOC0 to 2) during data input period (IN1 and IN2 modes CE-Hi period).                      The DO pin state allows output of the content of internal DO serial data in synchronization with CL regardless of the DO pin control data (DOC0 to 2) during data input period (OUT mode CE : Hi period).</p>	DOC2	DOC1	DOC0	DO pin state	0	0	0	Open	0	0	1	Low detection of unlock	0	1	0	end-UC (See below)	0	1	1	Open	1	0	0	Open	1	0	1	Low at SD ON	1	1	0	Low at stereo	1	1	1	Open	UL0, UL1 CTE
DOC2	DOC1	DOC0	DO pin state																																				
0	0	0	Open																																				
0	0	1	Low detection of unlock																																				
0	1	0	end-UC (See below)																																				
0	1	1	Open																																				
1	0	0	Open																																				
1	0	1	Low at SD ON																																				
1	1	0	Low at stereo																																				
1	1	1	Open																																				
(7)	Unlock detection data  UL0, UL1	<ul style="list-style-type: none"> <li>Data to select the phase error (<math>\phi E</math>) detection width to determine if PLL is locked. Unlock is determined when the phase error exceeding the detection width occurs.</li> </ul> <p style="text-align: right; font-size: small;">(* : don't care)</p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>UL1</th> <th>UL0</th> <th><math>\phi E</math> Detection width</th> <th>Detection output</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">Stop</td><td style="text-align: center;">Open</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;"><math>\phi E</math> output directly</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">*</td><td style="text-align: center;"><math>\pm 6.67\mu s</math></td><td style="text-align: center;"><math>\phi E</math> extended by 1 to 2ms</td></tr> </tbody> </table> <p>* unlock : DO pin becomes Low and the serial data output becomes UL = 0.</p>	UL1	UL0	$\phi E$ Detection width	Detection output	0	0	Stop	Open	0	1	0	$\phi E$ output directly	1	*	$\pm 6.67\mu s$	$\phi E$ extended by 1 to 2ms	DOC0 DOC1 DOC2																				
UL1	UL0	$\phi E$ Detection width	Detection output																																				
0	0	Stop	Open																																				
0	1	0	$\phi E$ output directly																																				
1	*	$\pm 6.67\mu s$	$\phi E$ extended by 1 to 2ms																																				
(8)	Phase comparator control data  DZ0, DZ1	<ul style="list-style-type: none"> <li>Data to control the dead band of phase comparator.</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>DZ1</th> <th>DZ0</th> <th>Deadband mode</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">DZA</td></tr> <tr><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">DZB</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">DZC</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">DZD</td></tr> </tbody> </table> <p style="text-align: center; font-size: small;">Dead band : DZA &lt; DZB &lt; DZC &lt; DZD</p>	DZ1	DZ0	Deadband mode	0	0	DZA	0	1	DZB	1	0	DZC	1	1	DZD																						
DZ1	DZ0	Deadband mode																																					
0	0	DZA																																					
0	1	DZB																																					
1	0	DZC																																					
1	1	DZD																																					
(9)	Output port data  $\overline{BO1}$	<ul style="list-style-type: none"> <li>Data to determine the output of output ports <math>\overline{BO1}</math></li> </ul> <p style="font-size: small;">"Data" = 0 : OPEN                      1 : Low</p>																																					
(10)	Charge pump control data  DLC	<ul style="list-style-type: none"> <li>Data for forced control of the charge pump output</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>DLC</th> <th>Charge pump output</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">0</td><td style="text-align: center;">Normal operation</td></tr> <tr><td style="text-align: center;">1</td><td style="text-align: center;">Forced Low</td></tr> </tbody> </table> <p style="font-size: small;">When the VCO control voltage (<math>V_{tune}</math>) develops dead lock because of stop of oscillation of VCO at 0V, set the charge pump output to LOW and <math>V_{tune}</math> to <math>V_{CC}</math> to escape the dead lock. (Dead lock clear circuit)</p>	DLC	Charge pump output	0	Normal operation	1	Forced Low																															
DLC	Charge pump output																																						
0	Normal operation																																						
1	Forced Low																																						
(11)	IFS	<ul style="list-style-type: none"> <li>Normally, set data = 1. Setting the data = 0 causes worsening of the input sensitivity, resulting in decrease of the sensitivity by about 10 to 30mVrms.</li> </ul>																																					
(12)	LSI test data  TEST0 to 2	<ul style="list-style-type: none"> <li>LSI test data</li> </ul> <table style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">TEST0</td> <td rowspan="3" style="font-size: 2em; vertical-align: middle;">}</td> <td rowspan="3" style="text-align: center; vertical-align: middle;">All to be set to "0"</td> </tr> <tr> <td style="text-align: center;">TEST1</td> </tr> <tr> <td style="text-align: center;">TEST2</td> </tr> </table> <p style="font-size: small;">All set to 0 for power ON reset</p>	TEST0	}	All to be set to "0"	TEST1	TEST2																																
TEST0	}	All to be set to "0"																																					
TEST1																																							
TEST2																																							
(13)	DNC	<ul style="list-style-type: none"> <li>Set data = 0.</li> </ul>																																					

Continued on next page.

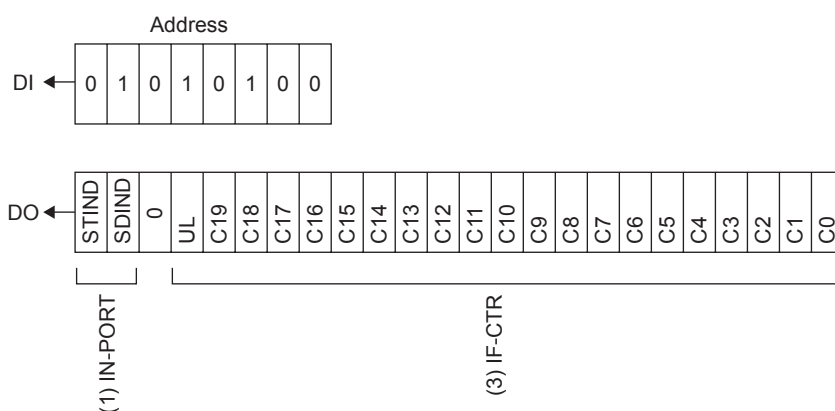
# LV23015T

Continued from preceding page.

No.	Control block data	Description	Related data
(14)	Forced monaural control data  STSW	<ul style="list-style-type: none"> <li>Data to determine the output of the output port STSW, controlling the forced monaural stereo function "Data" = 0 : MONO 1 : STEREO</li> </ul>	
(15) (16)	SD sensitivity adjustment data  SDC0 SDC1	<ul style="list-style-type: none"> <li>Data to determine the output of output ports SDC0 and SDC1, setting the SD sensitivity "Data" = SDC0 : 0, SDC1 : 0 → SD sensitivity = 50dB<math>\mu</math>V (Typ) SDC0 : 0, SDC1 : 1 → SD sensitivity = 53dB<math>\mu</math>V (Typ) SDC0 : 1, SDC1 : 0 → SD sensitivity = 59dB<math>\mu</math>V (Typ) SDC0 : 1, SDC1 : 1 → SD sensitivity = 64dB<math>\mu</math>V (Typ)</li> </ul>	

## Composition of the DO control data (serial data output)

### (1) OUT mode



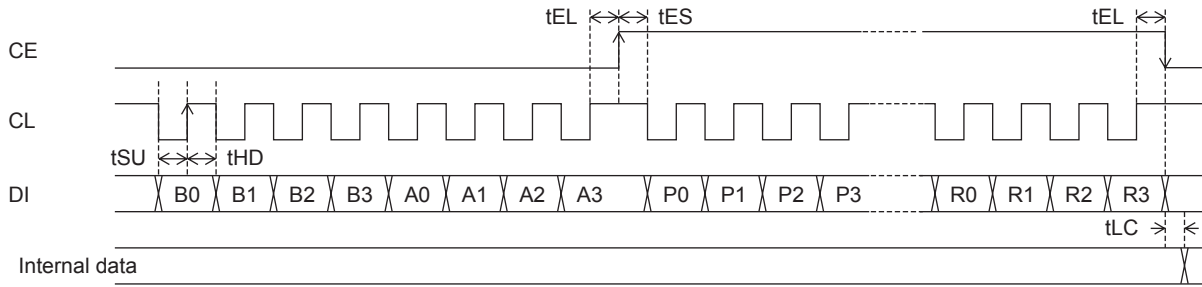
## Description of DO output data

No.	Control/data	Description	Related data
(1)	Stereo indicator SD indicator Control data  STIND, SDIND	<ul style="list-style-type: none"> <li>Data latching stereo indicator and SI indicator states. Latch made at a time of the data output mode (OUT mode). STIND ← Stereo indicator state    0 : ST ON, 1 : ST OFF SDIND ← SD indicator state        0 : SD ON, 1 : SD OFF</li> </ul>	
(2)	PLL unlock data  UL	<ul style="list-style-type: none"> <li>Data latching the content of the unlock detection circuit UL ← 0 : At unlock 1 : At lock or detection stop mode</li> </ul>	UL0 UL1
(3)	IF counter Binary counter  C19 to C0	<ul style="list-style-type: none"> <li>Data latching the content of IF counter (20 bit binary counter) C19 ← MSB of binary counter C0 ← LSB of binary counter</li> </ul>	CTE GT0 GT1

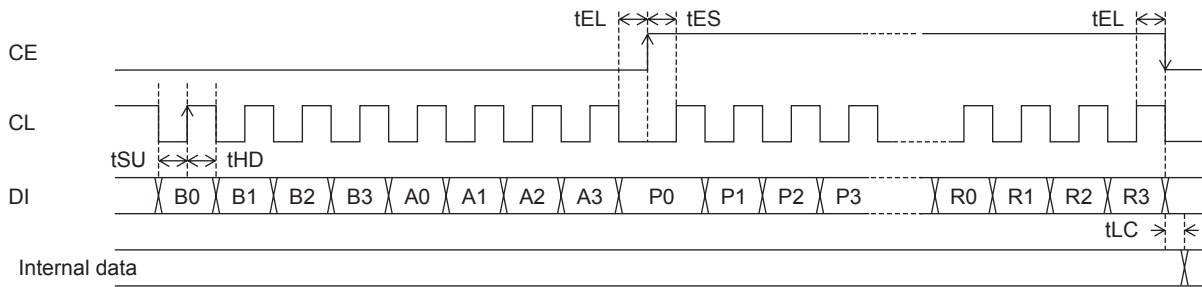
# LV23015T

**Serial data input (IN1/IN2)**  $t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$   $t_{LC} < 0.75\mu s$

(1) CL : normal Hi

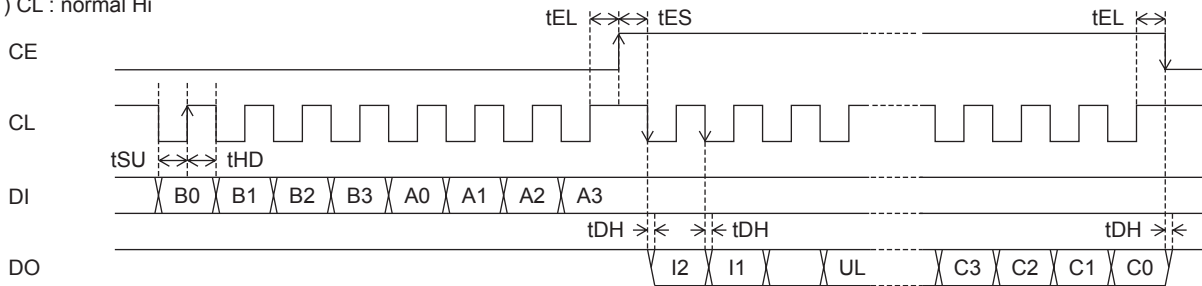


(2) CL : normal Low

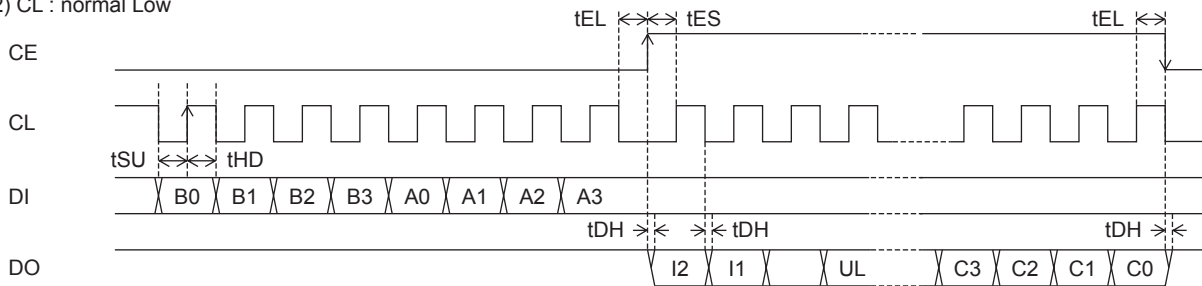


**Serial data output (OUT)**  $t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$   $t_{DC}, t_{DH} < 0.35\mu s$

(1) CL : normal Hi



(2) CL : normal Low

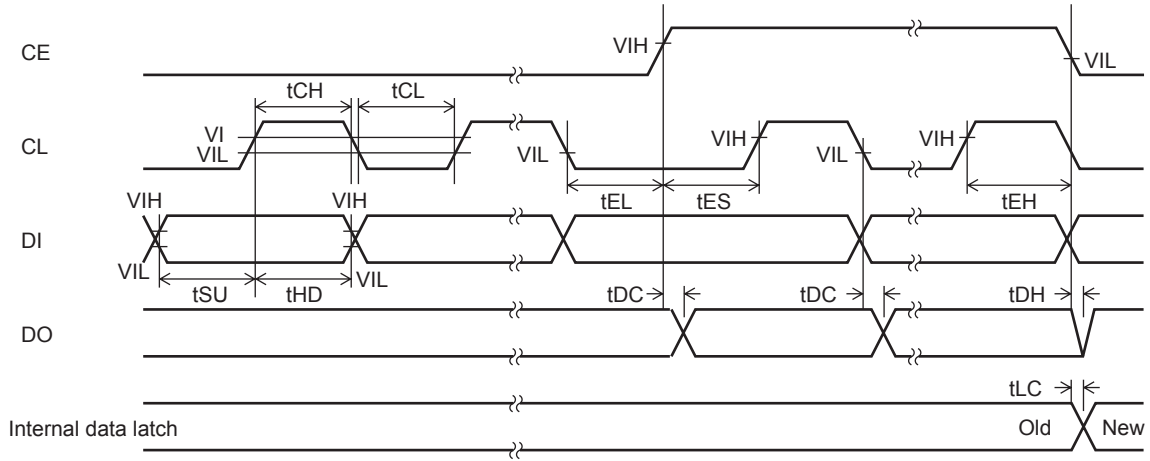


Note : The DO pin is an Nch open drain pin, so that the data change time ( $t_{DC}$ ,  $t_{DH}$ ) changes depending on the pull-up resistance and substrate capacity.

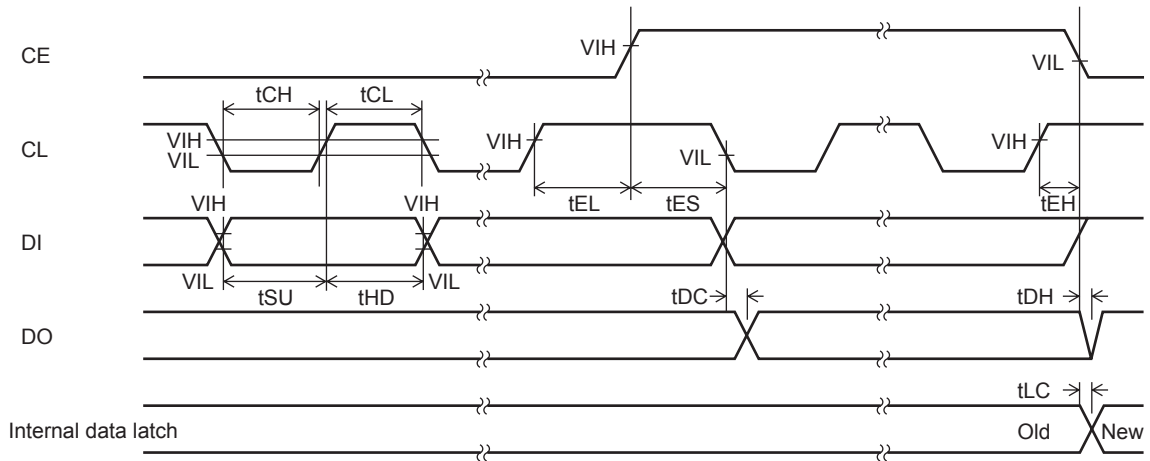


# LV23015T

## Serial data timing

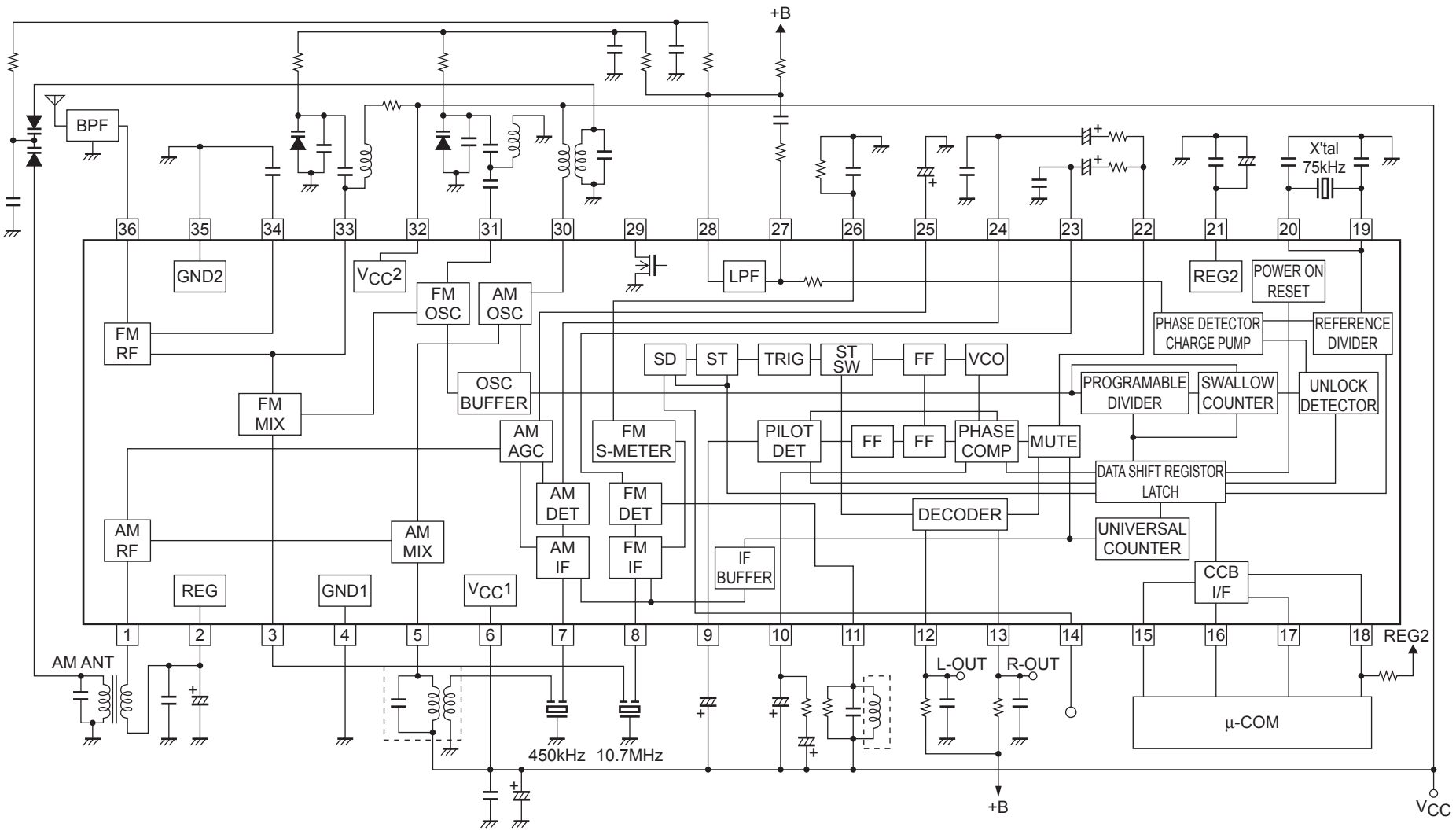


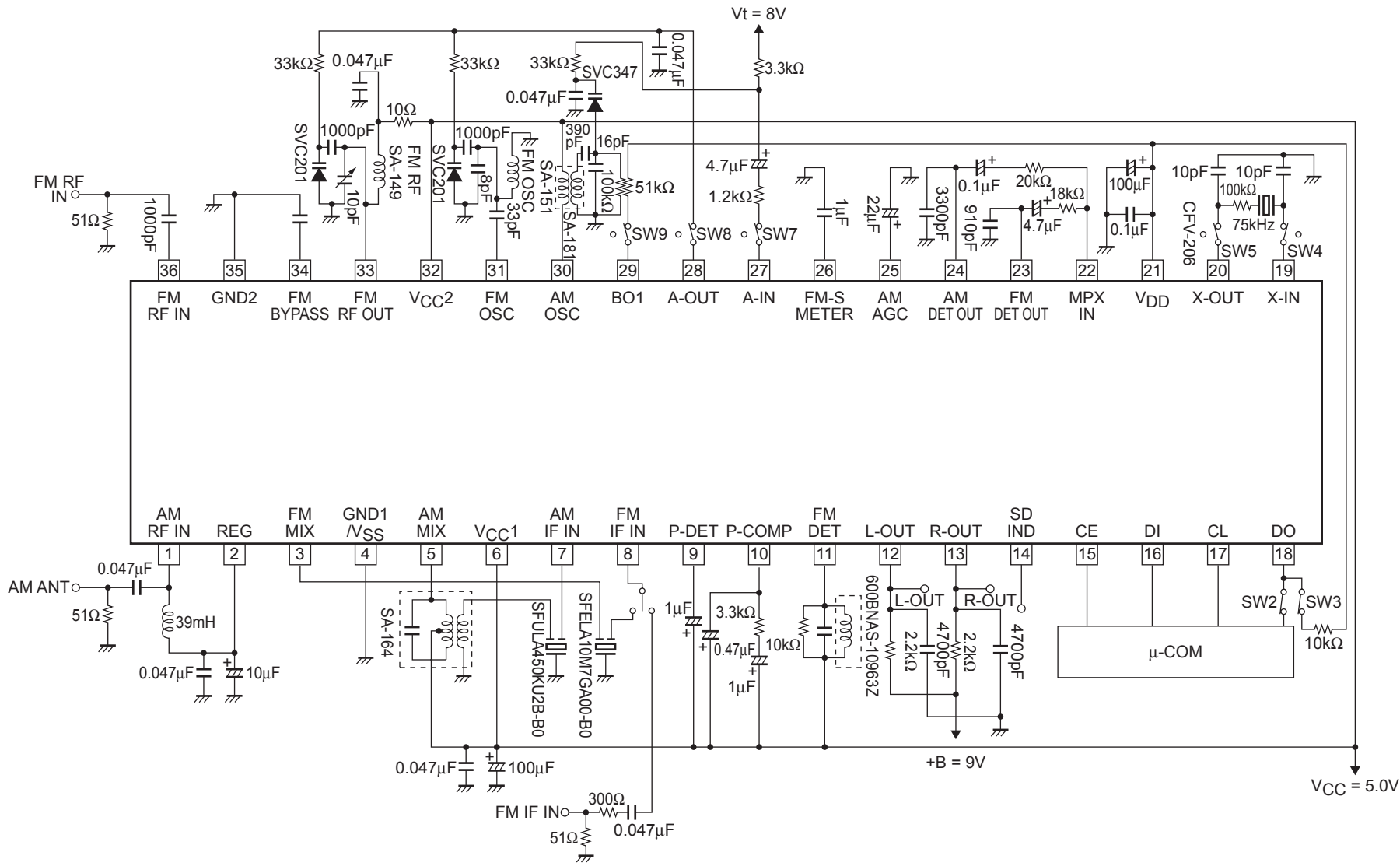
<< CL stopped at "L" level >>



<< CL stopped at "H" level >>

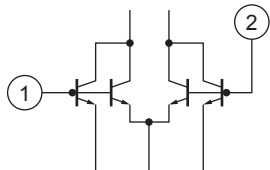
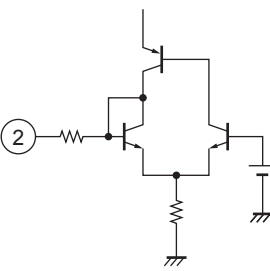
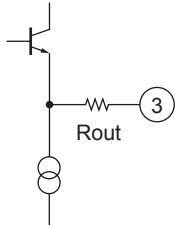
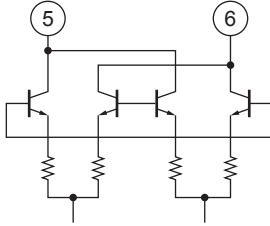
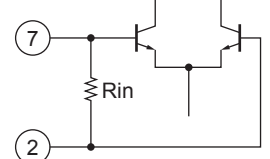
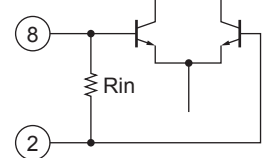
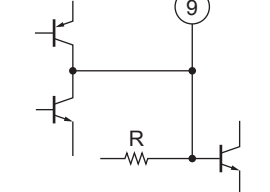
Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI, CL		0.75			μs
Data hold time	tHD	DI, CL		0.75			μs
Clock L level time	tCL	CL		0.75			μs
Clock H level time	tCH	CL		0.75			μs
CE wait time	tEL	CE, CL		0.75			μs
CE setup time	tES	CE, CL		0.75			μs
CE hold time	tEH	CE, CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO, CL	Varies depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO, CE					





# LV23015T

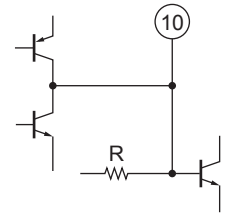
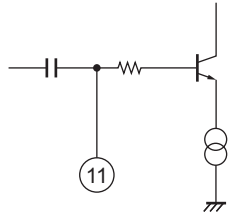
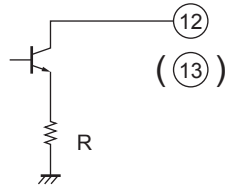
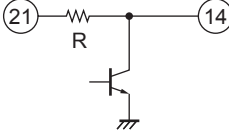
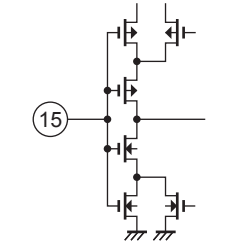
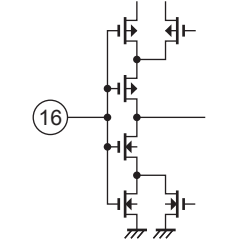
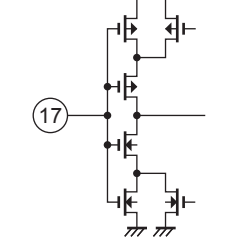
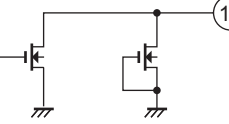
## LV23014T Pin description and pin voltage ( $V_{CC} = 5.0V$ , $+B = 9.0V$ )

No.	Pin name	Pin description	No input voltage (V)		Internal equivalent circuit
			AM	FM	
1	AM RF input	Connect the AM ANT coil between this pin and pin 2 (Vreg1).	Vreg1	Vreg1	
2	REG1	Reference voltage of AM/FM, IF/MPX block	2.2	2.2	
3	FM MIX output	$R_{out} = 270\Omega$	$(2/3)V_{CC} - 0.5$	$(2/3)V_{CC} - 0.7$	
4	GND1	GND of AM/FM, IF/MPX block	0	0	
5	AM MIX output	Connect the AM MIX coil between this pin and pin 6 ( $V_{CC}$ voltage).	$V_{CC}$	$V_{CC}$	
6	$V_{CC1}$	$V_{CC}$ of AM/FM, IF/MPX block	5.0	5.0	
7	AM IF input	$R_{in} = 2k\Omega$	Vreg1	Vreg1	
8	FM IF input	$R_{in} = 330\Omega$	Vreg1	Vreg1	
9	Pilot filter	$R = 10k\Omega$	$V_{CC}-1$	$V_{CC}-1$	

Continued on next page.

# LV23015T

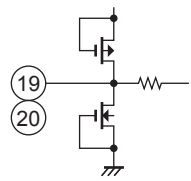
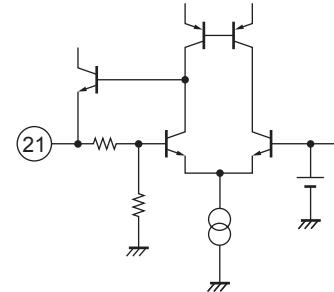
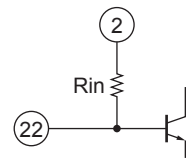
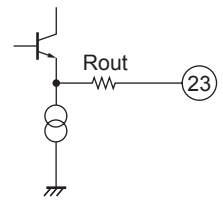
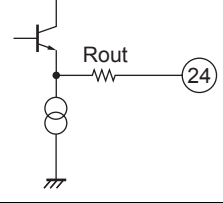
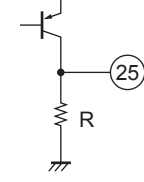
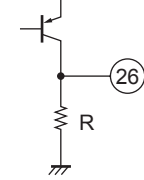
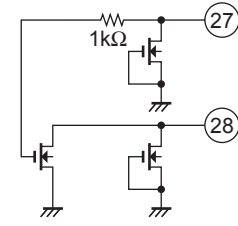
Continued from preceding page.

No.	Pin name	Pin description	No input voltage (V)		Internal equivalent circuit
			AM	FM	
10	Phase comparator filter	R = 10kΩ	V <sub>CC</sub> -1	V <sub>CC</sub> -1	
11	FM DET	Connect the FM DET coil between this pin and pin 6 (V <sub>CC</sub> voltage).  Recommended detection coil : 600BNAS-10963Z by TOKO.	V <sub>CC</sub>	V <sub>CC</sub>	
12	L output	Resistance 2.2kΩ for output level adjustments is connected between pin 12/13 and +B (+9V). R = 600Ω	6.0	6.0	
13	R output		6.0	6.0	
14	SD IND	SD indicator Active low output. R = 30kΩ	Vreg2	Vreg2	
15	CE	Chip enable port At changeover from "L" to "H" address latching. At changeover from "H" to "L" data latching.			
16	DI	Serial data input port Sets data in synchronization with rise of data clock.			
17	CL	Data clock input port			
18	DO	Data output port Outputs various data in synchronization with fall of data clock in the out mode.			

Continued on next page.

# LV23015T

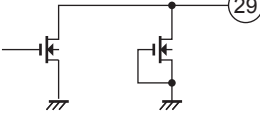
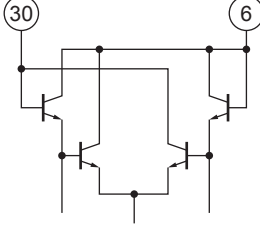
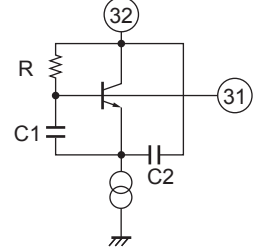
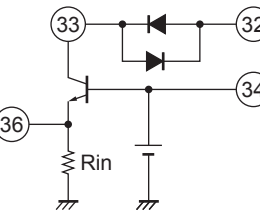
Continued from preceding page.

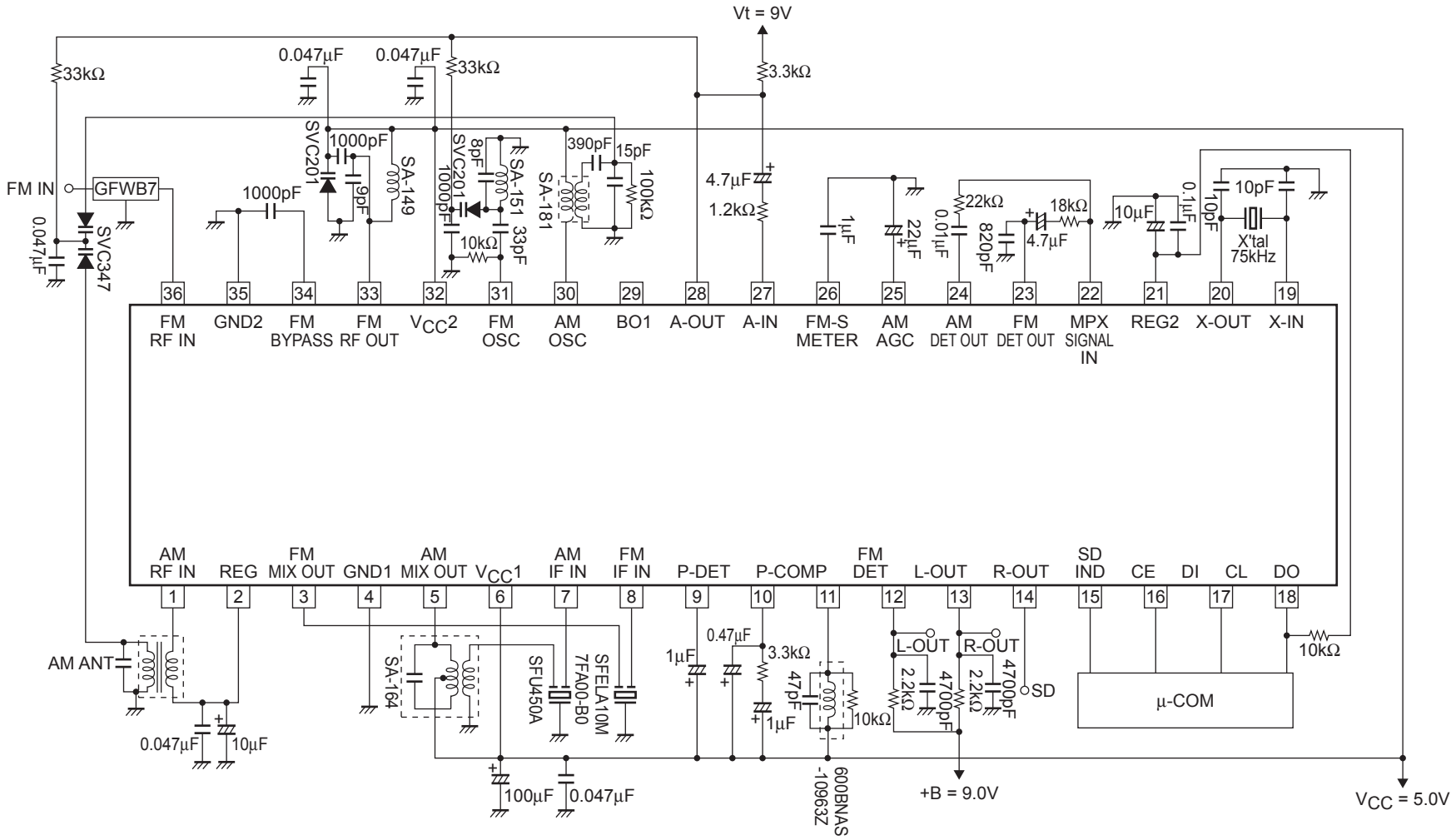
No.	Pin name	Pin description	No input voltage (V)		Internal equivalent circuit
			AM	FM	
19 20	XIN XOUT	Clock for internal reference Connect 75kHz crystal oscillator.			
21	VREG2	Reference voltage of PLL block	3.0	3.0	
22	MPX input	Rin = 20kΩ	Vreg1	Vreg1	
23	FM detection output	The separation can be adjusted with an external capacitor connected between this pin and GND.  Rout = 3.3kΩ	0.8	Vreg1	
24	AM detection output	AM low frequency characteristic can be adjusted with an external capacitor connected between this pin and GND.  Rout = 5.0kΩ	2.0	0	
25	AM AGC output	R = 13.8kΩ	0.8	0	
26	FM S-meter output and FM SD adjust	The FMSD sensitivity can be adjusted with an external resistor connected between this pin and GND.  R = 14.0kΩ	0	0.8	
27 28	AIN AOUT	Nch MOS transistor for PLL active low pass filter.			

Continued on next page.

# LV23015T

Continued from preceding page.

No.	Pin name	Pin description	No input voltage (V)		Internal equivalent circuit
			AM	FM	
29	BO1	General purpose output port			
30	AM OSC	AM OSC circuit with ALC AM OSC coil used between pins 31 and 6 ( $V_{CC}$ voltage).	$V_{CC}$	$V_{CC}$	
31	FM OSC	$R = 10k\Omega$ $C1 = 10pF$ $C2 = 20pF$	$V_{CC}$	4.95	
32	$V_{CC2}$	$V_{CC}$ of FM FE block	5.0	5.0	
33	FM RF output	FM RF coil used between pins 33 and 32 ( $V_{CC}$ voltage).	$V_{CC}$	$V_{CC}$	
34	FM bypass	The capacity of 1000pF is connected between pins 34 and 35 (GND).	0	1.6	
35	FM RF input	$R_{in} = 1.5k\Omega$	0	0.9	
35	GND2	GND of FM FE block	0	0	





ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.