

MOD-ENC624J600 development board

Users Manual



All boards produced by Olimex are ROHS compliant

Rev. A, June 2011

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INTRODUCTION

MOD-ENC624J600 is development board with UEXT connector and 100 Mbit ENC624J600 ethernet controller from Microchip Technology Inc.

BOARD FEATURES

- MOD-ENC624J600 is the easiest way to add 100 Mbit ethernet connectivity to any of our boards with UEXT connector
- ENC624J600 Ethernet controller with UEXT connector for easy connection to our other development boards with UEXT connector
- LAN connector with build in transformer
- two status LEDs on LAN connector
- SPI/PARALLEL port interface to add Ethernet interface to your microcontroller project
- UEXT 10 pin interface on 0.1" row pins header
- PCB: FR-4, 1.5 mm (0,062"), soldermask, white silkscreen component print
- Dimensions: 46.99x36.83 mm (1.85 x 1.45")

ELECTROSTATIC WARNING

The MOD-ENC624J600 board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

BOARD USE REQUIREMENTS

Hardware: Our development board PIC 32-WEB use ENC624J600

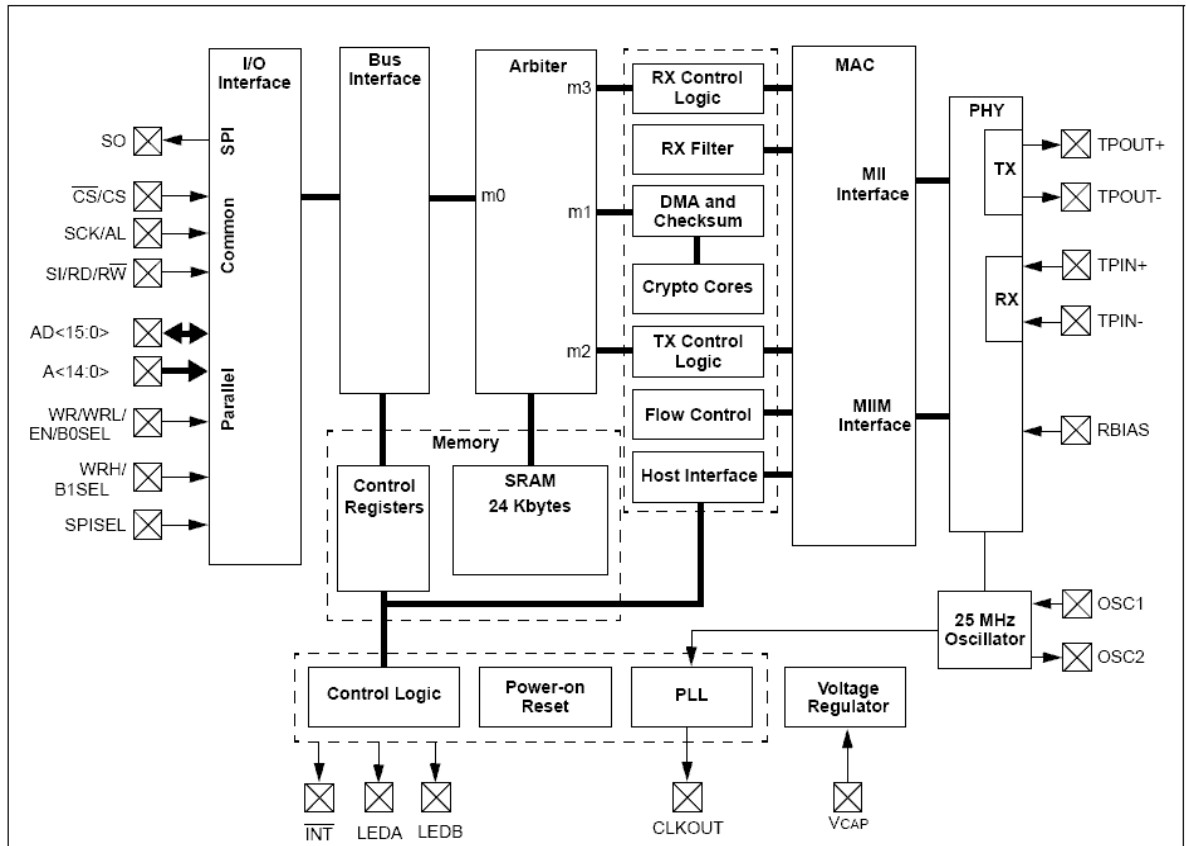
ETHERNET CONTROLLER FEATURES

MOD-ENC28J60 board use ENC624J600 stand-alone ethernet controller with these features:

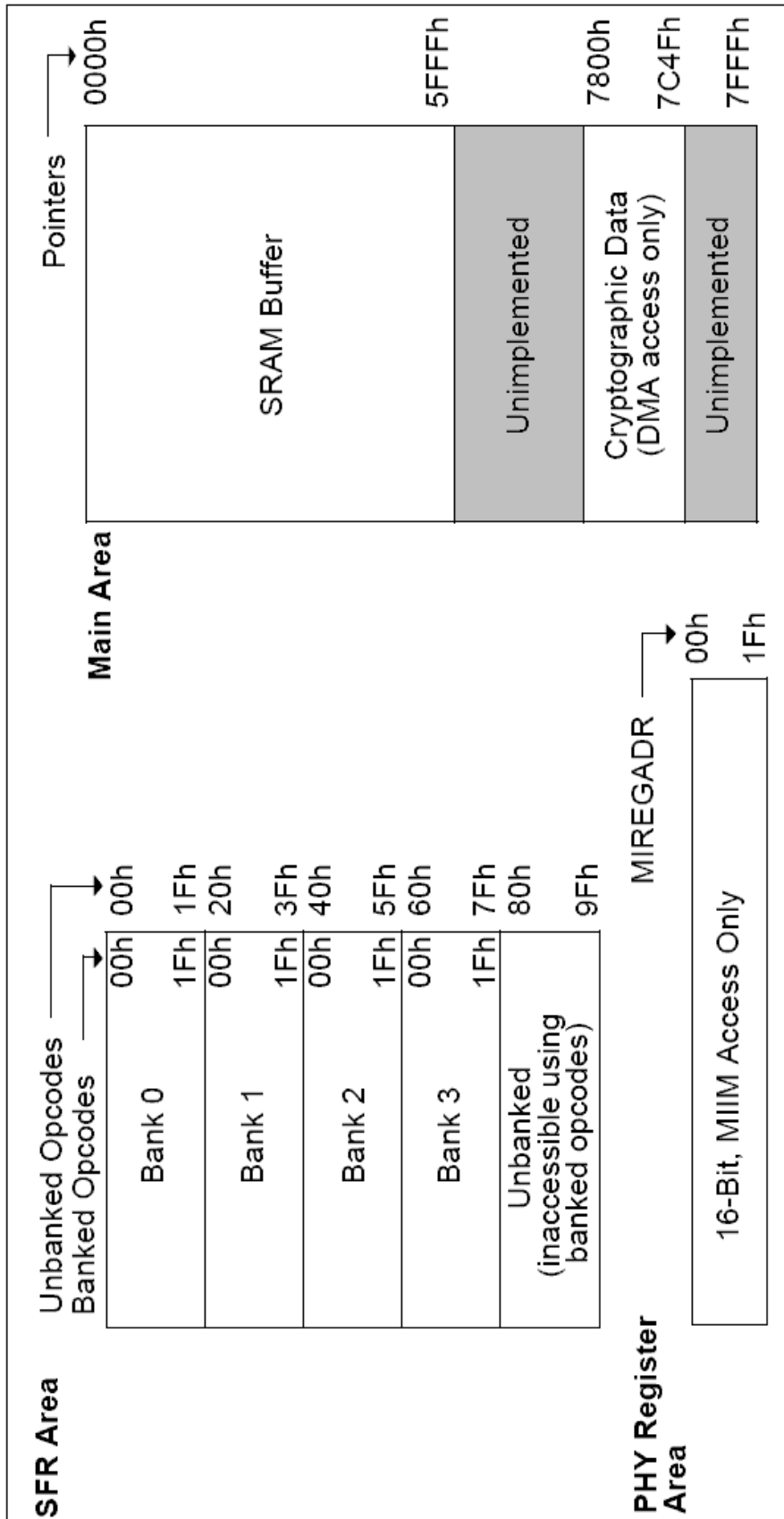
- IEEE 802.3™ Compliant Fast Ethernet Controller
- Integrated MAC and 10/100Base-T PHY
- Hardware Security Acceleration Engines
- 24-Kbyte Transmit/Receive Packet Buffer SRAM
- Supports one 10/100Base-T Port with Automatic Polarity Detection and Correction
- Supports Auto-Negotiation
- Support for Pause Control Frames, including Automatic Transmit and Receive Flow Control
- Supports Half and Full-Duplex Operation
- Programmable Automatic Retransmit on Collision
- Programmable Padding and CRC Generation
- Programmable Automatic Rejection of Erroneous and Runt Packets
- Factory Preprogrammed Unique MAC Address
- MAC:
 - Support for Unicast, Multicast and Broadcast packets
 - Supports promiscuous reception
 - Programmable pattern matching
 - Programmable filtering on multiple packet formats, including Magic Packet™, Unicast, Multicast, Broadcast, specific packet match, destination address hash match or any packet
- PHY:
 - Wave shaping output filter
 - Internal Loopback mode
 - Energy Detect Power-Down mode
- Security Engines:
 - High-performance, modular exponentiation engine with up to 1024-bit operands
 - Supports RSA® and Diffie-Hellman key exchange algorithms
 - High-performance AES encrypt/decrypt engine with 128-bit, 192-bit or 256-bit key
 - Hardware AES ECB, CBC, CFB and OFB mode capability
 - Software AES CTR mode capability
 - Fast MD5 hash computations
 - Fast SHA-1 hash computations

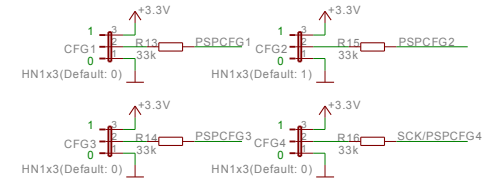
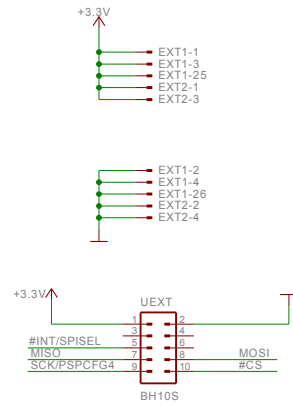
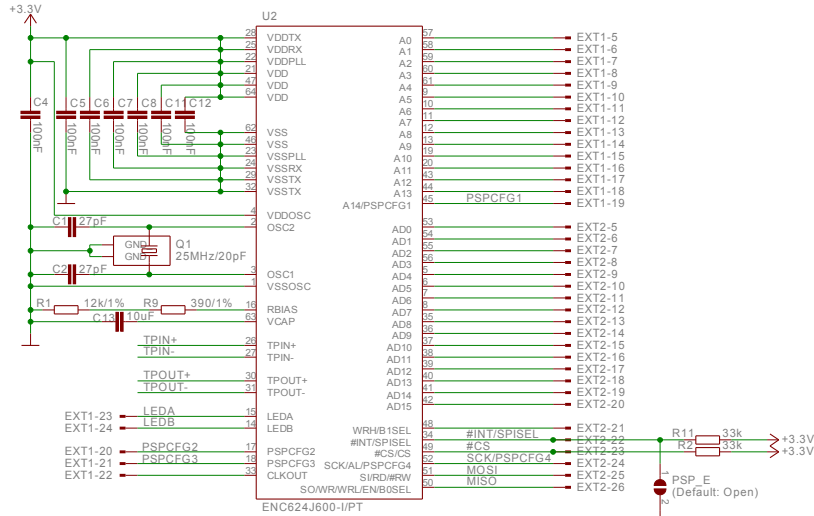
- Buffer:
 - Configurable transmit/receive buffer size
 - Hardware-managed circular receive FIFO
 - 8-bit or 16-bit random and sequential access
 - High-performance internal DMA for fast memory copying
 - High-performance hardware IP checksum calculations
 - Accessible in low-power modes
 - Space can be reserved for general purpose application usage in addition to transmit and receive packets
- Operational:
 - Outputs for two LED indicators with support for single and dual LED configurations
 - Transmit and receive interrupts
 - 25MHz clock
 - 5V tolerant inputs
 - Clock out pin with programmable frequencies from 50 kHz to 33.3 MHz
 - Operating voltage range of 3.0V to 3.6V
 - Temperature range: -40°C to +85°C industrial

BLOCK DIAGRAM



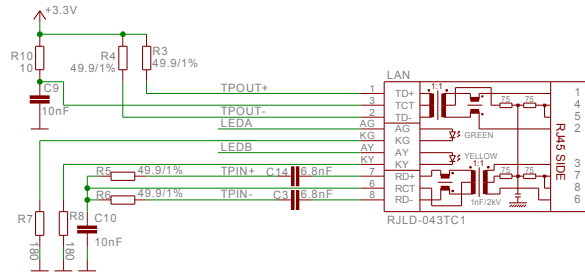
MEMORY MAP



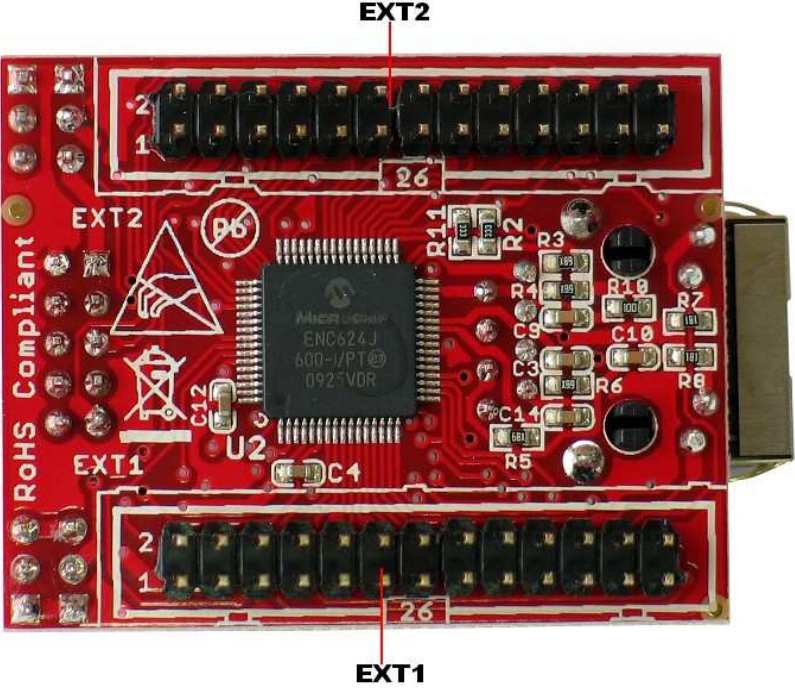
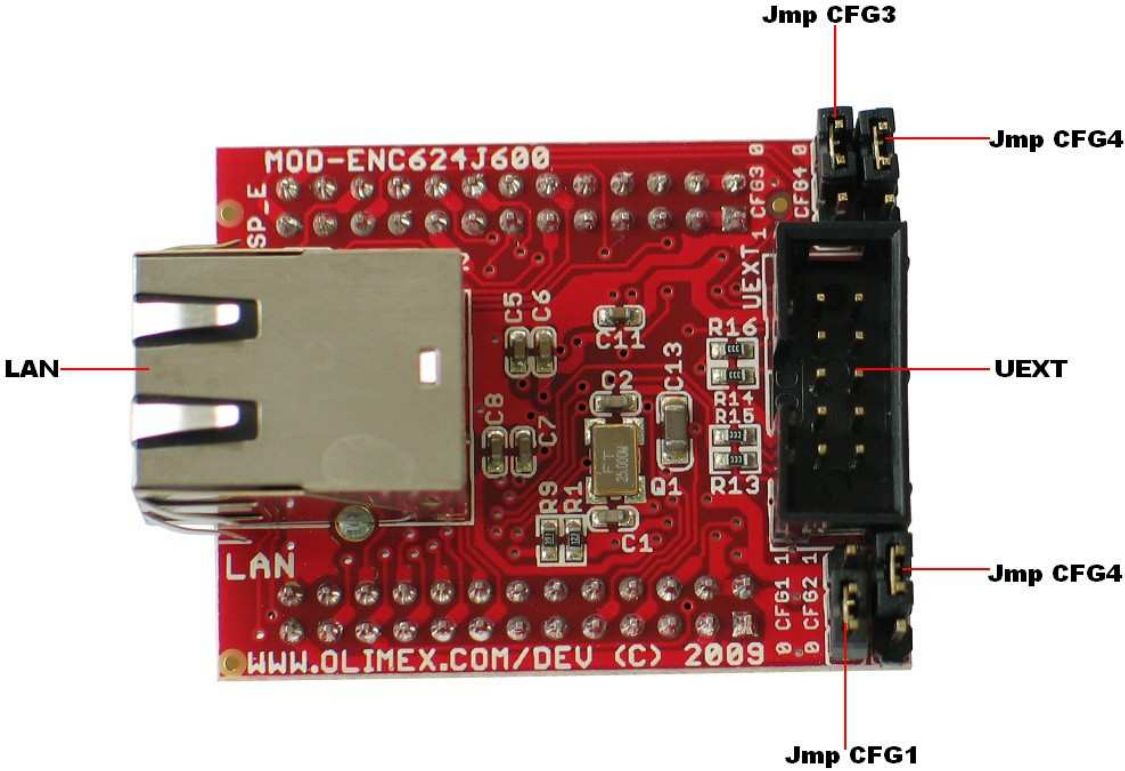


MOD-ENC624J600

Rev. Initial
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BOARD LAYOUT



POWER SUPPLY CIRCUIT

MOD-ENC624J600 is typically power supplied by UEXT pin 1 and pin 2, EXT1 - pins 1, 3, 25 and pins 2, 4, 26, EXT2 - pins 1, 3 and 2, 4.

CLOCK CIRCUIT

Quartz crystal 25 MHz is connected to ENC624J600 pin 2 (OSC2) and pin3 (OSC1).

JUMPER DESCRIPTION

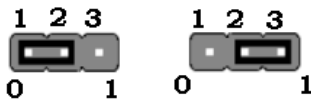
PSP_E



When is closed this jumper enables PSP mode.

Default state is open.

CFG1, CFG2, CFG3, CFG4



MOD-ENC624J600 works in several modes. Jumpers position define the working mode :

PSP Mode 9:

CFG1 - in position "0"

CFG2 - in position "1"

CFG3 - in position "1"

CFG4 - in position "0"

PSP Mode 3:

CFG1 - in position "0"

CFG2 - in position "1"

CFG3 - in position "0"

CFG4 - in position "0"

SPI Mode - connected to SPI2:

CFG1 - doesn't matter

CFG2 - doesn't matter

CFG3 - doesn't matter

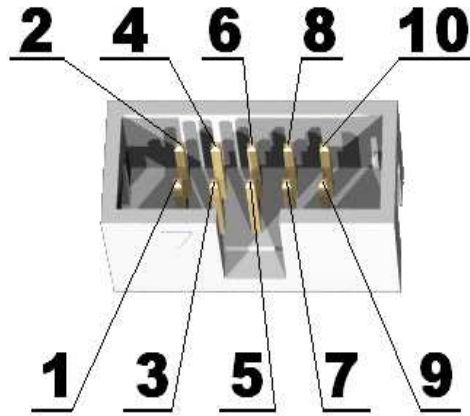
CFG4 - doesn't matter

PSP_E - open

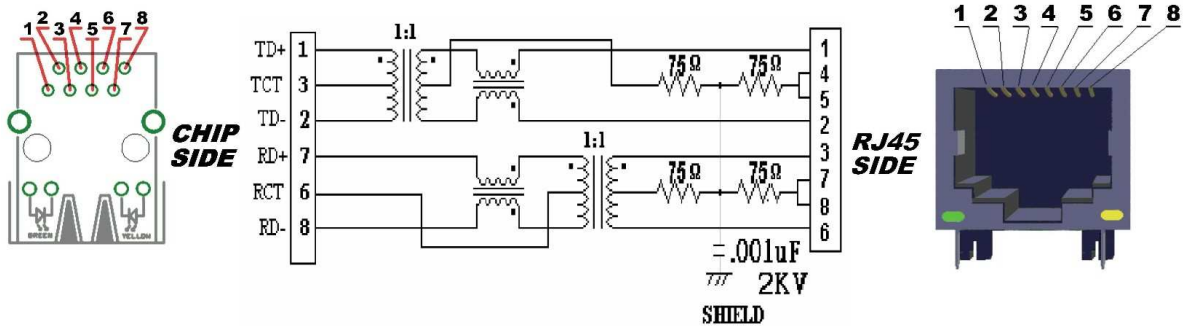
CONNECTOR DESCRIPTION

UEXT

Pin #	Signal Name
1	+3.3V
2	GND
3	NC
4	NC
5	#INT/SPISEL
6	NC
7	MISO
8	MOSI
9	SCK/PSPCFG4
10	#CS



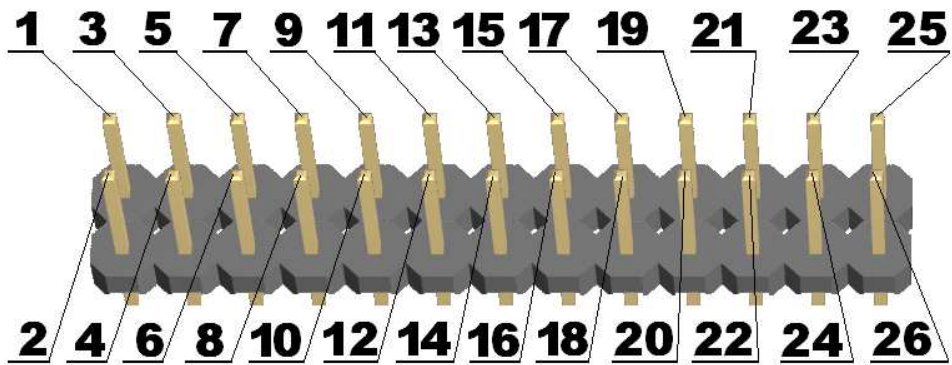
LAN



Pin #	Signal Name Chip Side	Pin #	Signal Name Chip Side
1	TX+	5	Not Connected (NC)
2	TX-	6	VDD
3	VDD	7	RX+
4	Not Connected (NC)	8	RX-

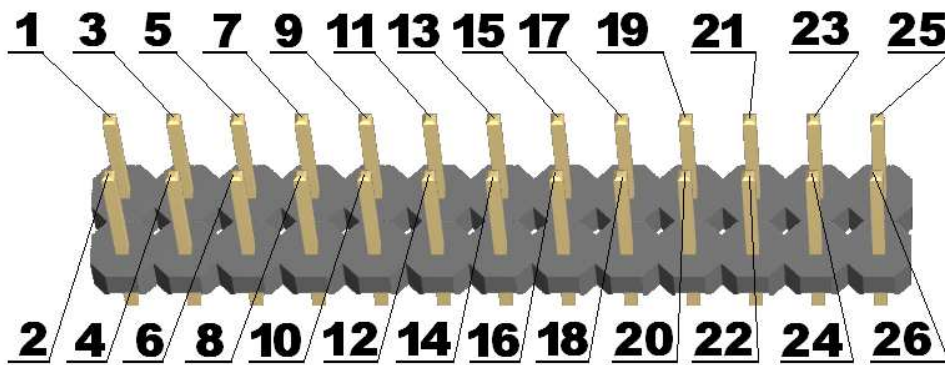
LED	Color	Usage
Right	Green	Link status
Left	Yellow	Activity status

EXT1



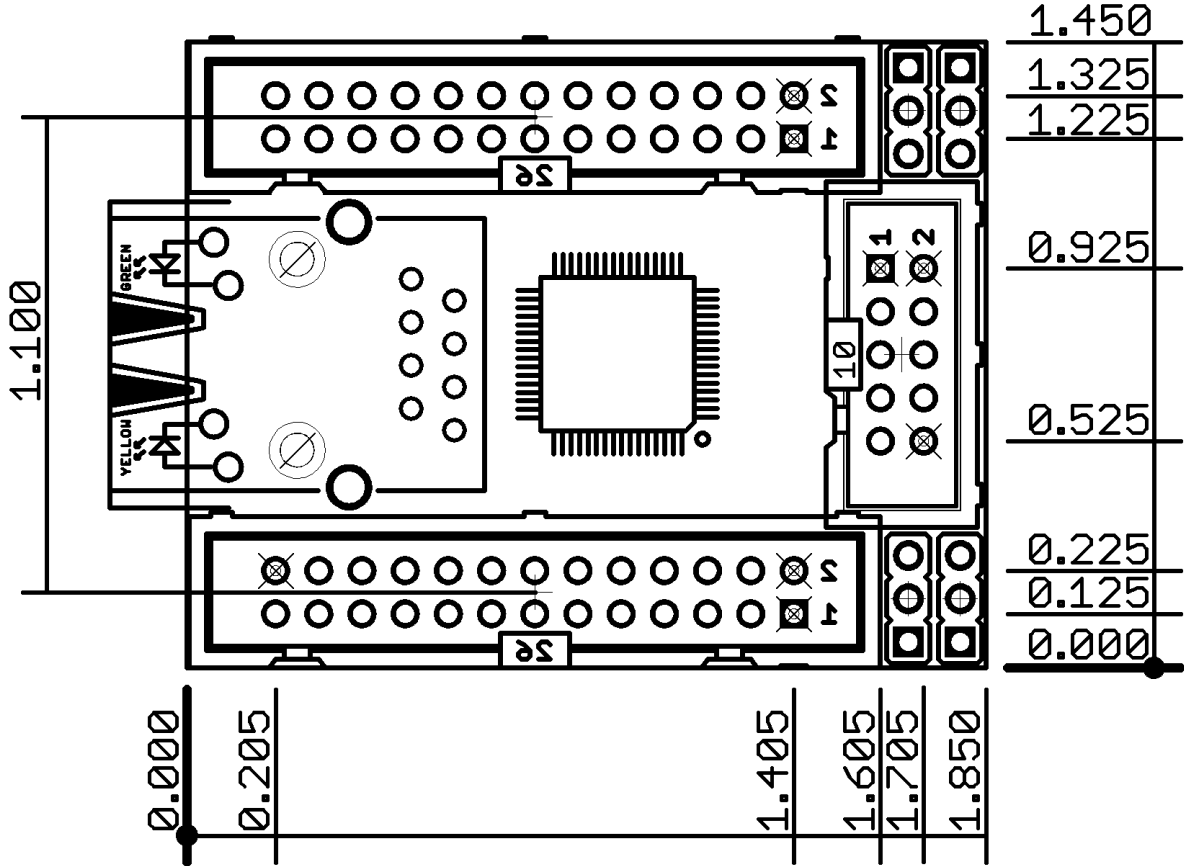
Pin #	Signal Name	Pin #	Signal Name
1	3.3V	2	GND
3	3.3V	4	GND
5	A0	6	A1
7	A2	8	A3
9	A4	10	A5
11	A6	12	A7
13	A8	14	A9
15	A10	16	A11
17	A12	18	A13
19	PSPCFG1	20	PSPCFG2
21	PSPCFG3	22	CLKOUT
23	LEDA	24	LEDB
25	3.3V	26	GND

EXT2



Pin #	Signal Name	Pin #	Signal Name
1	3.3V	2	GND
3	3.3V	4	GND
5	AD0	6	AD1
7	AD2	8	AD3
9	AD4	10	AD5
11	AD6	12	AD7
13	AD8	14	AD9
15	AD10	16	AD11
17	AD12	18	AD13
19	AD14	20	AD15
21	WRH/B1SEL	22	#INT/SPISEL
23	#CS	24	SCK/PSPCFG4
25	MOSI	26	MISO

MECHANICAL DIMENSIONS



All measures are in inches.

AVAILABLE DEMO SOFTWARE

- Microchip's TCP-IP stack full featured TCP-IP stack, very easy to configure and use with PIC microcontrollers.
- Demo code with PIC32-WEB board

ORDER CODE

MOD-ENC624J600 Completely assembled and tested, includes ENC624J600 Ethernet controller

How to order?

You can order to us directly or by any of our distributors.

Check our web www.olimex.com/dev for more info.

Revision history:

Rev. Initial	- create November 2009
Rev. A	- edited June 2011 - added more detailed mechanical dimensions

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