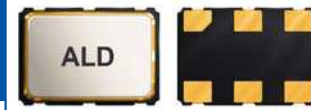


# PECL/LVDS/CMOS OUTPUT SMD CRYSTAL CLOCK OSCILLATOR



5.0 x 7.0 x 1.8mm

ALD SERIES



RoHS  
Compliant

## FEATURES:

- Based on a proprietary digital multiplier
- Tri-State Output
- Low Phase Noise and Jitter
- 2.5V to 3.3V +/- 5% operation
- Ceramic SMD, low profile package
- 156.25MHz, 187.5MHz, and 212.5MHz applications

## APPLICATIONS:

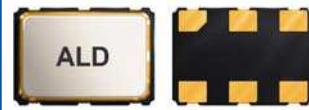
- SONET, xDSL
- SDH, CPE
- STB

## STANDARD SPECIFICATIONS:

### PARAMETERS

ABRACON P/N:	ALD Series
Frequency range:	750 kHz to 800 MHz
Operating temperature:	0° C to + 70° C (see options)
Storage temperature:	- 55° C to + 125° C
Overall frequency stability:	± 50 ppm max. (see options)
Supply voltage (Vdd):	3.3V ±10% (see options)
Jitter:	RMS phase jitter 3ps typ., <5ps max. (12KHz - 20MHz) Period jitter peak to peak ,35ps typical
Low Phase Noise:	-109 dBc/Hz @ 1kHz Offset from 622.08MHz -110 dBc/Hz @ 10kHz Offset from 622.08MHz -109 dBc/Hz @ 100KHz Offset from 622.08MHz -112 dBc/Hz @ 1kHz Offset from 155.52MHz -125 dBc/Hz @ 10kHz Offset from 155.52MHz -123 dBc/Hz @ 100KHz Offset from 155.52MHz
Tristate Function:	"1" (V <sub>IH</sub> ≥ 0.7*Vdd) or open: Oscillation "0" (V <sub>IL</sub> < 0.3*Vdd): No Oscillation / Hi Z
<b>PECL:</b>	Supply current (I <sub>DD</sub> ): <b>65mA max (for 750kHz &lt; Fo &lt; 96MHz), 100mA max (96MHz ≤ Fo &lt; 800MHz)</b> Output Logic High: <b>V<sub>dd</sub>-1.025V min, V<sub>dd</sub>-0.880V max.</b> Output Logic Low: <b>V<sub>dd</sub>-1.810V min. V<sub>dd</sub>-1.620V max.</b> Symmetry (Duty Cycle): <b>45% min, 50% typ, 55% max,</b> Rise time: <b>0.85ns</b> Fall time: <b>0.85ns</b>
<b>LVDS</b>	Supply current (I <sub>DD</sub> ): <b>65mA max (for 750kHz &lt; Fo &lt; 96MHz), 100mA max (96MHz ≤ Fo &lt; 800MHz)</b> Output Clock Duty Cycle @ 1.25V: <b>45% min, 50% typical, 55% max</b> Output Differential Voltage (V <sub>OD</sub> ): <b>247mV min, 355mV typical, 454mV max</b> VDD Magnitude Change (ΔV <sub>OD</sub> ): <b>-50mV min, 50mV max</b> Output High Voltage : <b>V<sub>OH</sub> = 1.4V typical, 1.6V max.</b> Output Low Voltage : <b>V<sub>OL</sub> = 0.9V min, 1.1V typical</b> Offset Voltage [R <sub>L</sub> = 100Ω]: <b>V<sub>OS</sub> = 1.125V min, 1.2V typical, 1.375V max</b> Offset Magnitude Change [R <sub>L</sub> = 100Ω]: <b>ΔV<sub>OS</sub> = 0mV min, 3mV typical, 25mV max</b> Power-off Leakage (I <sub>OXD</sub> ) [Vout=VDD or GND, VDD=0V] = <b>±1μA typical, ±10μA max.</b> Differential Clock Rise Time (t <sub>r</sub> ) [R <sub>L</sub> =100Ω, CL=10pF]: <b>0.2nS min, 0.7nS typical, 1.0nS,max</b> Differential Clock Fall Time (t <sub>f</sub> ) [R <sub>L</sub> =100Ω, CL=10pF]: <b>0.2nS min, 0.7nS typical, 1.0nS max</b>
<b>CMOS:</b>	Supply current (I <sub>DD</sub> ): <b>15mA max (for 750kHz &lt; Fo &lt; 24MHz), 30mA max (for 24MHz ≤ Fo &lt; 96MHz), 65mA max (96MHz ≤ Fo &lt; 800MHz)</b> Output Clock Rise/ Fall Time [10%~90% VDD with 10pF load]: <b>5.0ns max (for 750kHz &lt; Fo &lt; 24MHz) 5.0ns max (for 24MHz ≤ Fo &lt; 800MHz)</b> Output Clock Duty Cycle [Measured @ 50% VDD]: <b>45% min, 50% typical, 55% max</b>

# PECL/LVDS/CMOS OUTPUT SMD CRYSTAL CLOCK OSCILLATOR



5.0 x 7.0 x 1.8mm

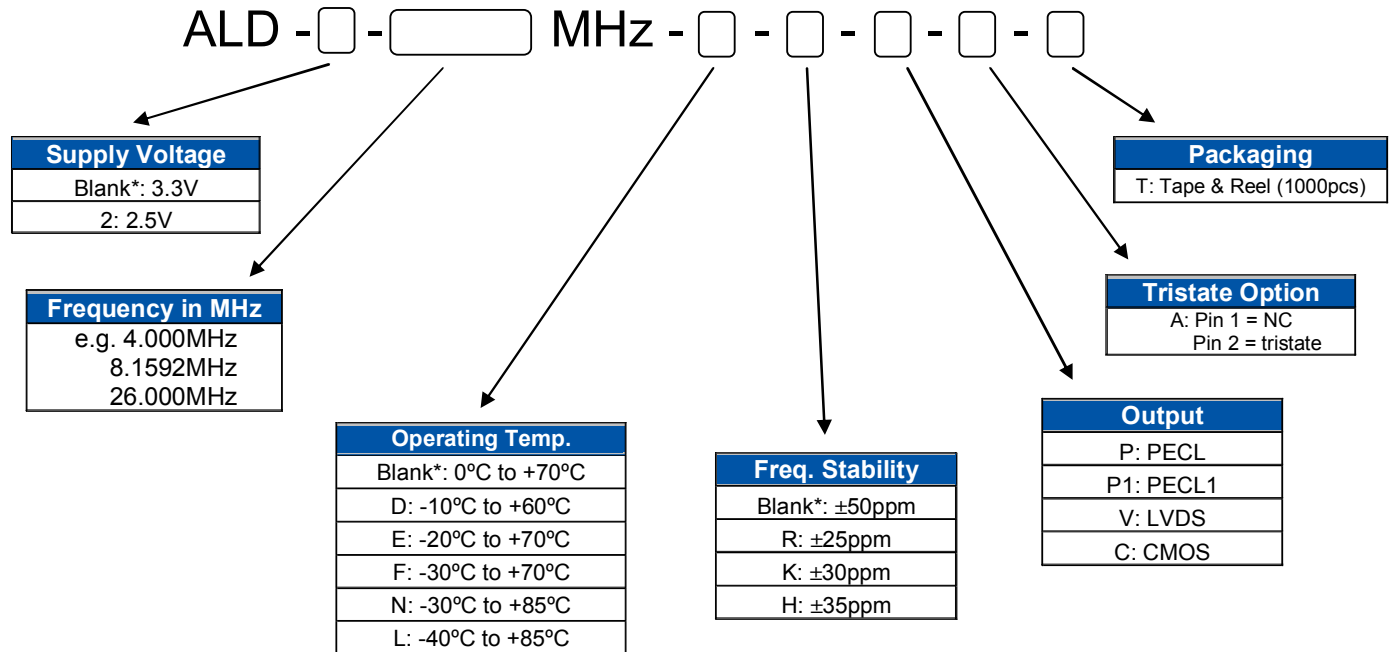
ALD SERIES



RoHS Compliant

## OPTIONS AND PART IDENTIFICATION

(Left blank if standard)



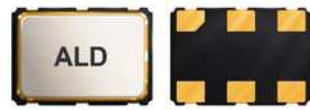
\*Standard specification

### TRI-STATE PIN OUT DESCRIPTION:

OUTPUT TYPE OPTION		PIN 1 logic level*	Output State
P	PECL	0 (Default)	Enabled
		1	Tri-state
P1	PECL1	1 (Default)	Enabled
		0	Tri-state
V	LVDS	0	Tri-state
		1(Default)	Enabled
C	CMOS	0	Tri-state
		1(Default)	Enabled

\*Connect to VDD for logic level "1", connect to ground for logic level "0".

# PECL/LVDS/CMOS OUTPUT SMD CRYSTAL CLOCK OSCILLATOR



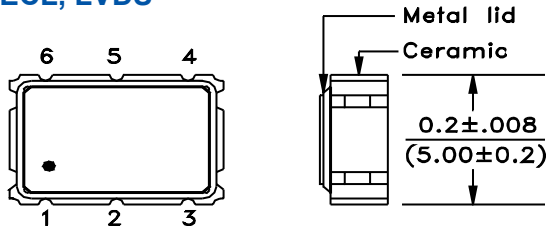
5.0 x 7.0 x 1.8mm

ALD SERIES

**Pb** **RoHS**  
Compliant

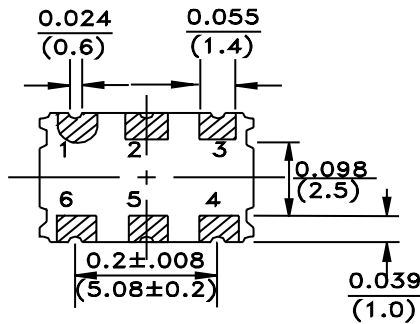
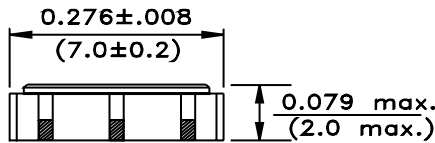
## OUTLINE DIMENSIONS:

### PECL, LVDS



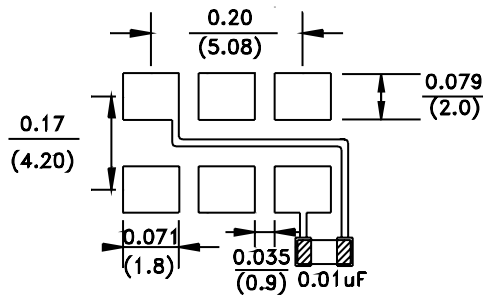
PIN #	Name	DESCRIPTION
1	Tri-state / NC	Tristate or No Connect
2	NC / Tristate	No Connect / Tristate
3	GND	Ground
4	Q	PECL, LVDS
5	$\bar{Q}$	Complimentary PECL, LVDS
6	V <sub>DD</sub>	VDD Connection.

Note: Recommend using an approximately 0.01uF bypass capacitor between PIN 3 and 6.

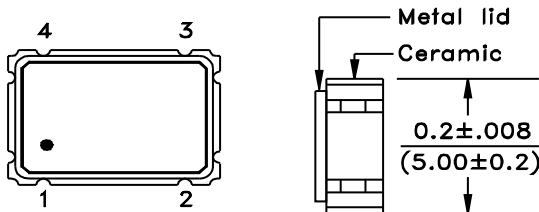


Bottom view

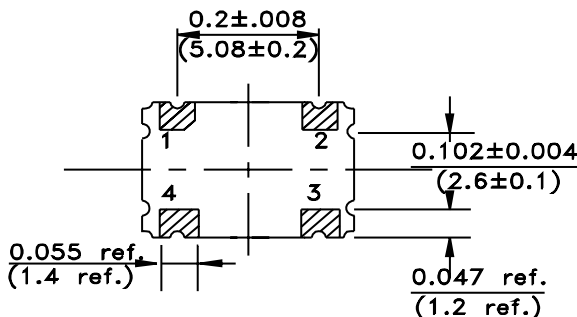
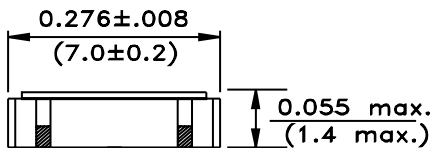
### Recommended land pattern



### CMOS

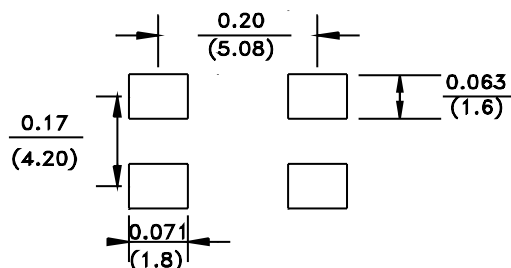


PIN #	Name
1	Tri-state
2	GND
3	OUTPUT
4	Vdd



Bottom view

### Recommended land pattern



Dimensions: inches (mm)

# PECL/LVDS/CMOS OUTPUT SMD CRYSTAL CLOCK OSCILLATOR



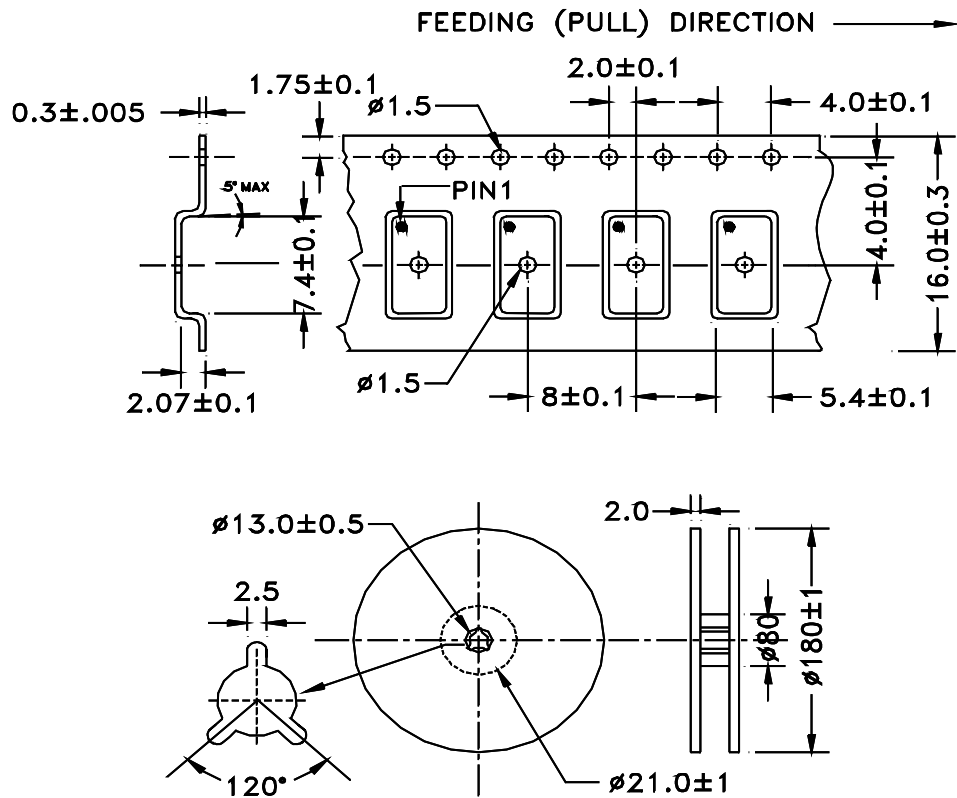
5.0 x 7.0 x 1.8mm

ALD SERIES

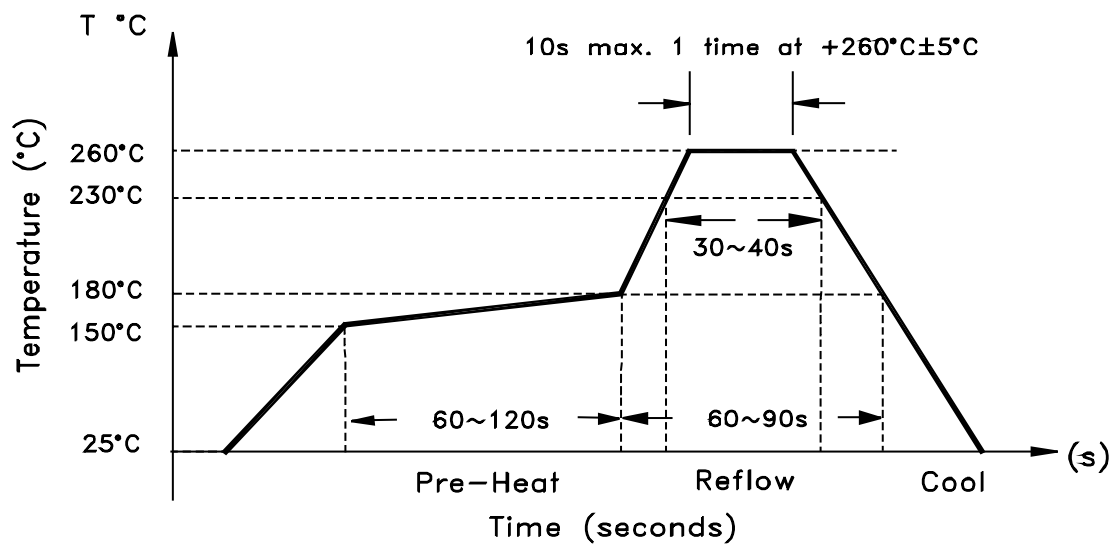
**Pb** **RoHS**  
Compliant

➤ **TAPE AND REEL:** T= tape and reel (1,000pcs/reel)

Dimension : mm



➤ **REFLOW PROFILE:**



**NOTE:** Abracon manufactured products are intended for general commercial and industrial use. For applications requiring high reliability and/or presenting extreme operating environment, written consent & authorization from Abracon is required.

ABRACON IS  
ISO9001:2008  
CERTIFIED



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