

General Description

The AO4440 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

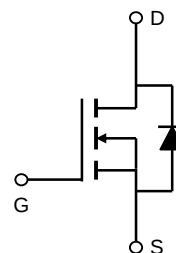
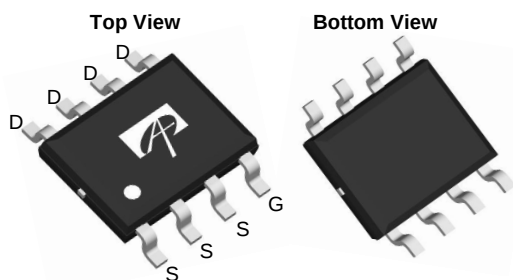
Product Summary

V_{DS} (V) = 60V
 I_D = 5A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 55m Ω (V_{GS} = 10V)
 $R_{DS(ON)}$ < 75m Ω (V_{GS} = 4.5V)

100% UIS Tested
 100% Rg Tested



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	I_D	5	A
	$T_A=70^\circ\text{C}$	4	
Pulsed Drain Current ^B	I_{DM}	20	
Power Dissipation	P_D	2.5	W
	$T_A=70^\circ\text{C}$	1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	38	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		69	80	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	24	30	$^\circ\text{C/W}$

N Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	2.3	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5A T _J =125°C		42 75	55	mΩ
		V _{GS} =4.5V, I _D =4A		54	75	
						mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =5A		11		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.78	1	V
I _S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		450	540	pF
C _{oss}	Output Capacitance			60		pF
C _{rss}	Reverse Transfer Capacitance			25		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.65	2	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =5A		8.5	10.5	nC
Q _{g(4.5V)}	Total Gate Charge			4.3	5.5	nC
Q _{gs}	Gate Source Charge			1.6		nC
Q _{gd}	Gate Drain Charge			2.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =6Ω, R _{GEN} =3Ω		5.1	7	ns
t _r	Turn-On Rise Time			2.6	4	ns
t _{D(off)}	Turn-Off DelayTime			15.9	20	ns
t _f	Turn-Off Fall Time			2	3	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =5A, dI/dt=100A/μs		25.1	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5A, dI/dt=100A/μs		28.7		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating. Rev2: Nov. 2010

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

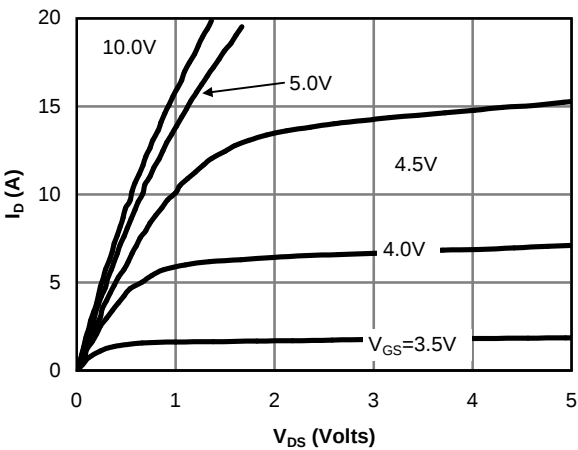


Fig 1: On-Region Characteristics

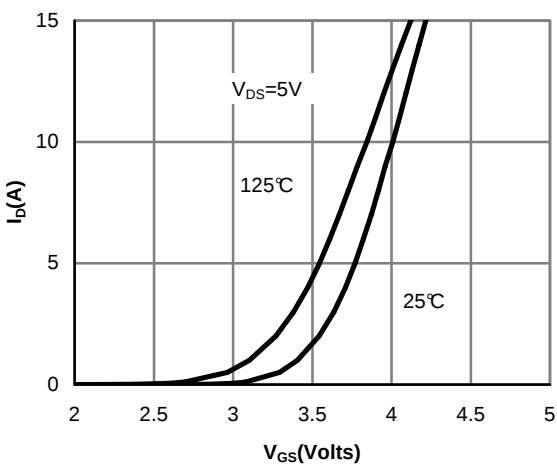


Figure 2: Transfer Characteristics

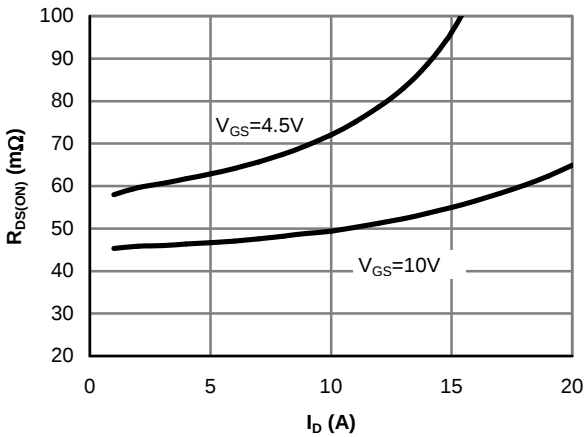


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

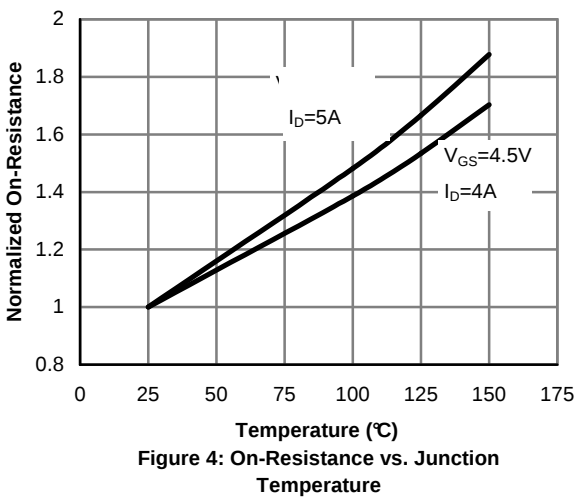


Figure 4: On-Resistance vs. Junction Temperature

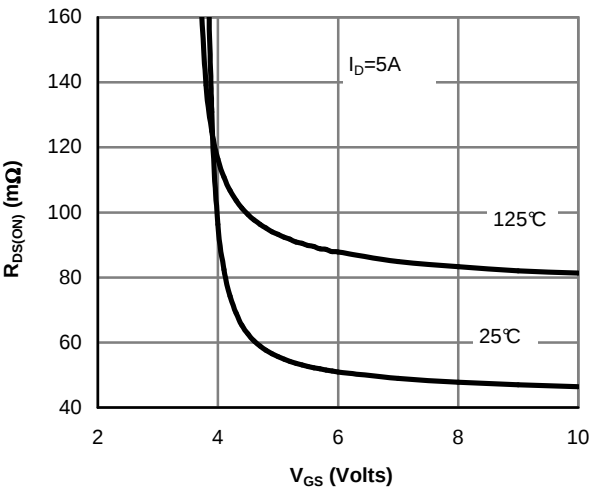


Figure 5: On-Resistance vs. Gate-Source Voltage

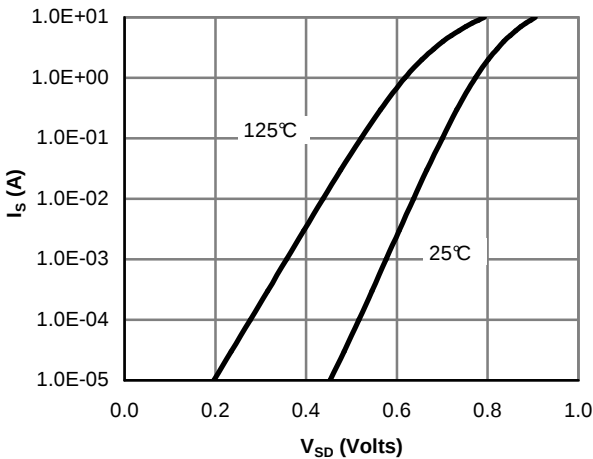


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL

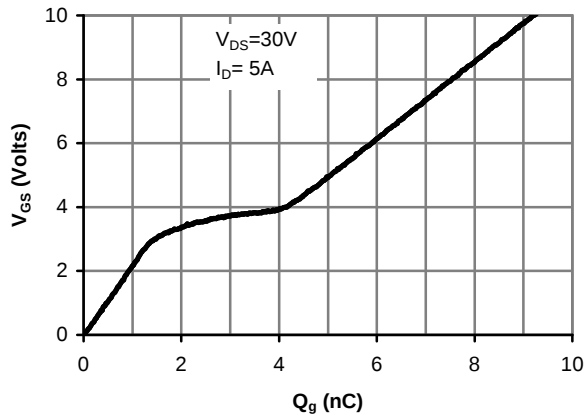


Figure 7: Gate-Charge Characteristics

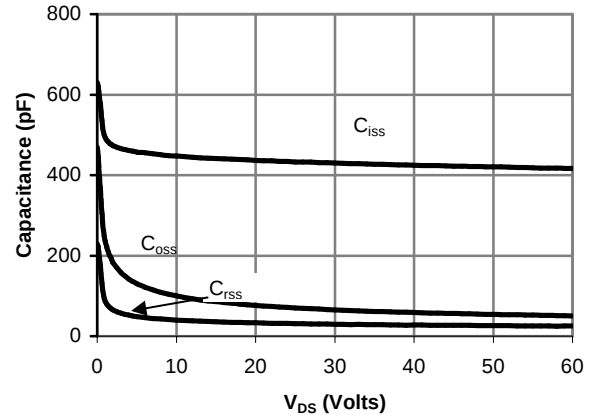


Figure 8: Capacitance Characteristics

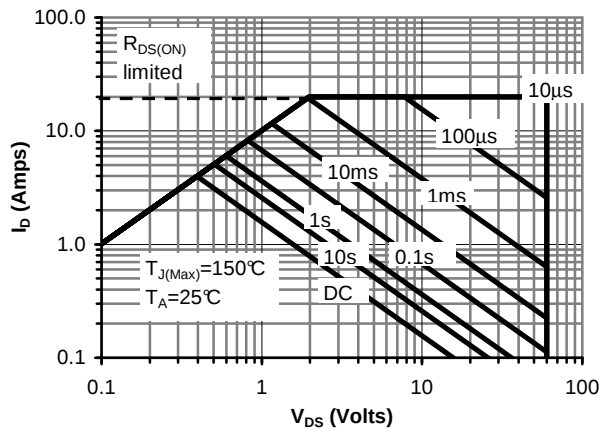


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

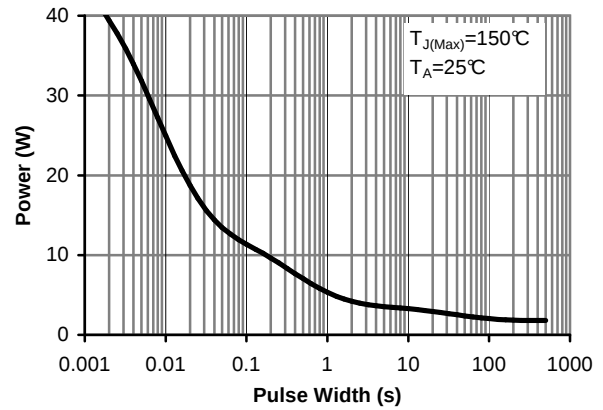


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

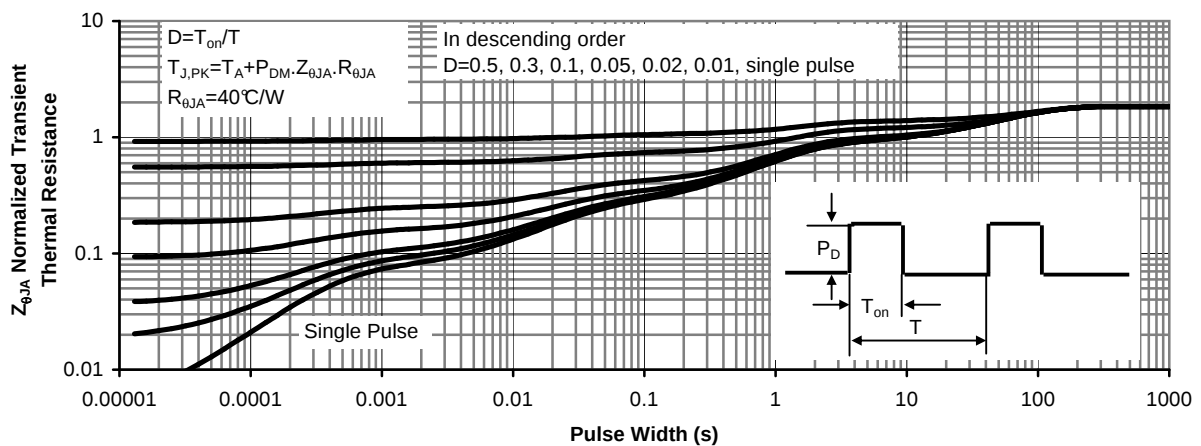


Figure 11: Normalized Maximum Transient Thermal Impedance