

Power Operational Amplifier

FEATURES

- HIGH INTERNAL DISSIPATION — 125 Watts
- HIGH VOLTAGE, HIGH CURRENT — 100V, 10A
- HIGH SLEW RATE — 10V/ μ s
- 4 WIRE CURRENT LIMIT SENSING
- OPTIONAL BOOST VOLTAGE INPUTS

APPLICATIONS

- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ± 45 V
- INDUSTRIAL AUDIO
- PACKAGE OPTION - DIP10 - DUAL-IN-LINE

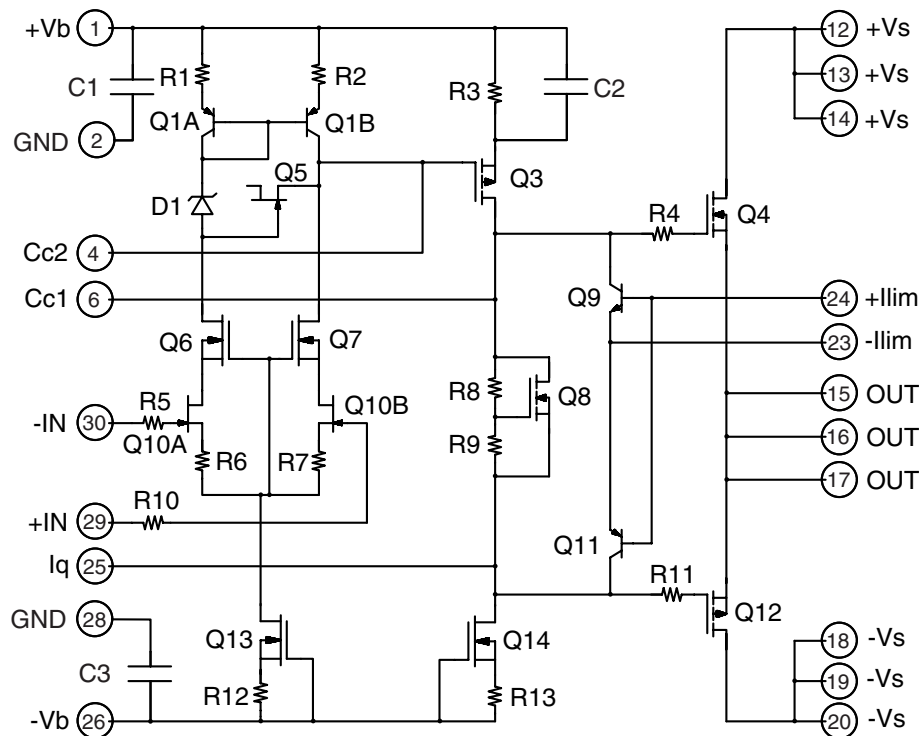
DESCRIPTION

The MP39 is a cost-effective high voltage MOSFET power operational amplifier constructed with surface mount components on a thermally conductive but electrically isolated substrate.

While the cost is low the MP39 offers many of the same features and performance specifications found in much more expensive hybrid power amplifiers.

The metal substrate allows the MP39 to dissipate power up to 125 watts and its power supply voltages can range up to ± 50 Volts (100V total). Optional boost voltage inputs allow the small signal portion of the amplifier to operate at higher supply voltages than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high current for extra efficient operation. External compensation tailors performance to the user needs. A four-wire sense technique allows current limiting without the need to consider internal or external milli-ohm parasitic resistance in the output line. An Iq pin is available which can be used to shut off the quiescent current in the output stage. The output stage then operates class C and lowers quiescent power dissipation. This is useful in applications where output crossover distortion is not important.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			100	V
BOOST VOLTAGE			$\pm V_S \pm 20$	V
OUTPUT CURRENT, within SOA			25	A
POWER DISSIPATION, internal			125	W
INPUT VOLTAGE, differential		-20	+20	V
INPUT VOLTAGE, common mode		$-V_B$	$+V_B$	V
TEMPERATURE, pin solder - 10s			200	°C
TEMPERATURE, junction (Note 2)			175	°C
TEMPERATURE, storage		-40	+105	°C
OPERATING TEMPERATURE RANGE, case		-40	+85	°C

SPECIFICATIONS

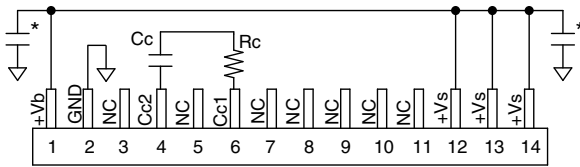
Parameter	Test Conditions (Note 1)	MP38			MP38A			Units
		Min	Typ	Max	Min	Typ	Max	
INPUT								
OFFSET VOLTAGE, initial			5	10		*	3	mV
OFFSET VOLTAGE, vs. temperature	Full temp range		50			*		$\mu\text{V}/^\circ\text{C}$
OFFSET VOLTAGE, vs. supply			15			*		$\mu\text{V}/\text{V}$
OFFSET VOLTAGE, vs. power	Full temp range		30			*		$\mu\text{V}/\text{W}$
BIAS CURRENT, initial			10	200		*	100	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		*	30	pA
INPUT IMPEDANCE, DC			10^{10}			*		Ω
INPUT CAPACITANCE			20			*		pF
COMMON MODE VOLTAGE RANGE	Full temp range	$\pm V_B \mp 15$	$\pm V_B \mp 12$		*	*		V
COMMON MODE REJECTION, DC	Full temp, range, $V_{CM} = \pm 20\text{V}$	86	98		*	*		dB
INPUT NOISE	100kHz BW, $R_S = 1\text{K}\Omega$		10			*		μVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temp range, $C_C = 100\text{pF}$	94	113		*	*		dB
GAIN BANDWIDTH PRODUCT	$I_O = 10\text{A}$		2			*		MHz
POWER BANDWIDTH	$R_L = 10\Omega$, $V_O = 90V_{P-P}$ $C_C = 100\text{pF}$		40			*		kHz
PHASE MARGIN	Full temp range		60			*		°

Parameter	Test Conditions (Note 1)	MP38			MP38A			Units
		Min	Typ	Max	Min	Typ	Max	
OUTPUT								
VOLTAGE SWING	$I_o=10A$	$\pm V_s \mp 8.8$	$\pm V_s \mp 6.0$		*	*		V
VOLTAGE SWING	$\pm V_B = \pm V_S \pm 10V$, $I_o=10A$	$\pm V_s \mp 6.8$	$\pm V_s \mp 1.1$		*	*		V
SETTLING TIME to .1%	$A_v=+1$, 10V step, $R_L=4\Omega$		2.5			*		μS
SLEW RATE	$A_v=-10$, $C_c=100pF$	10			*			V/ μS
CAPACITIVE LOAD	Full temp range, $A_v=+1$	10			*			nF
RESISTANCE			4			*		Ω
CURRENT, CONTINUOUS				10			11	A
POWER SUPPLY								
VOLTAGE	Full temp range	± 15	± 40	± 50	*	*	*	V
CURRENT, quiescent, boost supply				22			*	mA
CURRENT, quiescent, total				26			*	mA
THERMAL								
RESISTANCE, AC, junction to case (Note 3)	Full temp range, $F>60Hz$.9			*	$^{\circ}C/W$
RESISTANCE, DC, junction to case	Full temp range, $F<60Hz$			1.2			*	$^{\circ}C/W$
RESISTANCE, junction to air (Note 4)	Full temp range		12			*		$^{\circ}C/W$
TEMPERATURE RANGE, case	Meets full range specification	-40		+85	*		*	$^{\circ}C$

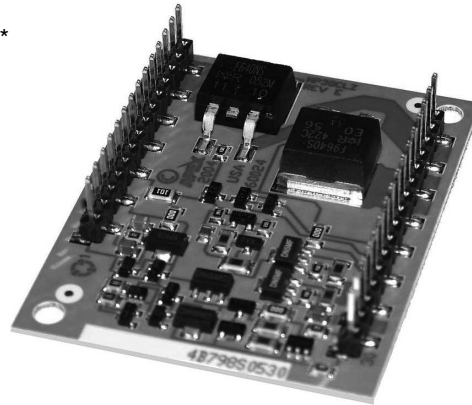
- NOTES: * The specification of MP39A is identical to the specification for MP39 in applicable column to the left.
1. Unless otherwise noted: $T_c = 25^{\circ}C$, $R_c = 100\Omega$, $C_c = 470pF$. DC input specifications are \pm value given. Power supply voltage is typical rating. $\pm V_B = \pm V_S$.
 2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
 3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
 4. The MP39 must be used with a heat sink or the quiescent power may drive the unit to junction temperatures higher than $175^{\circ}C$.

CAUTION The MP39 is constructed from MOSFET transistors. ESD handling procedures must be observed.

EXTERNAL CONNECTIONS



COMPONENT SIDE VIEW



30-pin DIP PACKAGE STYLE CL



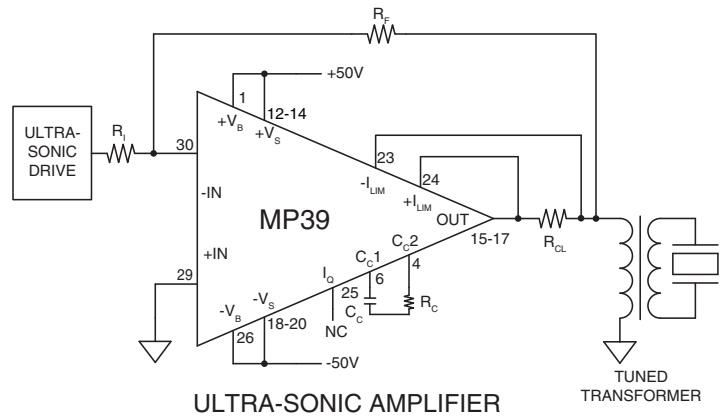
* SEE "BYPASSING" PARAGRAPH
Phase Compensation

Gain	Cc	Rc
1	470pF	100Ω
≥ 3	220pF	Short
≥ 10	100pF	Short

TYPICAL APPLICATION

Ref: Application Note 25

The high power bandwidth and high voltage output of the MP39 allows driving ultra-sonic transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the MP39.



ULTRA-SONIC AMPLIFIER

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. **For the current limit to work correctly pin 24 must be connected to the amplifier output side and pin 23 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.** This connection will bypass any parasitic resistances, R_p, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.7}{I_{LIMIT}}$$

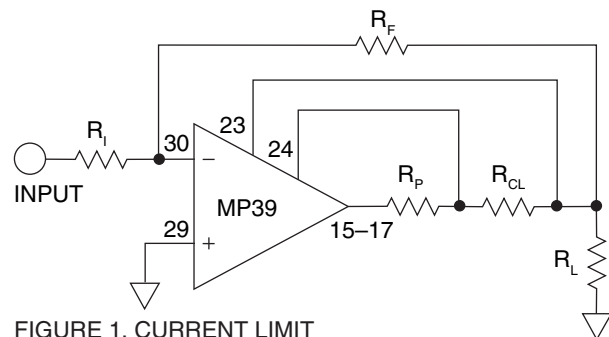
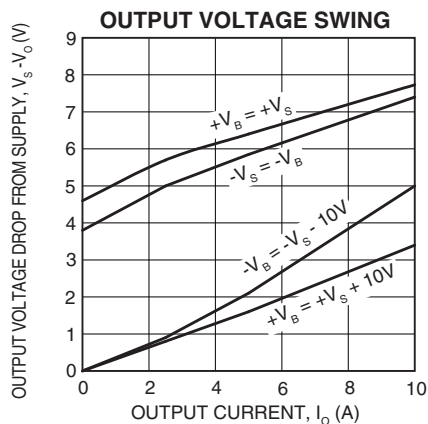
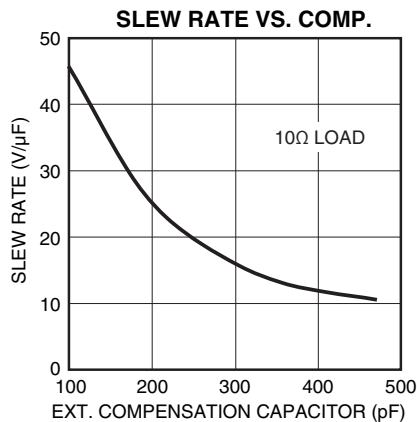
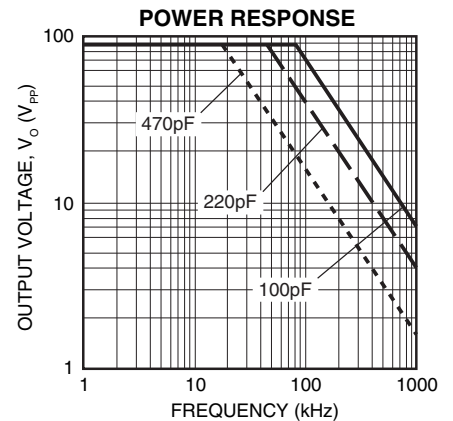
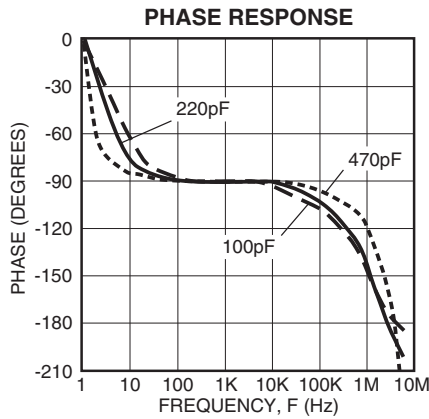
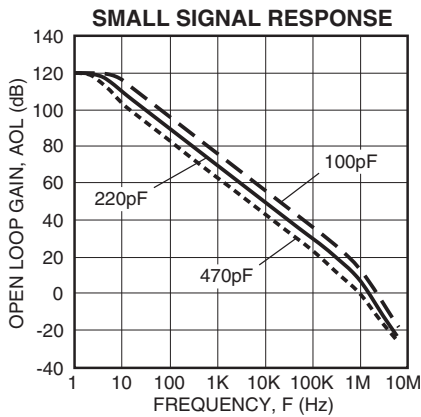
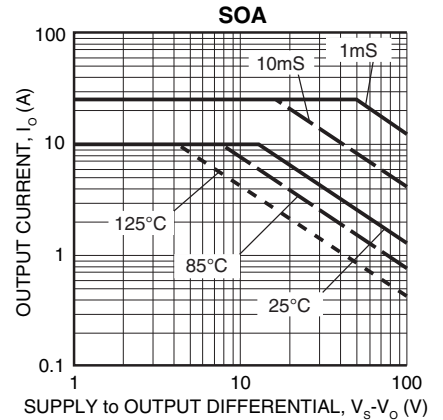
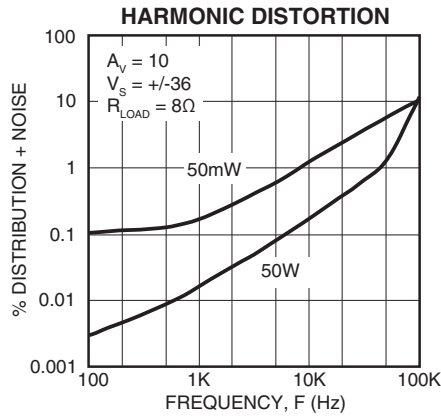
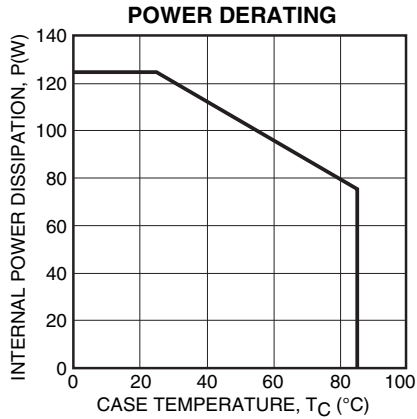


FIGURE 1. CURRENT LIMIT

TYPICAL PERFORMANCE GRAPHS



BOOST OPERATION

With the V_B feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_S$ (pins 12-14) and $-V_S$ (pins 18-20) are connected to the high current output stage. An additional 10V on the V_B pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swing to the supply rails is not required the $+V_B$ and $+V_S$ pins must be strapped together as well as the $-V_B$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

BYPASSING

Proper bypassing of the power supply pins is crucial for proper operation. Bypass the $\pm V_s$ pins with a aluminum electrolytic capacitor with a value of at least $10\mu\text{F}$ per amp of expected output current. In addition a $.47\mu\text{F}$ to $1\mu\text{F}$ ceramic capacitor should be placed in parallel with each aluminum electrolytic capacitor. Both of these capacitors have to be placed as close to the power supply pins as physically possible. If not connected to the V_s pins (See BOOST OPERATION) the V_b pins should also be bypassed with a $.47\mu\text{F}$ to $1\mu\text{F}$ ceramic capacitor.

USING THE I_q PIN FUNCTION

Pin 25 (I_q) can be tied to pin 6 (C_{c1}) to eliminate the class AB biasing current from the output stage. Typically this would remove 1-4 mA of quiescent current. The resulting decrease in quiescent power dissipation may be important in some applications. Note that implementing this option will raise the output impedance of the amplifier and increase crossover distortion as well.

COMPENSATION

The external compensation components C_c and R_c are connected to pins 4 and 6. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate.

APPLICATION REFERENCES

For additional technical information please refer to the following application notes.

- AN01 General Operating Considerations
- AN11 Thermal Techniques
- AN38 Loop Stability with Reactive Loads

CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.

For inquiries via email, please contact apex.support@cirrus.com.

International customers can also request support by contacting their local Cirrus Logic Sales Representative.

To find the one nearest to you, go to www.cirrus.com

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs, Apex Precision Power, Apex and the Apex Precision Power logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.
