TMC34NP-PSO

Manual

Complementary 30V Enhancement Mode MOSFET
In Miniature Package
For use with e.g. TMC239 or TMC249

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TRINAMIC
MOTION CONTROL

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1 Features

Packaged in the low thermal resistance 3.3mm x 3.3mm PowerPAK 1212-8 with low 1.07 mm profile outline this 30V N and P channel Trench MOSFET utilizes a unique structure combining the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage power management applications, such as stepper motor drivers. Its low gate charge makes it an ideal power driver for the TMC239A and TMC249A family of stepper motor drivers. Using only four of these transistor packages, and the miniaturized TMC239A-LA or TMC249A-LA, a 2A stepper driver can be build in the size of a stamp. Up to 4A peak (2.8A RMS) continuous current are possible.

SUMMARY

- N-Channel: $V_{(BR)DSS}$= 30V,
  V_{GS}= 10V : $R_{DS(on)}$= 0.035Ω; I_D= 7.7A
  V_{GS}= 4.5V: $R_{DS(on)}$= 0.050Ω; I_D= 6.5A
- P-Channel: $V_{(BR)DSS}$= -30V,
  V_{GS}= -10V: $R_{DS(on)}$= 0.051Ω; I_D= -6.4A
  V_{GS}= -6V : $R_{DS(on)}$= 0.075Ω; I_D= -5.3A

Applications

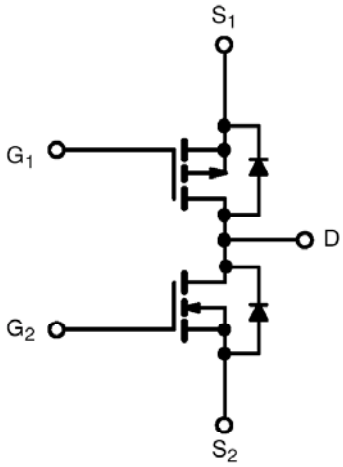
- Stepper motor driver stages

Highlights

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- High motor current
- Good thermal characteristics

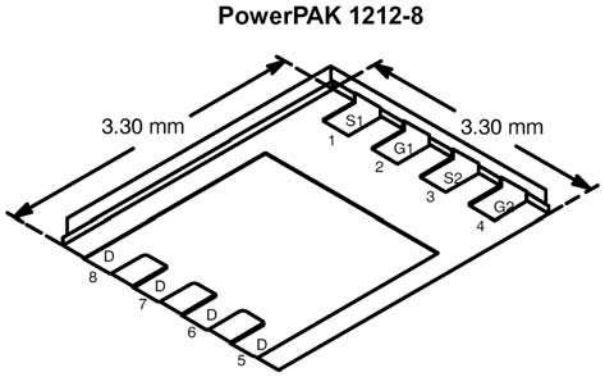
Other

- 3.3mm x 3.3mm PowerPAK package
- RoHS compliant



N&P-Channel

Pinout / Dimensions



Bottom View

Order code	Description
TMC34NP-PSO	Complementary 30V Enhancement Mode MOSFET in PowerPAK 1212-8 package

Table 1.1: Order codes

2 Life support policy

TRINAMIC Motion Control GmbH & Co. KG does not authorize or warrant any of its products for use in life support systems, without the specific written consent of TRINAMIC Motion Control GmbH & Co. KG.

Life support systems are equipment intended to support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.

3 Operational Ratings

3.1 Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	N-Channel		P-Channel		Unit
		10secs	Steady state	10secs	Steady state	
V_{DS}	Drain-source voltage	30		-30		V
V_{GS}	Gate-source voltage	± 20		± 25		
I_D	Continuos drain current [a] T_A=25°C T_A=70°C	 7.7 4.7	 5.4 4.3	 -6.4 -5.1	 -4.5 -3.6	A
I_{DM}	Pulsed drain current	25		-25		
I_S	Continuous source current (diode) [a]	2.6	1.3	-2.6	-1.3	
P_D	Maximum power dissipation [a] T_A=25°C T_A=70°C	 3.1 2	 1.6 1.0	 3.1 3	 1.6 1.0	W
T_J,T_{STG}	Operating junction and storage temperature range	-55 to 150				°C
	Soldering recommendations (peak temperature) [b] [c]	260				

Table 3.1: Absolute Maximum Ratings

3.2 Thermal Resistance

Symbol	Parameter		Typical	Maximum	Unit
R_{THJA}	Junction to ambient [a]	t ≤ 10 sec	32	40	°C/W
		Steady state	65	81	
R_{THJC}	Junction to foot	Steady state	5	6.3	

Table 3.2: Thermal Resistance

[a] Surface mounted on "1 x 1" FR4 board.
[b] The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
[c] Rework conditions: manual soldering with soldering iron is not recommended for leadless components.

3.3 Characteristics

T_A = 25°C unless otherwise noted

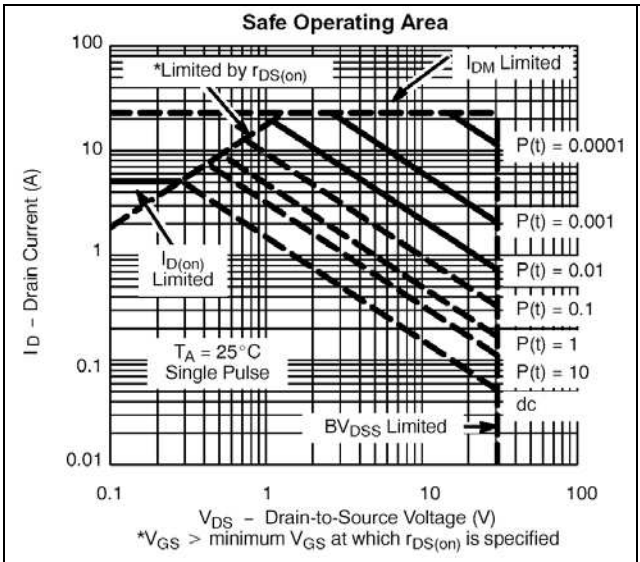


Figure 3.1: N-channel Safe Operating Area

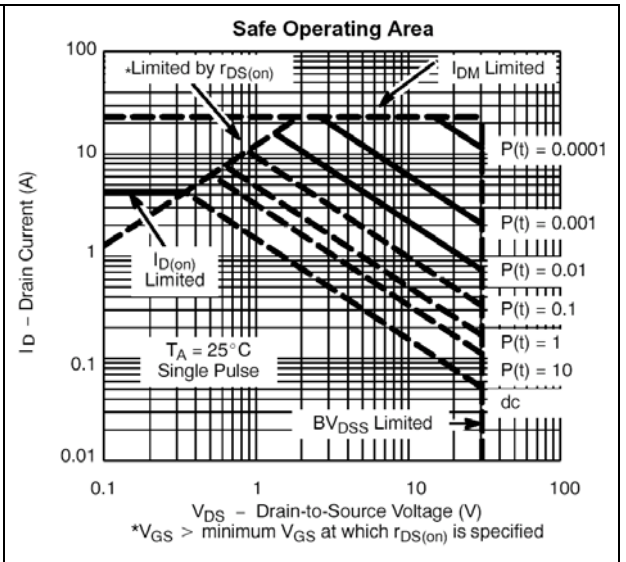


Figure 3.2: P-channel Safe Operating Area

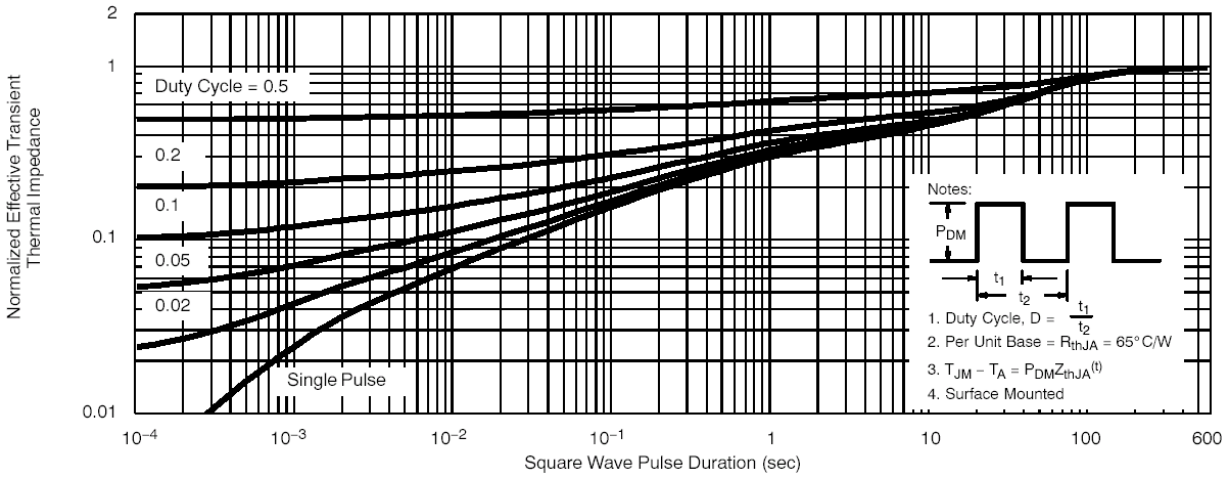


Figure 3.3: Normalized Thermal Transient Impedance, Junction-to-Ambient

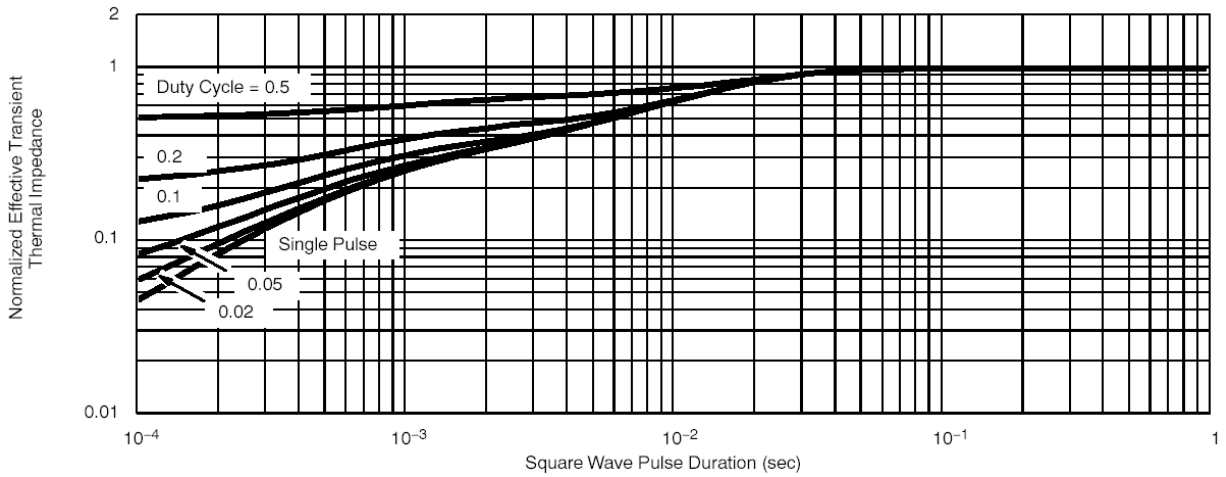


Figure 3.4: Normalized Thermal Transient Impedance, Junction-to-Case

4 N-Channel

4.1 Electrical Characteristics

at T_J = 25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
STATIC						
I_{DSS}	Zero gate voltage drain current			1	µA	V_{DS}= 30V, V_{GS}= 0V
				5		V_{DS}= 30V, V_{GS}= 0V, T_J= 55°C
I_{GSS}	Gate-body leakage			±100	nA	V_{GS}= ±20V, V_{DS}= 0V
$V_{GS(th)}$	Gate-source threshold voltage	1.0		3	V	I_D= 250µA, V_{DS}= V_{GS}
$I_{D(on)}$	On-state drain current [a]	25			A	V_{DS} ≤ 5V, V_{GS}= 10V
$R_{DS(on)}$	Drain-source on-state resistance [a]		0.028 0.040	0.035 0.050	Ω	V_{GS}= 10V, I_D= 7.7A V_{GS}= 4.5V, I_D= 6.5A
g_{fs}	Forward transconductance [a]		15		S	V_{DS}= 15V, I_D= 7.7A
V_{SD}	Diode forward voltage [a]		0.80	1.2	V	I_S= 1.7A, V_{GS}= 0V
DYNAMIC [b]						
Q_g	Total gate charge		9	14	nC	V_{DS}= 15V, V_{GS}= 10V I_D= 7.7A
Q_{gs}	Gate-source charge		2			
Q_{gd}	Gate drain charge		1.3			
R_G	Gate resistance		3		Ω	
$t_{d(on)}$	Turn-on-delay time		10	15	ns	V_{DD}= 15V, I_D= 3A, R_L= 5Ω, R_G= 1Ω, V_{GEN}= 10V
t_r	Rise time		15	25		
$t_{d(off)}$	Turn-off delay time		20	30		
t_f	Fall time		10	15		
t_{rr}	Source-drain reverse recovery time		20	40		I_F= 1.7A, di/dt= 100A/µs

Table 4.1: Electrical Characteristics, N-Channel

[a] Pulse test; pulse width ≤ 300µs, duty cycle ≤ 2%
[b] Guaranteed by design, not subject to production testing

4.2 Typical Characteristics

T_A = 25°C unless otherwise noted

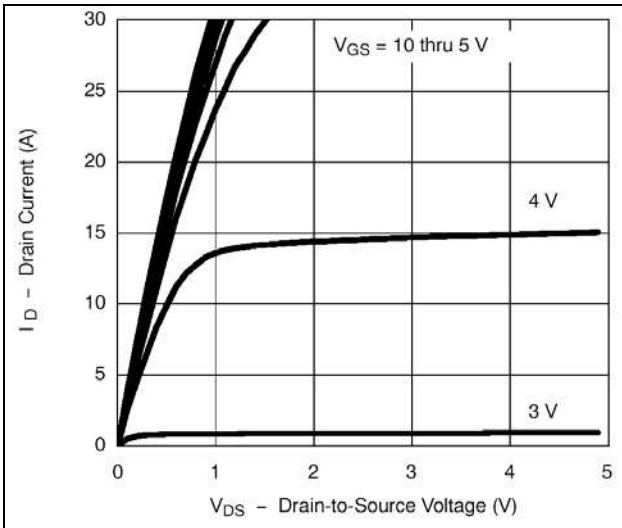


Figure 4.1: Output Characteristics (N)

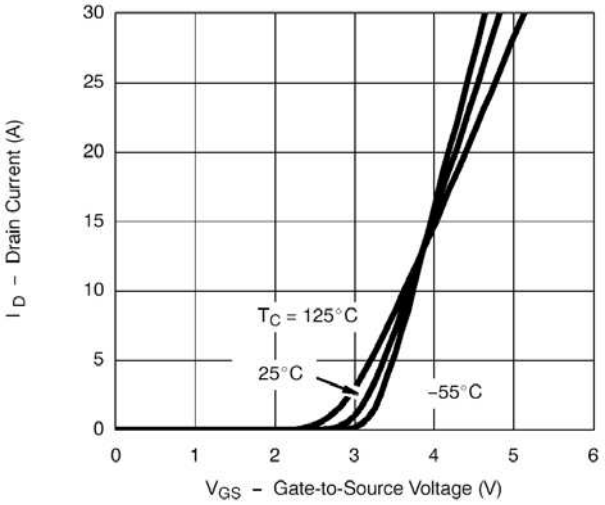


Figure 4.2: Transfer Characteristics (N)

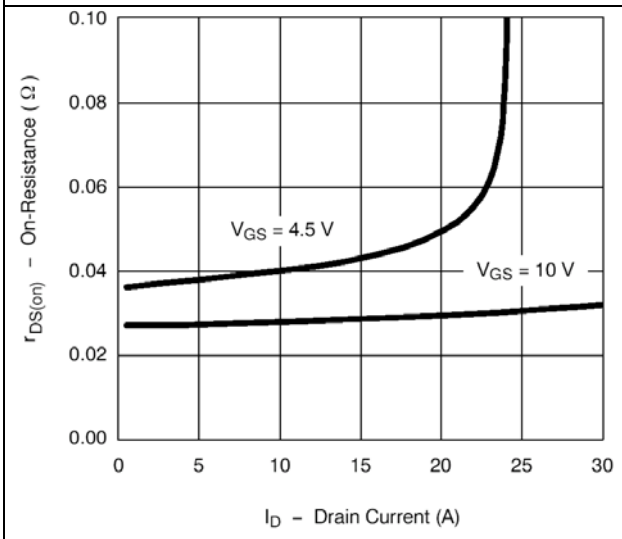


Figure 4.3: On-Resistance vs. Drain current (N)

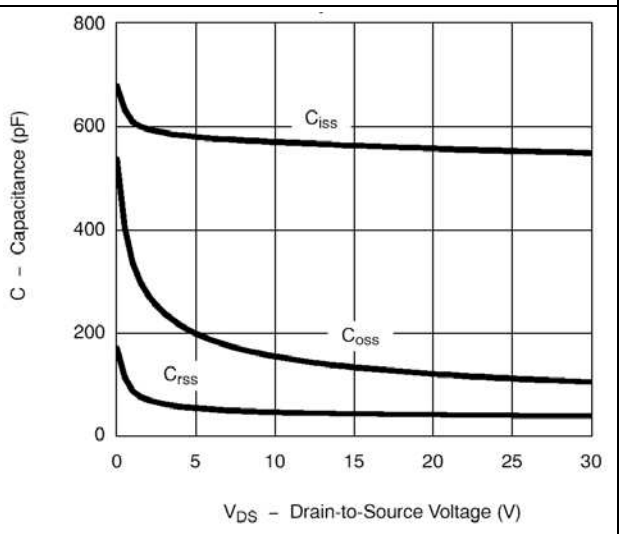


Figure 4.4: Capacitance (N)

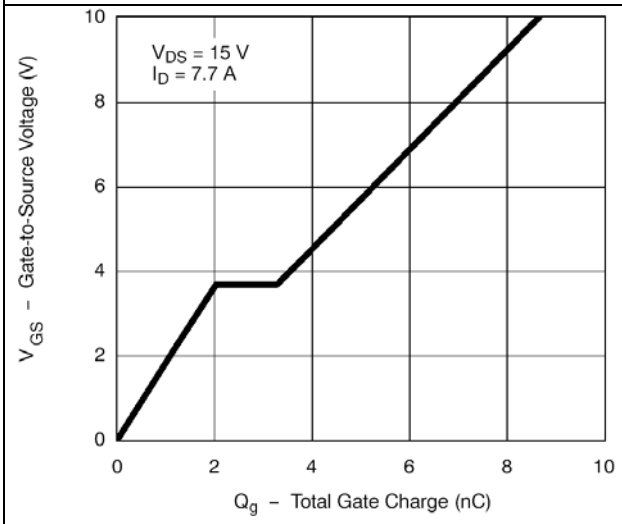


Figure 4.5: Gate Charge (N)

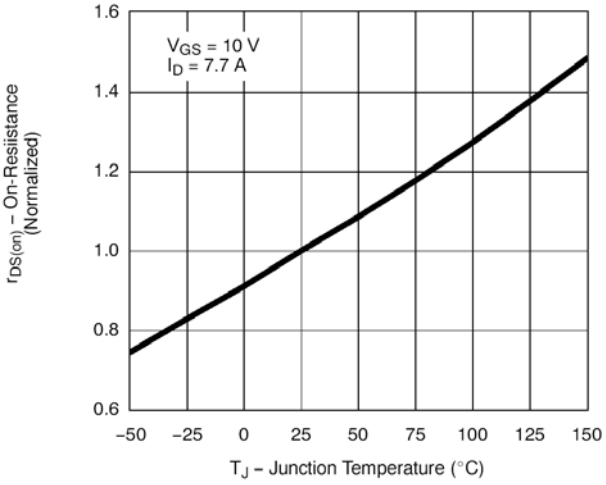


Figure 4.6: On-Resistance vs. Junction Temp. (N)

T_A = 25°C unless otherwise noted

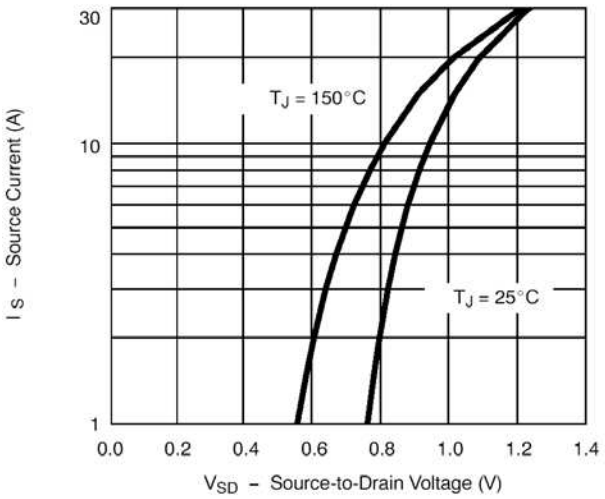


Figure 4.7: Source-Drain Diode Forward Voltage (N)

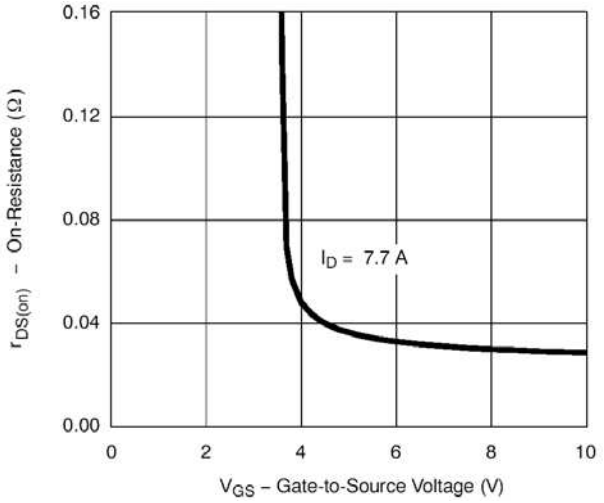


Figure 4.8: On-Resistance vs. Gate-to-Source Voltage (N)

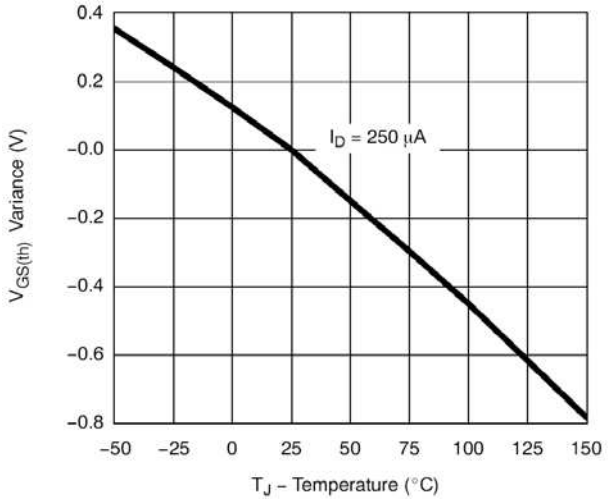


Figure 4.9: Threshold Voltage (N)

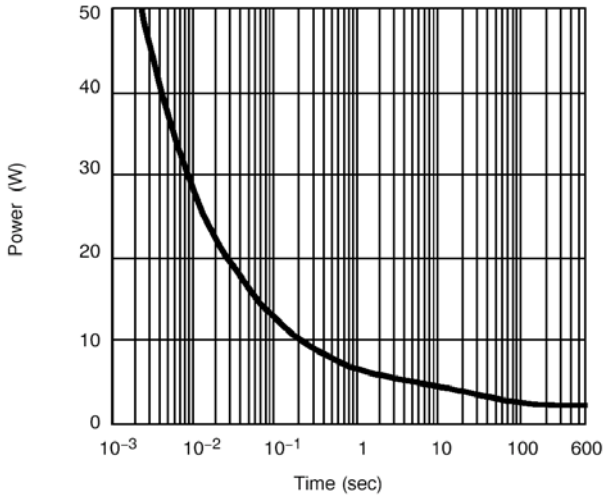


Figure 4.10: Single Pulse Power (N)

5 P-Channel

5.1 Electrical Characteristics

at T_J = 25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
STATIC						
I_{DSS}	Zero gate voltage drain current			-1	µA	V_{DS}= -30V, V_{GS}= 0V
				-5		V_{DS}= -30V, V_{GS}= 0V, T_J= 55°C
I_{GSS}	Gate-body leakage			±200	nA	V_{GS}= ±25V, V_{DS}= 0V
$V_{GS(th)}$	Gate-source threshold voltage	-1.0		-3	V	I_D= -250µA, V_{DS}= V_{GS}
$I_{D(on)}$	On-state drain current [a]	-25			A	V_{DS} ≥ -5V, V_{GS}= -10V
$R_{DS(on)}$	Drain-source on-state resistance [a]		0.041 0.055	0.051 0.075	Ω	V_{GS}= -10V, I_D= -6.4A V_{GS}= -6V, I_D= -5.3A
g_{fs}	Forward transconductance [a]		13		S	V_{DS}= -15V, I_D= 6.4A
V_{SD}	Diode forward voltage [a]		-0.80	-1.2	V	I_S= -1.7A, V_{GS}= 0V
DYNAMIC [b]						
Q_g	Total gate charge		12.5	19	nC	V_{DS}= -15V, V_{GS}= -10V I_D= -6.4A
Q_{gs}	Gate-source charge		2.5			
Q_{gd}	Gate drain charge		3.6			
R_G	Gate resistance		9		Ω	
$t_{d(on)}$	Turn-on-delay time		10	15	ns	V_{DD}= -15V, I_D= -3A, R_L= 5Ω, R_G= 1Ω, V_{GEN}= -10V
t_r	Rise time		20	30		
$t_{d(off)}$	Turn-off delay time		25	40		
t_f	Fall time		30	45		
t_{rr}	Source-drain reverse recovery time		25	50		I_F=-1.7A, di/dt= 100A/µs

Table 5.1: Electrical Characteristics, P-Channel

[a] Pulse test; pulse width ≤ 300µs, duty cycle ≤ 2%
[b] Guaranteed by design, not subject to production testing

5.2 Typical Characteristics

T_A = 25°C unless otherwise noted

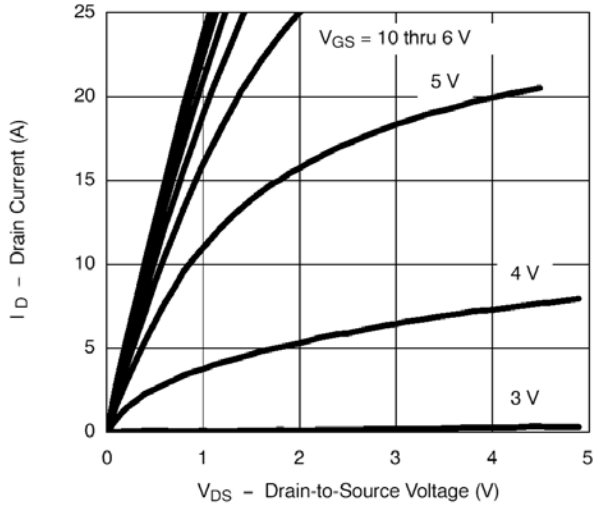


Figure 5.1: Output Characteristics (P)

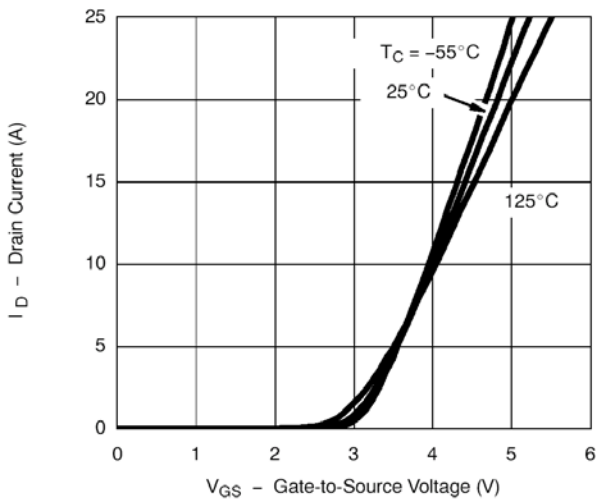


Figure 5.2: Transfer Characteristics (P)

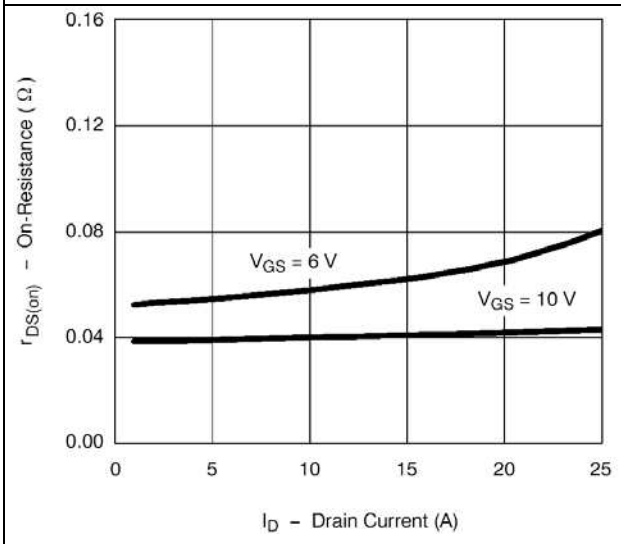


Figure 5.3: On-Resistance vs. Drain Current (P)

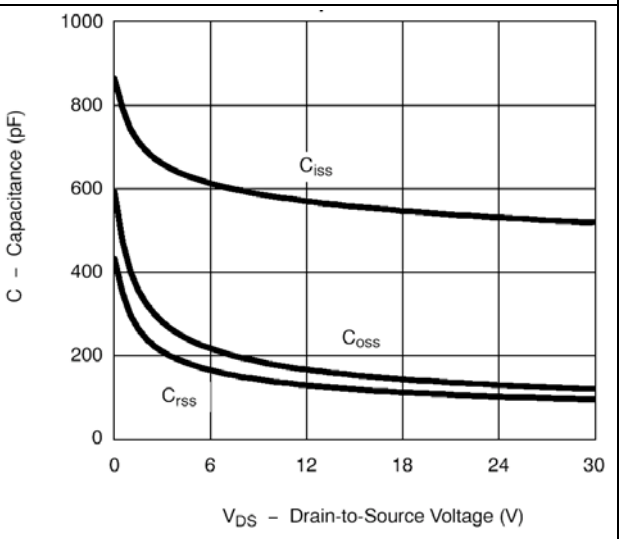


Figure 5.4: Capacitance (P)

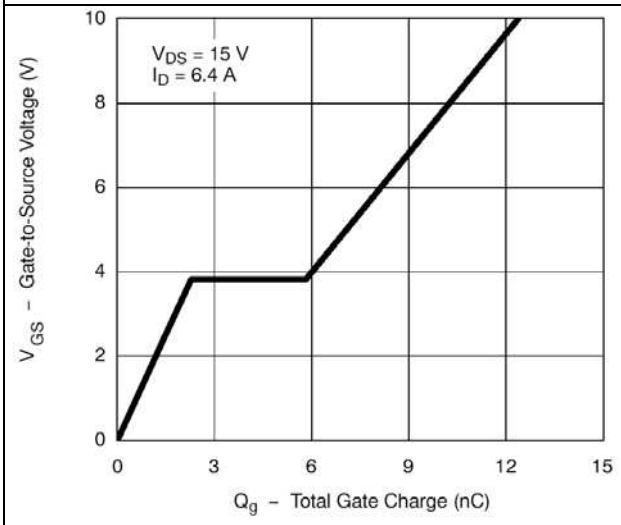


Figure 5.5: Gate Charge (P)

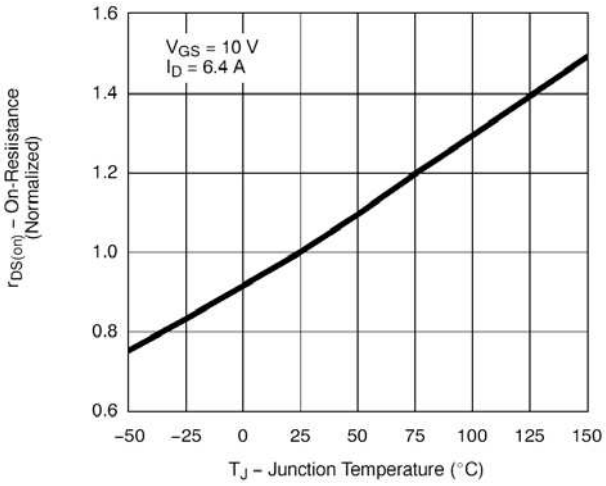


Figure 5.6: On-Resistance vs. Junction Temp. (P)

T_A = 25°C unless otherwise noted

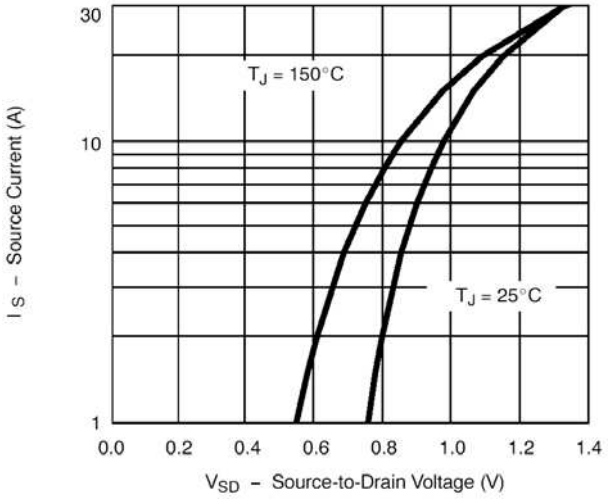


Figure 5.7: Source-Drain Diode Forward Voltage (P)

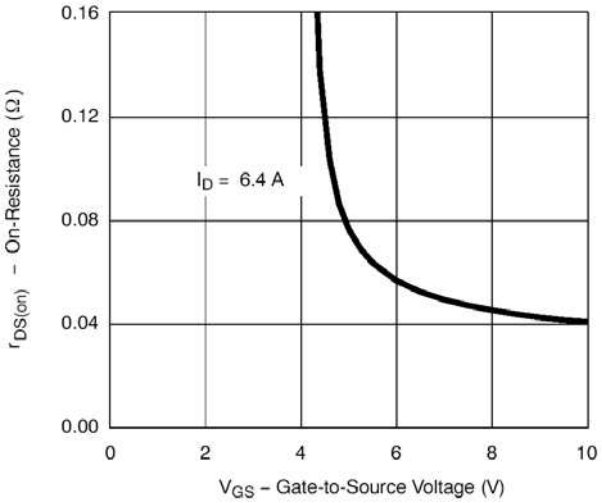


Figure 5.8: On-Resistance vs. Gate-to-Source Voltage (P)

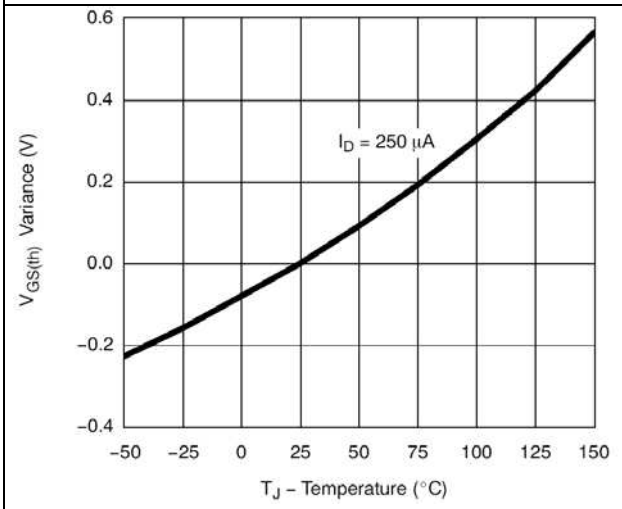


Figure 5.9: Threshold Voltage (P)

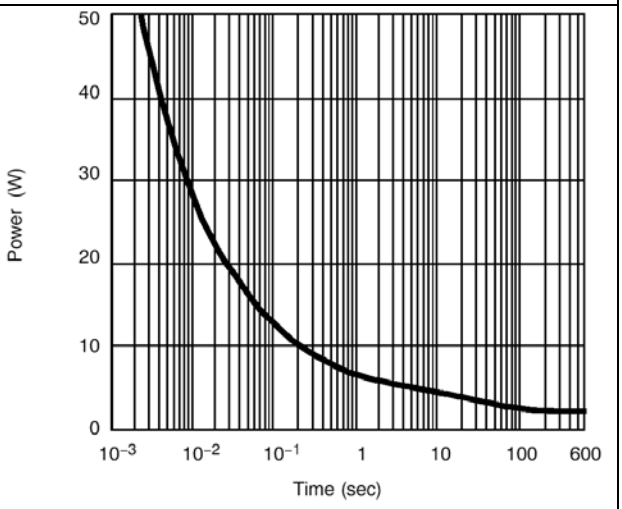


Figure 5.10: Single Pulse Power (P)

6 Application with TMC239 / TMC249

6.1 Example Wiring

Example wiring with four TMC34NP-PSO and a TMC239. Sense resistors shown are selected for 3.09A peak current (2.2A RMS). The Schottky diodes are ZHCS1000 or MSS1P3 types. (Power supply filter capacitors not shown.)

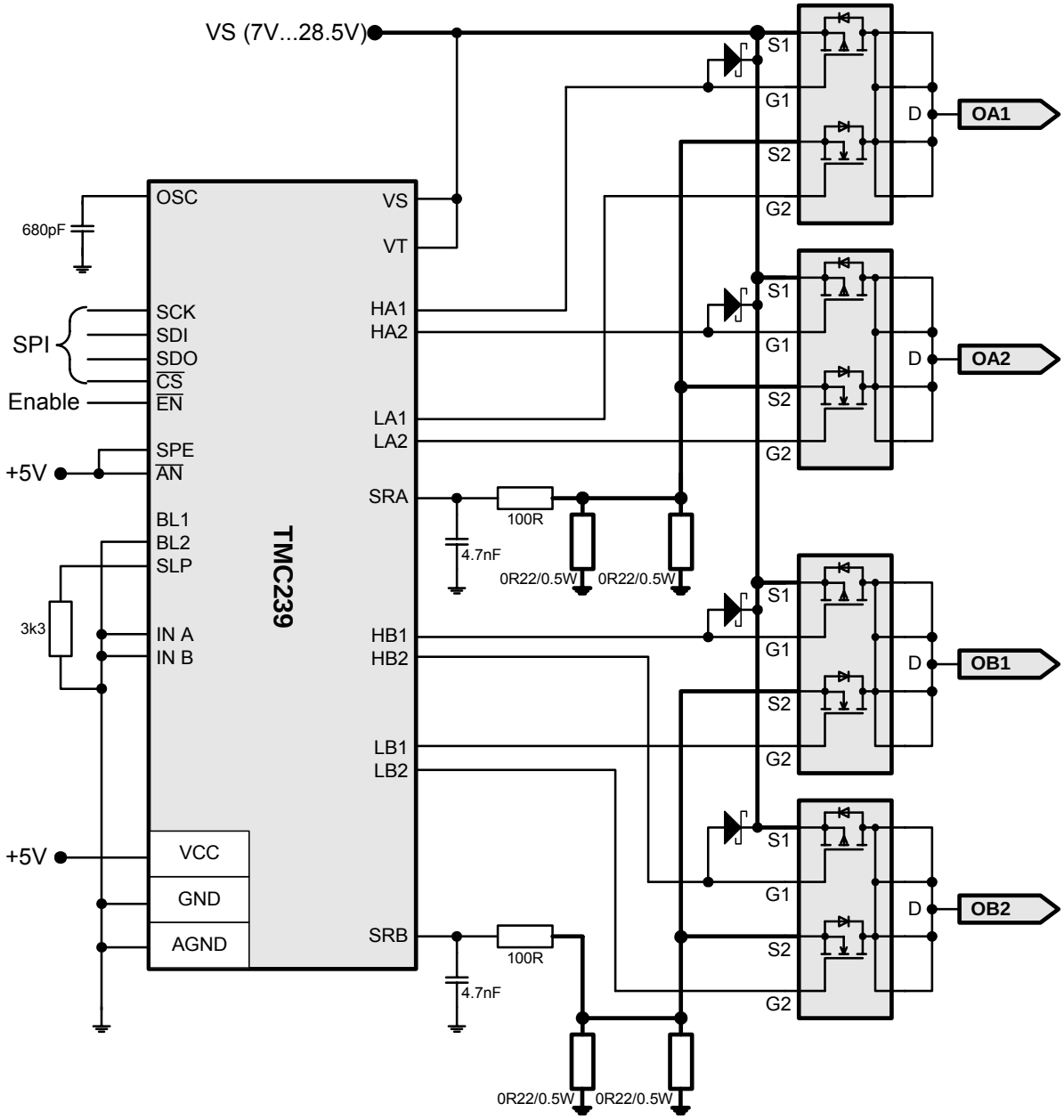


Figure 6.1: Example wiring with a TMC239

6.2 Example Layout

Table 6.1 shows an example layout for four TMC34NP-PSO with a TMC249A-LA driver chip. Original size of this layout on a PCB is about 29x25mm, see Figure 6.2. Current capability with is 4A peak (2.8A RMS).

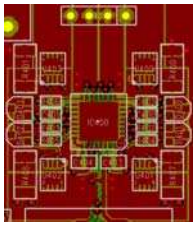


Figure 6.2: Example Layout in original size on PCB

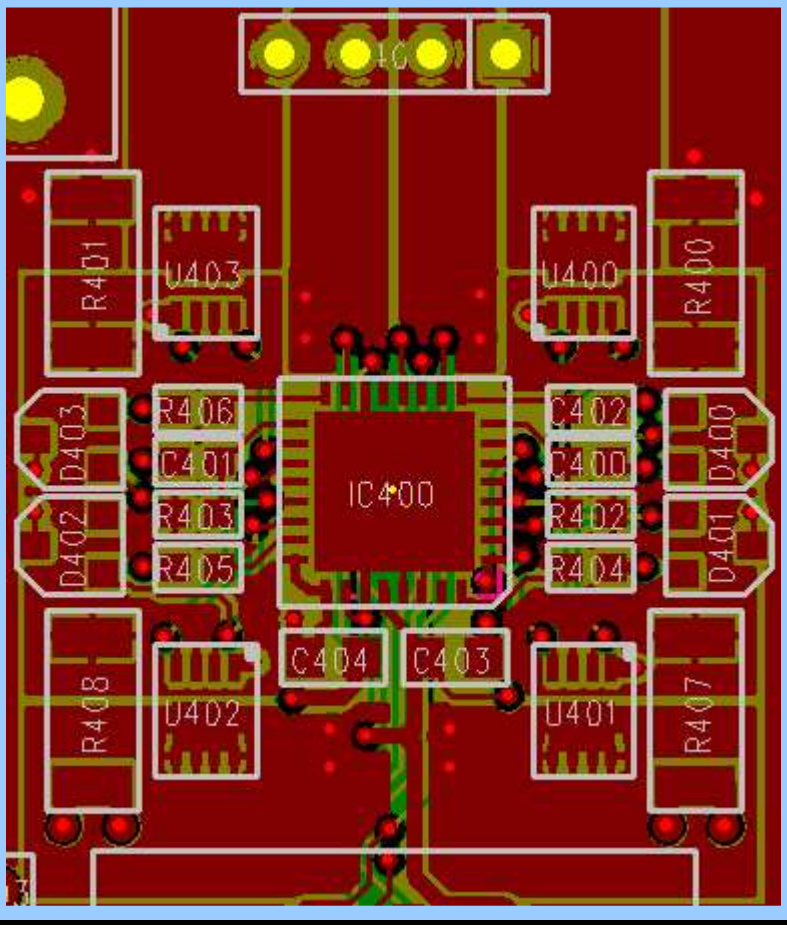
Layout	Name	Value/Description
	IC400	TMC249A-LA
	U400	TMC34NP-PSO
	U401	
	U402	
	U403	
	R400	2* 0R82/1W (1206) or 4* 0R15/0.5W
	R401	
	R402	
	R403	
	R402	100R/1% (0603)
	R403	
	R404	3k30/1% (RSLP)
	R405	0R (BL2 input)
	C400	4.7nF/50V (0603)
	C401	
	C402	680pF/50V (0603)
	C403	100nF/50V (0805)
	C404	
	R406	Spare (BL1 input)
	D400	ZHCS1000
	D401	
	D402	
	D403	

Table 6.1: Example Layout

Please refer to the evaluation board manual / website for more details.

7 Package Outline / Dimensions

7501	Base part id number
LL	Lot code
T	Assembly factory code
Y	Year code
W	Week code
F	Wafer fab code
•	Pin 1 indicator
	ESD symbol

Table 7.1: Package label

PowerPAK 1212 Package Outline (3.3mm x 3.3mm)

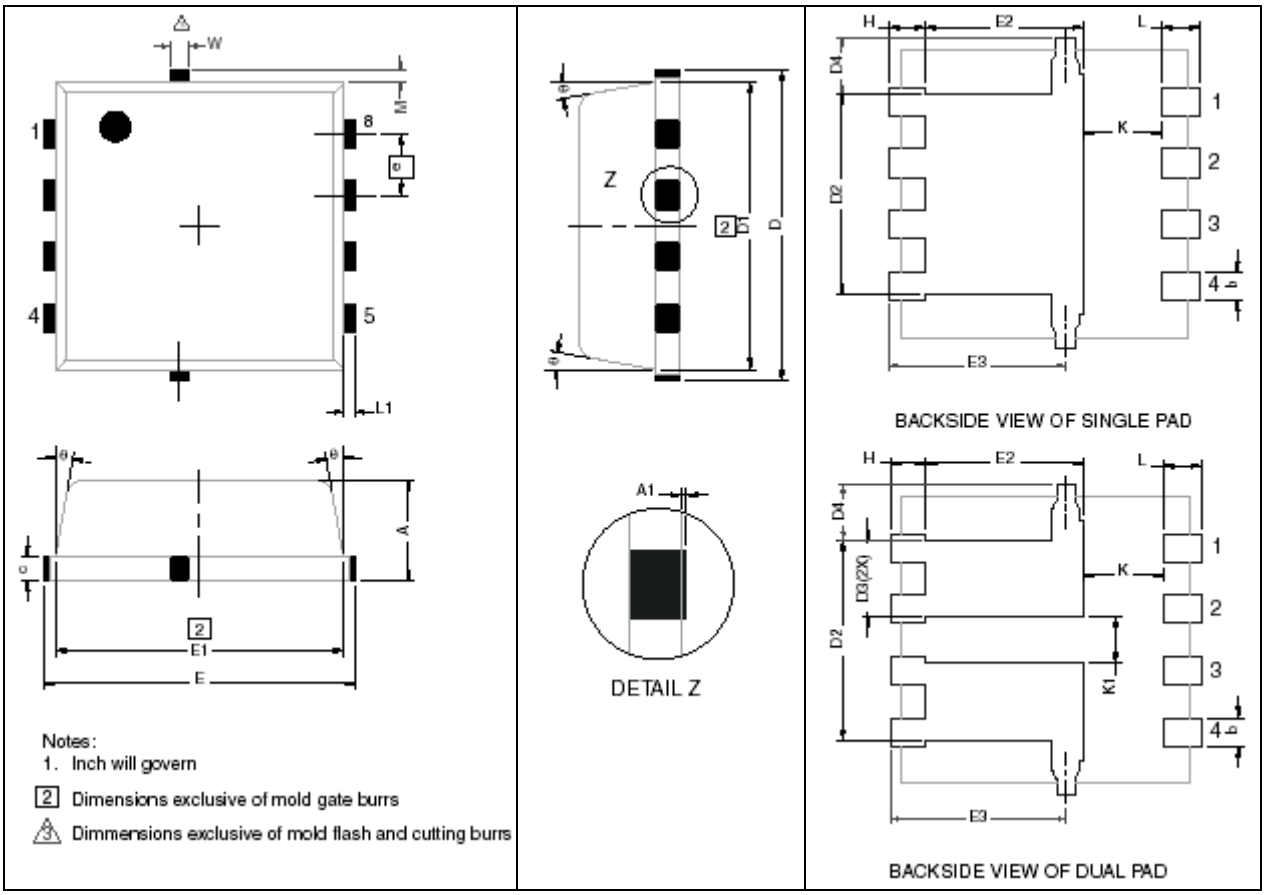


Figure 7.1: Package Outline

DIM	Millimeters			DIM	Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.97	1.04	1.12	E2	1.47	1.60	1.73
A1	0	-	0.05	E3 [a]	1.75	1.85	1.98
b	0.23	0.30	0.41	e [b]	0.65 BSC		
c	0.23	0.28	0.33	K	0.64	-	-
D	3.20	3.30	3.40	K1	0.35	-	-
D1	2.95	3.05	3.15	H	0.30	0.41	0.51
D2	1.98	2.11	2.24	L	0.30	0.43	0.56
D3	0.48	-	0.89	L1	0.06	0.13	0.20
D4 [a]	-	-	0.71	Θ	0°	-	12°
E	3.20	3.30	3.40	W [a]	0.15	0.25	0.36
E1	2.95	3.05	3.15	M [a]	-	-	0.23

Table 7.2: Package Dimensions in Millimeters

[a] Dimensions exclusive of mold flash and cutting burrs
[b] Dimensions exclusive of mold gate burrs

PowerPAK 1212 Package Outline (0.13inch x 0.13 inch)

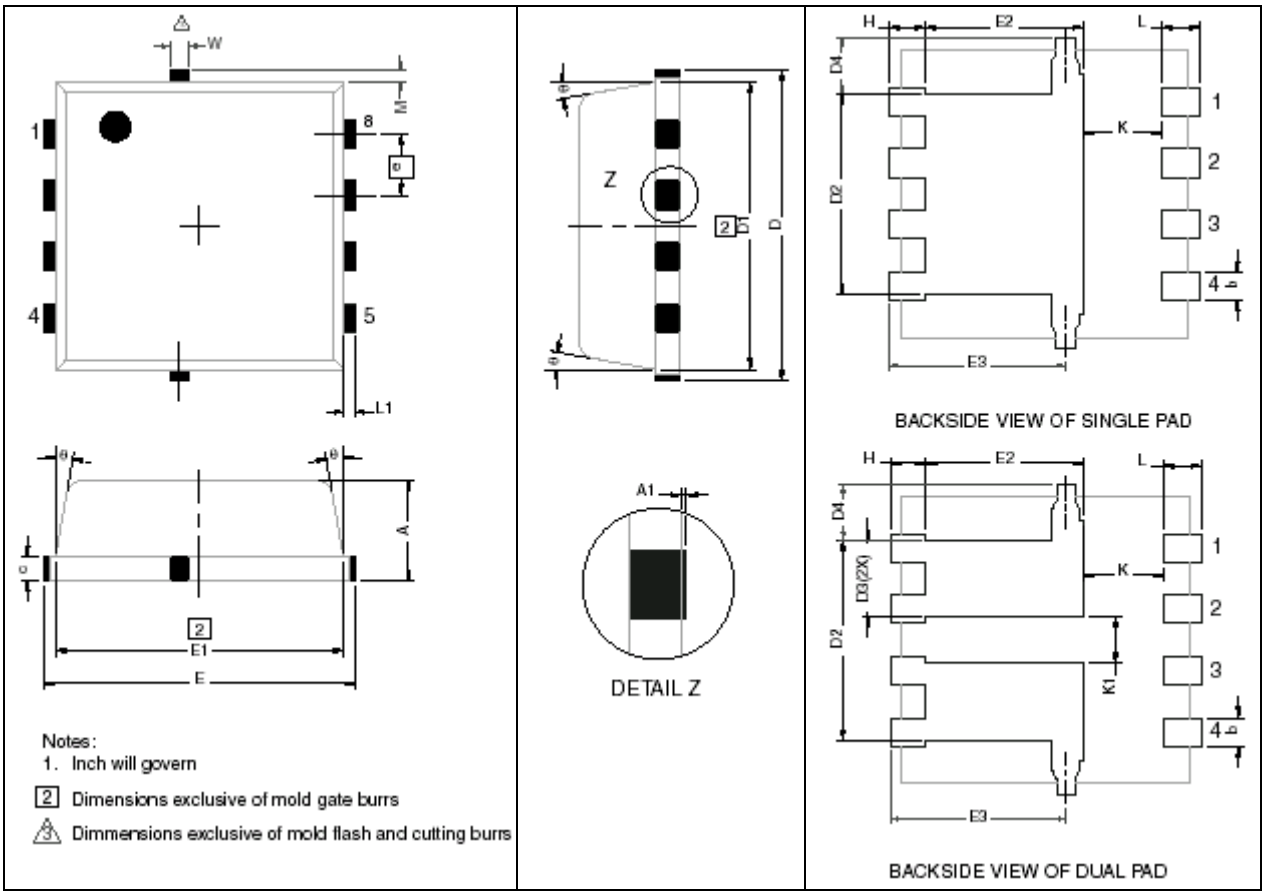


Figure 7.2: Package Outline

DIM	Inches			DIM	Inches		
	Min	Nom	Max		Min	Nom	Max
A	0.038	0.041	0.044	E2	0.058	0.063	0.068
A1	0	-	0.002	E3 [a]	0.069	0.073	0.078
b	0.009	0.012	0.016	e [b]	0.026 BSC		
c	0.009	0.011	0.013	K	0.025	-	-
D	0.126	0.130	0.134	K1	0.014	-	-
D1	0.116	0.120	0.124	H	0.012	0.016	0.020
D2	0.078	0.083	0.088	L	0.012	0.017	0.022
D3	0.019	-	0.035	L1	0.002	0.005	0.008
D4 [a]	-	-	0.028	Θ	0°	-	12°
E	0.126	0.130	0.134	W [a]	0.006	0.010	0.014
E1	0.116	0.120	0.124	M [a]	-	-	0.009

Table 7.3: Package Dimensions in Inches

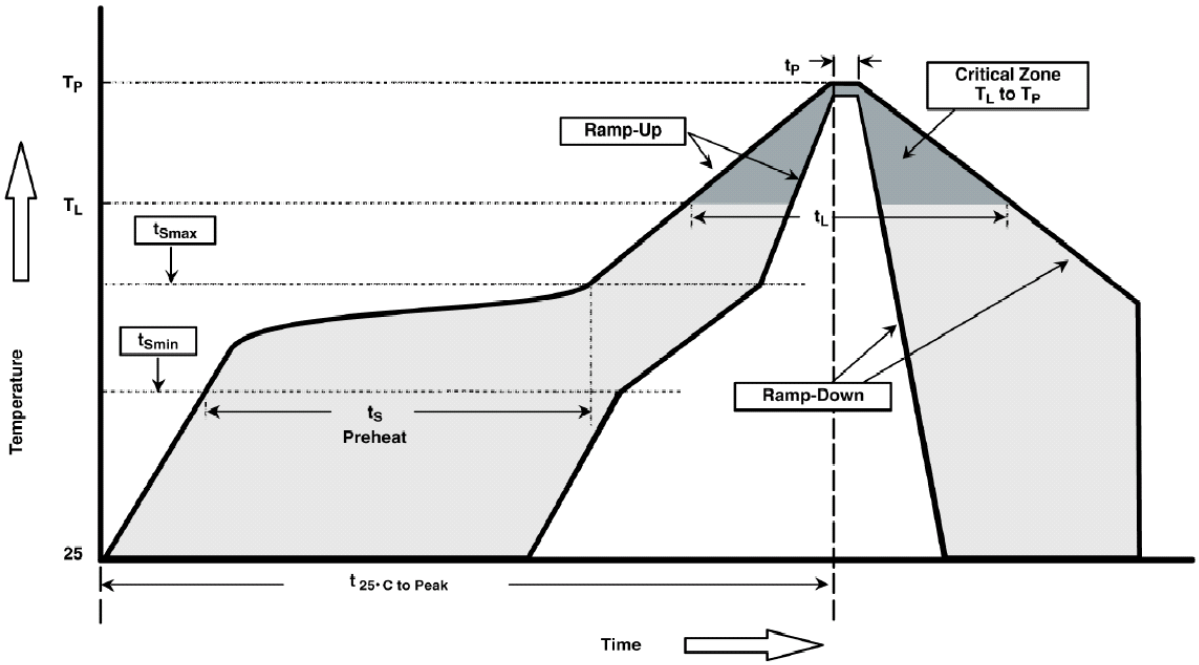
[a] Dimensions exclusive of mold flash and cutting burrs
[b] Dimensions exclusive of mold gate burrs

8 Solder profile

CLASSIFICATION REFLOW PROFILES (IPC/JEDEC J-STD-020C)			
Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly
	Large Body	Small Body	All Packages
Reflow Conditions	Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm³	Pkg. Thickness < 2.5 mm and Pkg. Volume < 350 mm³	
Average ramp-up rate (T_L to T_P)	3 °C/second max.		3 °C/second max.
Preheat • Temperature Min. (T_{Smin}) • Temperature Max. (T_{Smax}) • Time (min to max) (t_S)	100 °C 150 °C 60-120 seconds		150 °C 200 °C 60-180 seconds
Time maintained above: • Temperature (T_L) • Time (t_L)	183 °C 60-150 seconds		217 °C 60-150 seconds
Peak Temperature (T_P)	225 +0/-5 °C	240 +0/-5 °C	260 +0/-5 °C
Time within 5 °C of actual Peak Temperature (t_P)	10-30 seconds		20-40 seconds
Ramp-down Rate	6 °C/second max.		6 °C/second max.
Time 25 °C to Peak Temperature ($t_{25\ °C\ to\ Peak}$)	6 minutes max.		8 minutes max.

NOTE: All temperatures refer to topside of the package, measured on the package body surface.

Table 8.1: Soldering profile



Definitions of Classification Reflow Profiles as Given in the above Table

Figure 8.1: Soldering profile

9 Revision History

9.1 Documentation Revision

Version	Comment	Author	Description
1.00	26-Jul-2007	HC	Initial Version
1.01	15-Aug-2007	HC	Added note that ambient temp is 25°C unless otherwise noted and soldering profile

Table 9.1: Documentation Revisions

10 References

[TMC239] Microstep driver manual (see http://www.trinamic.com)
[TMC249] Microstep driver manual, with StallGuard (see http://www.trinamic.com)