

AON2801

Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

The AON2801/L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

AON2801 and AON2801L are electrically identical.

-RoHS Compliant

-Halogen Free*

Features

V_{DS} (V) = -20V

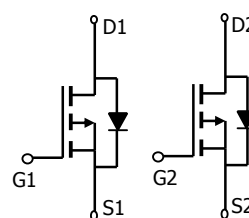
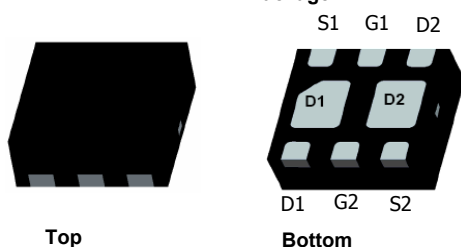
I_D = -3A (V_{GS} = -4.5V)

$R_{DS(ON)}$ < 120m Ω (V_{GS} = -4.5V)

$R_{DS(ON)}$ < 160m Ω (V_{GS} = -2.5V)

$R_{DS(ON)}$ < 200m Ω (V_{GS} = -1.8V)

DFN 2x2 Package



Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ^A	I_D	-3	A
$T_A = 25^\circ\text{C}$		-2.3	
Pulsed Drain Current ^C	I_{DM}	-15	
Power Dissipation ^A	P_{DSM}	1.5	W
		0.95	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	35	45	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		65	85	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^B	$R_{\theta JA}$	120	155	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^B		175	235	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-20\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 8\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-0.3	-0.55	-1	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}$, $V_{DS}=-5\text{V}$	-15			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-4.5\text{V}$, $I_D=-3\text{A}$ $T_J=125^{\circ}\text{C}$		100 135	120 170	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}$, $I_D=-2.6\text{A}$		128	160	$\text{m}\Omega$
		$V_{GS}=-1.8\text{V}$, $I_D=-1.5\text{A}$		160	200	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-3\text{A}$		6		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.76		V
I_S	Maximum Body-Diode Continuous Current				-1	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-10\text{V}$, $f=1\text{MHz}$		540	700	pF
C_{oss}	Output Capacitance			90		pF
C_{rss}	Reverse Transfer Capacitance			63		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		9.5		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $I_D=-3\text{A}$		5	6.5	nC
Q_{gs}	Gate Source Charge			1.2		nC
Q_{gd}	Gate Drain Charge			1		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $R_L=1.5\Omega$, $R_{GEN}=3\Omega$		5		ns
t_r	Turn-On Rise Time			40		ns
$t_{D(off)}$	Turn-Off DelayTime			28.5		ns
t_f	Turn-Off Fall Time			46		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-3\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		21	28	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-3\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		9.1		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.

B: The value of $R_{\theta JA}$ is measured with the device mounted on a minimum pad board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 7111 (Oct 15 2007).

Rev 2: Sep 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

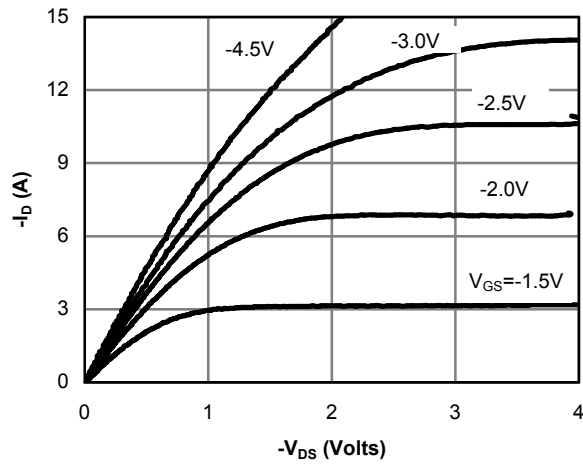


Figure 1: On-Region Characteristics

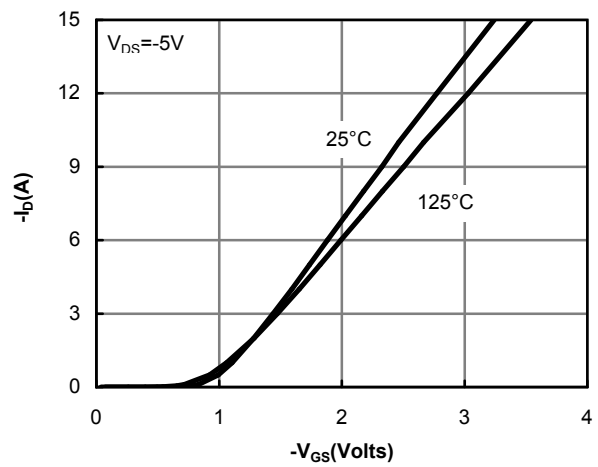


Figure 2: Transfer Characteristics

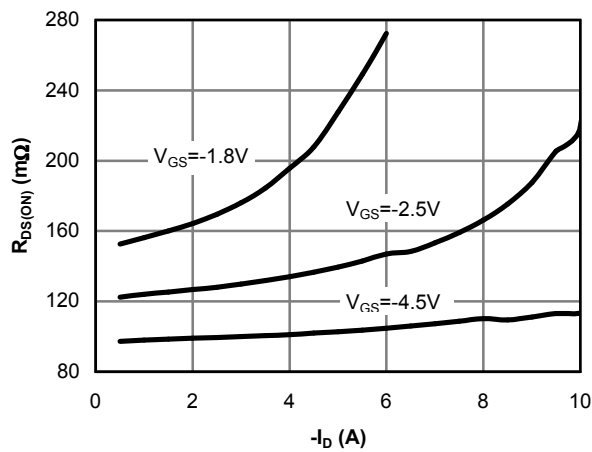


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

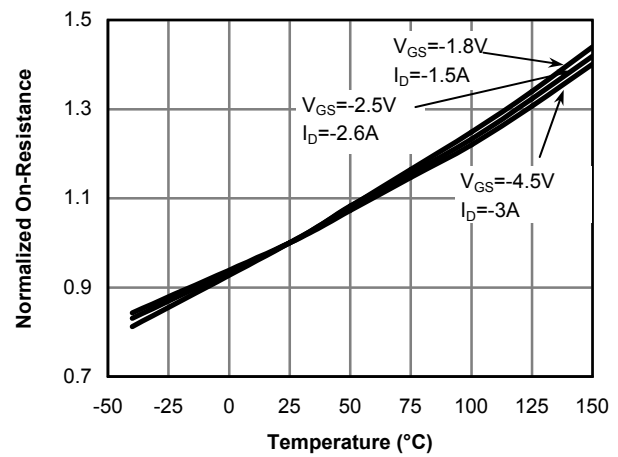


Figure 4: On-Resistance vs. Junction Temperature (Note E)

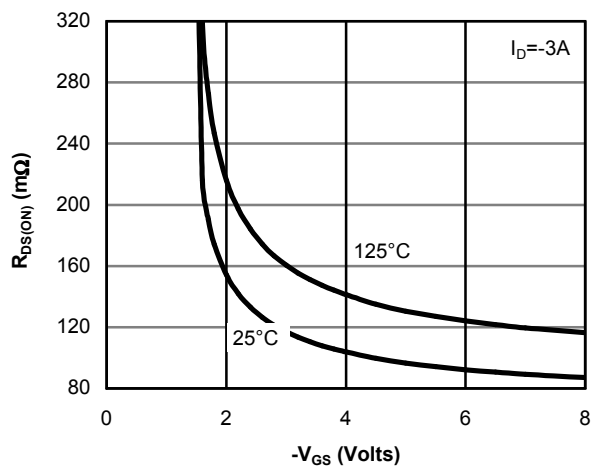


Figure 5: On-Resistance vs. Gate-Source Voltage

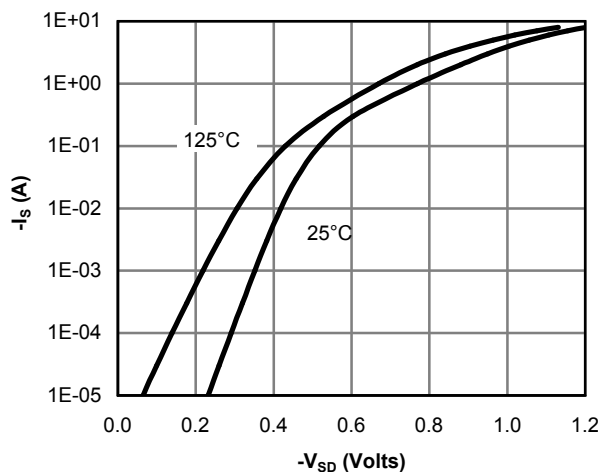


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

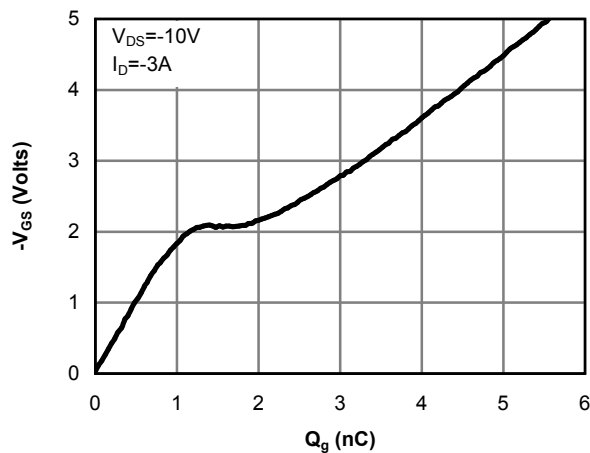


Figure 7: Gate-Charge Characteristics

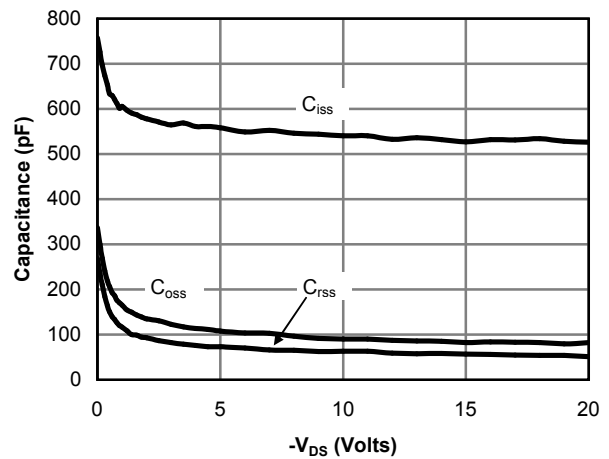


Figure 8: Capacitance Characteristics

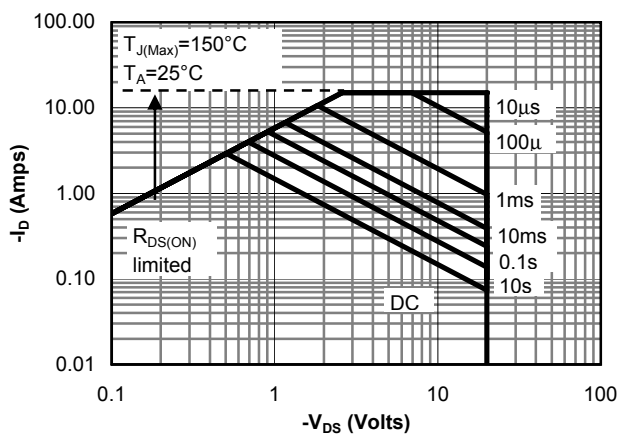


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

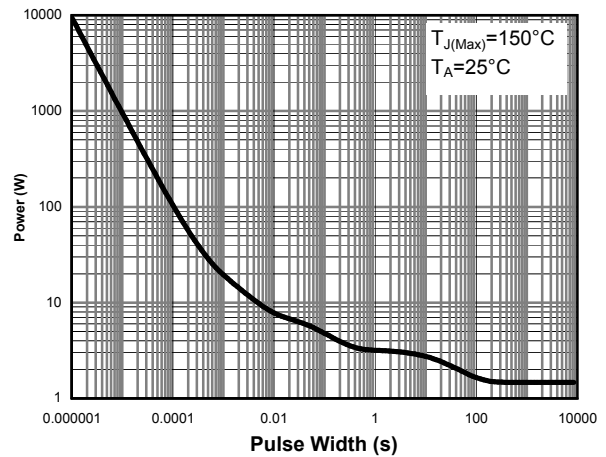


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

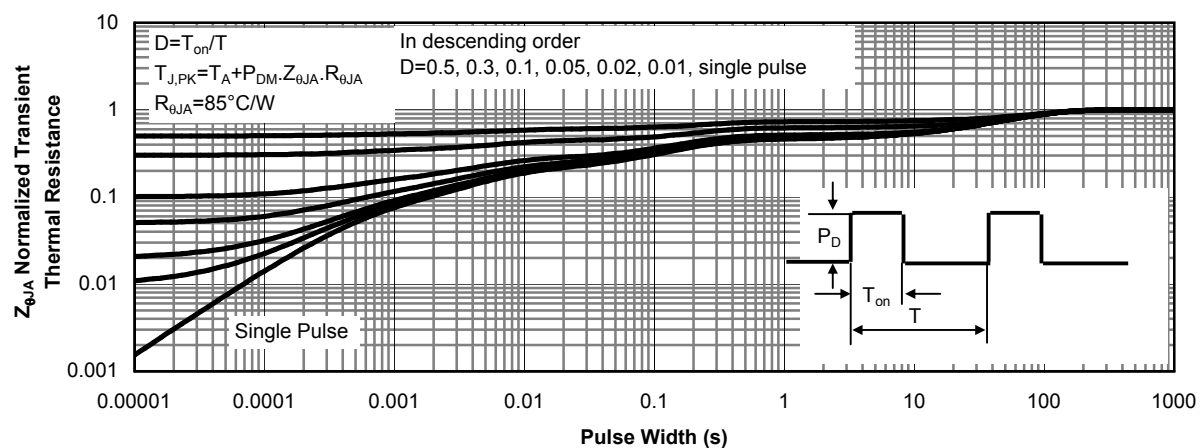
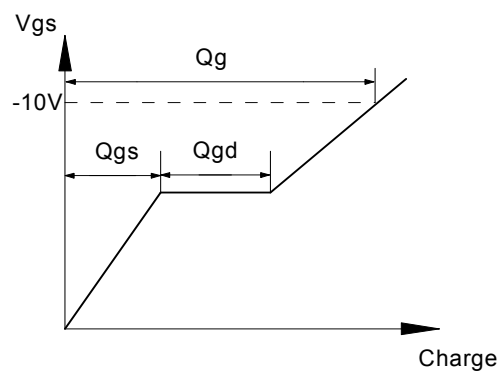
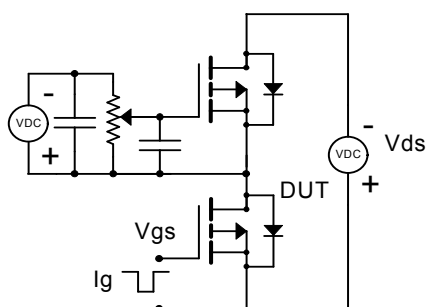
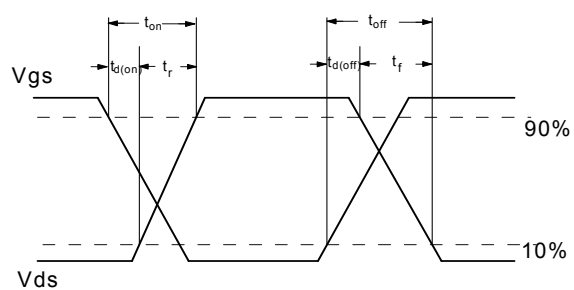
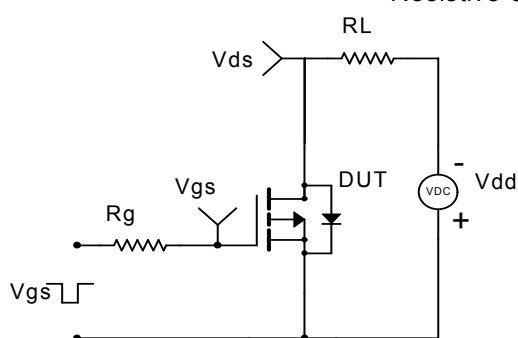


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

