

General Description

The AO4402 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

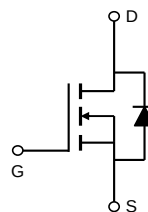
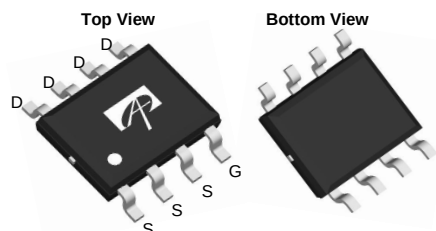
Product Summary

V_{DS}	20V
I_D (at $V_{GS}=4.5V$)	20A
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 5.5m Ω
$R_{DS(ON)}$ (at $V_{GS}=2.5V$)	< 7m Ω

100% UIS Tested
 100% R_g Tested



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	20	A
		16	
Pulsed Drain Current ^C	I_{DM}	140	
Avalanche Current ^C	I_{AS}, I_{AR}	57	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	162	mJ
Power Dissipation ^B	P_D	3.1	W
		2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	31	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}		59	75	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

Electrical Characteristics (T_j=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V T _j =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.5	1	1.6	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	140			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =20A T _j =125°C		4.6 5.8	5.5 7	mΩ
		V _{GS} =2.5V, I _D =18A		5.5	7	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		105		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.6	1	V
I _S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V, f=1MHz	3080	3860	4630	pF
C _{oss}	Output Capacitance		520	740	960	pF
C _{rss}	Reverse Transfer Capacitance		350	580	810	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.6	1.4	2.1	Ω
SWITCHING PARAMETERS						
Q _g (4.5V)	Total Gate Charge	V _{GS} =10V, V _{DS} =10V, I _D =20A	28	36	43	nC
Q _{gs}	Gate Source Charge		7	9	11	nC
Q _{gd}	Gate Drain Charge		7	12	17	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =10V, R _L =0.5Ω, R _{GEN} =3Ω		7		ns
t _r	Turn-On Rise Time			8		ns
t _{D(off)}	Turn-Off DelayTime			70		ns
t _f	Turn-Off Fall Time			18		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs	13	17	20	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs	29	36	43	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C. Maximum avalanche current limited by tester capability.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

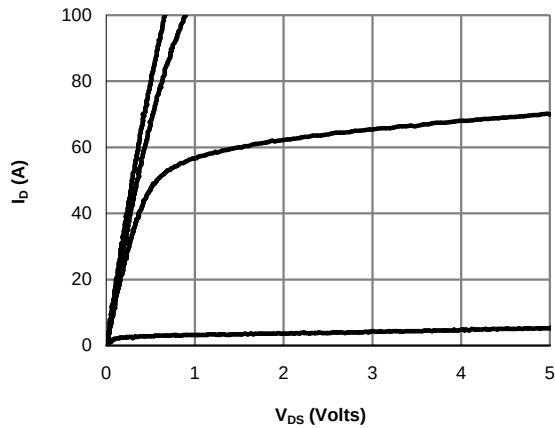


Fig 1: On-Region Characteristics (Note E)

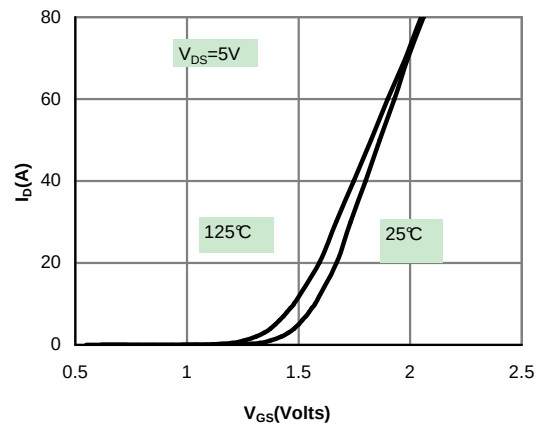


Figure 2: Transfer Characteristics (Note E)

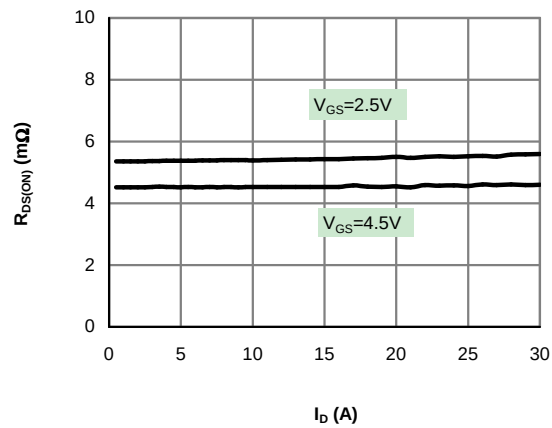


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

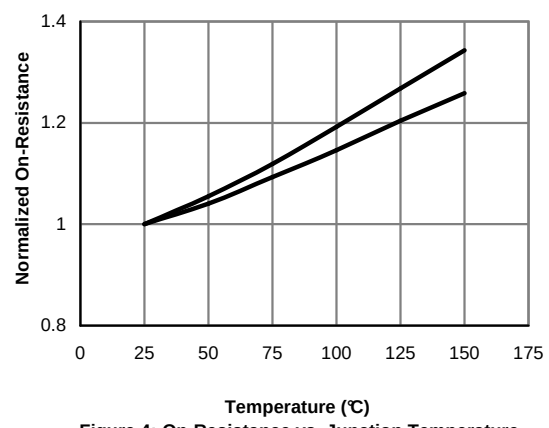


Figure 4: On-Resistance vs. Junction Temperature (Note E)

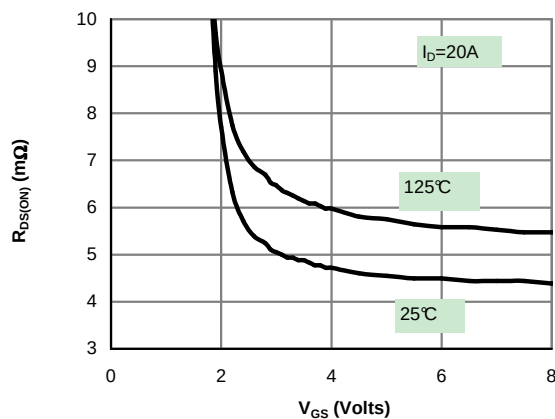


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

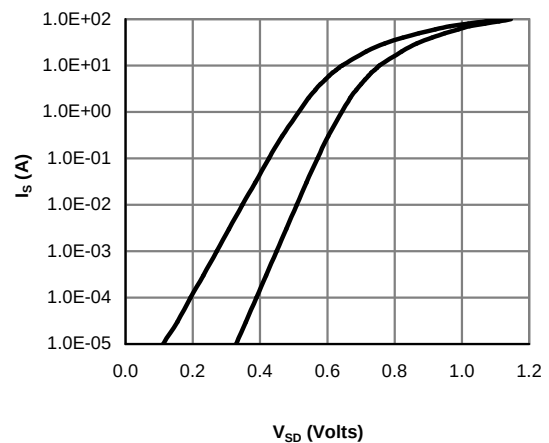


Figure 6: Body-Diode Characteristics (Note E)

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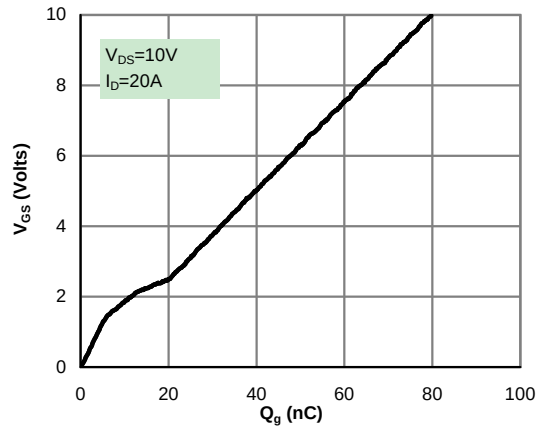


Figure 7: Gate-Charge Characteristics

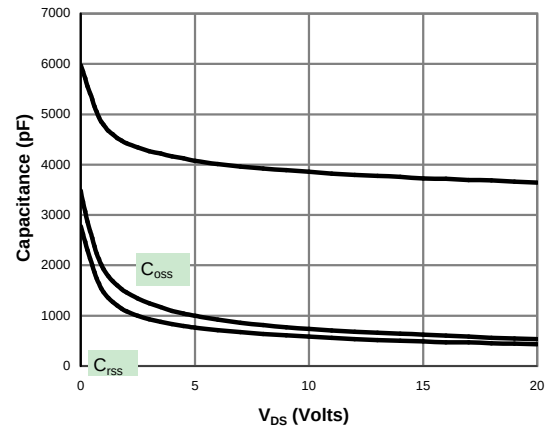


Figure 8: Capacitance Characteristics

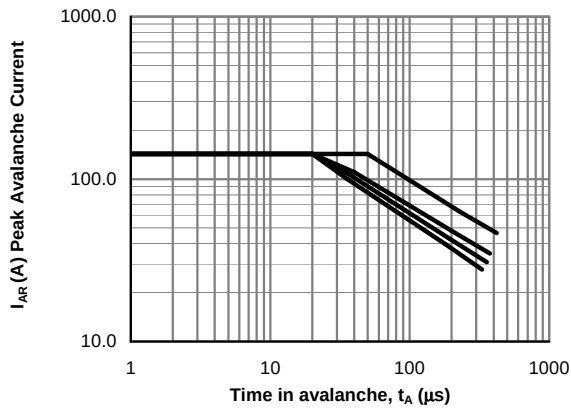


Figure 9: Single Pulse Avalanche capability (Note C)

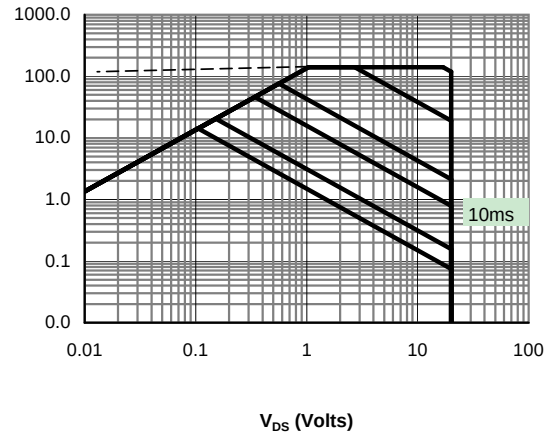
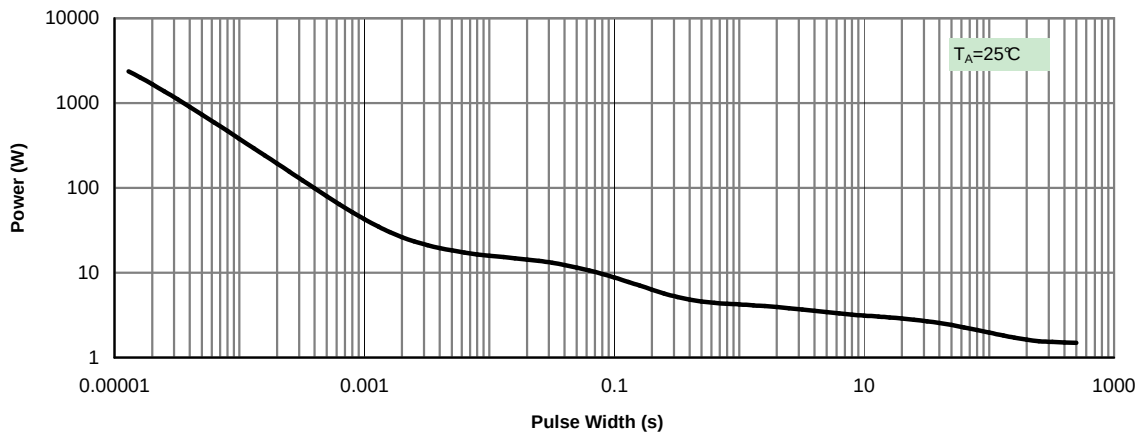


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

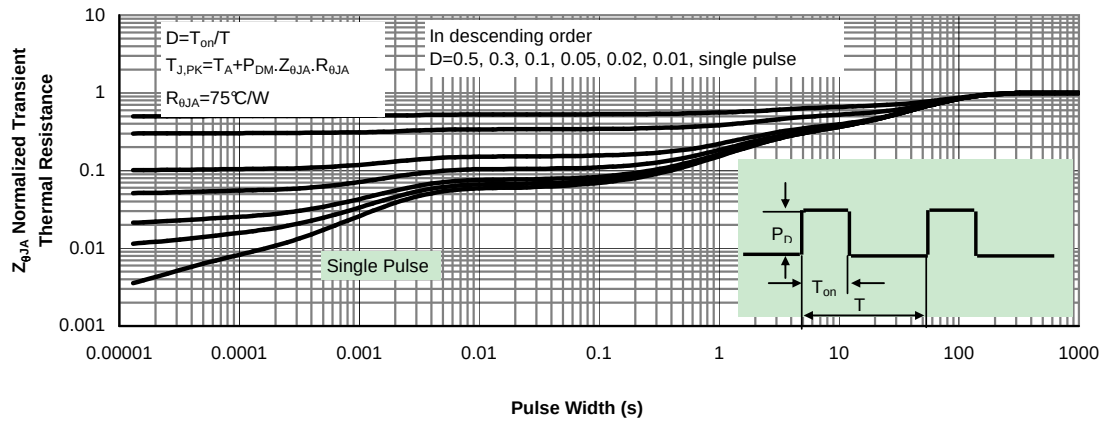
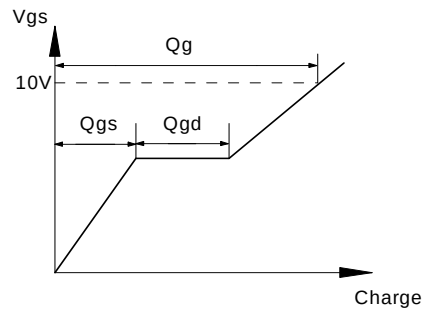
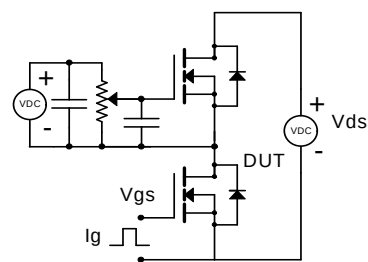
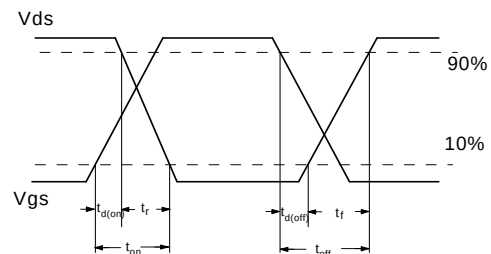
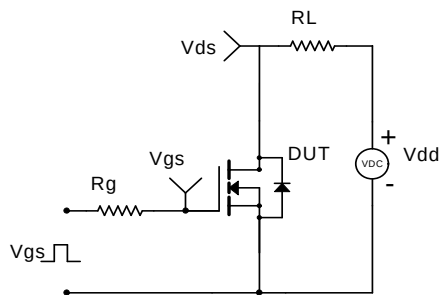


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

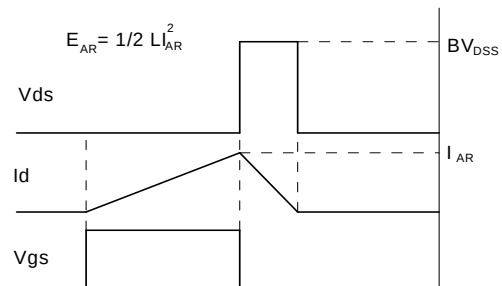
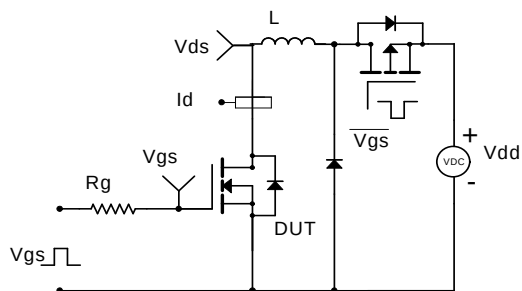
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

