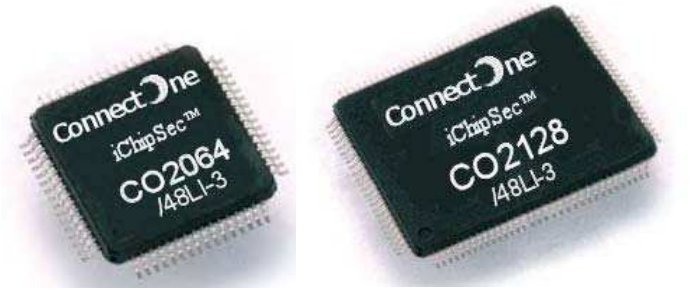
iChip™

iChip™ CO2064/CO2128/CO2144



Data Sheet

Ver. 1.30

Connect One Ltd.
20 Atir Yeda Street
Kfar Saba 44643, Israel
Tel: +972-9-766-0456
Fax: +972-9-766-0461
E-mail: sales@connectone.com
http://www.connectone.com

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1 Introduction

General Description

iChip™ CO2064, CO2128 and CO2144 are full-featured programmable IP Communication Controller™ chips that act as coprocessors to offload security and IP connectivity tasks from any host processor. They are ideal for enabling devices to achieve secure, high-speed throughput and access to IP networks via 10/100BaseT LAN or 802.11b/g wireless LAN, and cellular or dial-up modems. Typically only one man-month is needed for hardware engineering and adding IP connectivity commands to the host application.

While the CO2128/CO2144 include a complete set of features, the CO2064 uses an open software architecture that enables users to select and program different firmware flavors, each providing a unique subset of Internet protocols and features.

The CO2128/CO2144 firmware supports up to 10 simultaneous active TCP/UDP sockets and two listening sockets; HTTP, SMTP, MIME, POP3, FTP and TELNET clients; a web server with two websites: one for configuring the CO2128/CO2144 and one for the application; and serial-to-IP bridging.

The CO2064 comes in two firmware flavors:

- Flavor ***A*** offers 10 active TCP/UDP sockets and two listening sockets; sending ASCII e-mails; sending and retrieving data from an FTP server, and serial-to-IP bridging in SerialNet™ mode.
- Flavor ***B*** supports one secure TCP/UDP socket plus 9 non-secure sockets.

Security features in the CO2064 include the hardware implementation of a random number generator, SHA-1 secure hash accelerator, AES-128/256 encryption accelerator, 3DES, SSL3/TLS1, RSA, RC-4 and MD-5. The CO2128 includes, in addition to the above, WEP, WPA, and WPA2 encryption for WiFi.

CO2064 loads its firmware and Internet configuration parameters either from an external SPI flash memory, or accepts it from the host via one of the supported interfaces. Firmware can be updated locally via RS232.

CO2128/CO2144 load their firmware from an external EBI flash memory. Firmware can be remotely updated via sockets, FTP or HTTP.

All three iChips include a 32-bit ARM7TDMI RISC processor and 256KB of embedded high-speed SRAM. Basic peripherals for all models include USB v. 2.0 full-speed host and device port; 10/100BaseT Ethernet MAC with MII/RMII, USART and SPI interfaces.

Both CO2064 and CO2128/CO2144 feature Sleep mode for energy savings. The iChips come in a 64-pin (CO2064), 128-pin (CO2128) or 144-pin (CO2144) LQFP RoHS-compliant package.

Key Features

- Complete Internet protocol stack
- RSA, AES-128/256, 3DES, RC-4, SHA-1, MD-5 and SSL3/TLS1 encryption
- 10/100BaseT Ethernet MAC
- USB v2.0 full-speed host and device
- USART, SPI interfaces

Application Program Interface

Connect One's AT+i protocol eliminates the need for Internet programming and minimizes changes to the host application, while the SerialNET serial-to-IP bridging mode eliminates the need for any change to the host application. AT+i commands are intercepted by iChip, which puts the host device into Internet mode.

2 Features

2.1 CO2064 Features

Key Features

- Acts as a security gap between the application and the network
- Two firmware flavors for greater flexibility
- Up to 10 simultaneous TCP/UDP sockets and two listening sockets
- One secure SSL3/TLS1 socket
- Supports multiple Certificate Authorities and both client-side and server-side authentication
- Includes a true random number generator in hardware
- Sending plain-text email
- SerialNet mode for serial-to-IP bridging
- FTP client
- DHCP client
- Locally updateable firmware
- Retrieval of time data from a Network Time Server
- Software and hardware flow control

Performance Specifications

- Host Data Rate: Up to 3 Mbps in serial mode
- Serial Data Format (AT+i mode): Async. character; binary; 8 data bits; no parity; 1 stop bit
- Serial Data Format (SerialNET mode): Async. character; binary; 7 or 8 data bits; odd, even, or no parity; 1 stop bit
- Flow Control: hardware (DTR, RTS, CTS, DCD) and software flow control

Internet Protocols

- ARP, ICMP, DHCP, IP, UDP acceleration in hardware, TCP, DNS, NTP, SSL3/TLS1, SMTP, FTP

Hardware Description

- Package: 64-pin LQFP, RoHS-compliant
- Dimensions: 10x10x1.4mm, 0.5mm pitch
- Core CPU: 32-bit RISC ARM7TDMI, 0.13 micron, low-leakage
- I/O Operating Range: 3.3V+/-10%; Core Operating Range: 1.2V+/-10%
- Operating Frequency: Up to 48MHz
- Operating Humidity: 90% max. (non-condensing)

- Operating Temperature Range: -40° to 85°C (-40° to 185°F)
- Power Consumption with external VDD Core @ 1.2V: 200mW (typical)
- Sleep mode current: <2mA
- Interfaces: USART, SPI

Note: For a detailed description of all available features, see the *AT+i Programmer's Manual*.

2.2 CO2128/CO2144 Features

Key Features

- Acts as a security gap between the host application and the network
- Provides dialup, cellular, LAN and WiFi connectivity
- Non-volatile, on-chip operational parameter database
- Up to 10 simultaneous TCP/UDP sockets and two listening sockets
- One secure SSL3/TLS1 socket
- Supports multiple Certificate Authorities and both client-side and server-side authentication
- Routing of IP packets between dialup/cellular and LAN/WiFi platforms using NAPT
- Supports infrasturcture and ad-hoc wireless LAN networks
- Enables roaming among Access Points sharing the same SSID
- Provides WEP, WPA and WPA2 wireless LAN security
- Includes a true hardware random number generator
- Triple DES, AES and SHA implemented in hardware
- Includes 10/100BaseT Ethernet MAC
- Sending and receiving textual email and binary email with MIME attachments
- HTTP client
- HTTP web server with two on-chip websites: configuration site and application site
- SerialNet mode for serial-to-IP bridging (port server mode)
- FTP and Telnet clients
- Secure FTP client (over SSL3)
- DHCP client and server
- RAS server
- Locally updateable firmware
- Remote configuration and firmware update over the Internet
- Retrieval of time data from a Network Time Server

Performance Specifications

- Host Data Rate: Up to 3 Mbps in serial mode
- Serial Data Format (AT+i mode): Asynchronous character; binary; 8 data bits; no parity; 1 stop bit
- Serial Data Format (SerialNET mode): Asynchronous character; binary; 7 or 8 data bits; odd, even, or no parity; 1 stop bit
- Flow Control: Hardware (RTSH, CTSH, DCH) and software flow control

Internet Protocols

- ARP, ICMP, IP, UDP, TCP, DHCP, DNS, NTP, SMTP, POP3, MIME, HTTP, FTP, Telnet
- Security protocols: SSL3/TLS1, HTTPS, FTPS, RSA, AES-128/256, 3DES, RC-4, SHA-1, MD-5, WEP, WPA and WPA2

Hardware Description

- CO2128 Size: 14.0 x 20.0 x 1.4 mm, 0.5mm pitch
- CO2064 Size: 10.0 x 10.0 x 1.4 mm, 0.5mm pitch
- CO2144 Size: 10.0 x 10.0 x 1.4 mm, 0.8mm pitch
- Core CPU: 32-bit RISC ARM7TDMI, low-leakage, 0.13 micron, running at 48MHz
- Operating Voltage: +3.3V+/-10%
- Operating Humidity: 90% maximum (non-condensing)
- Operating Temperature Range: -40° to 85°C (-40° to 185°F)
- Power Consumption with External VDD Core: 200mW (typical),
  Sleep Mode current: <2mA
- Host Interface: USART, USB host and USB device
- RoHS-compliant; lead-free

Note: For a detailed description of all available features, see the *AT+i Programmer's Manual*.

3 Functional Block Diagram

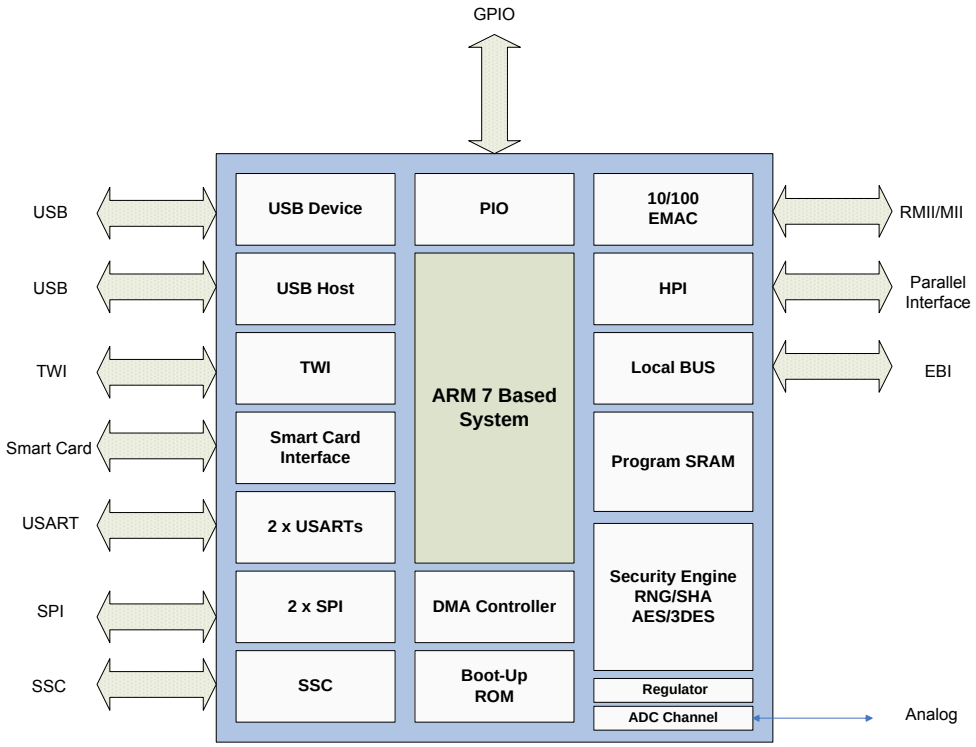


Figure 3-1: CO2128/CO2144 Block Diagram

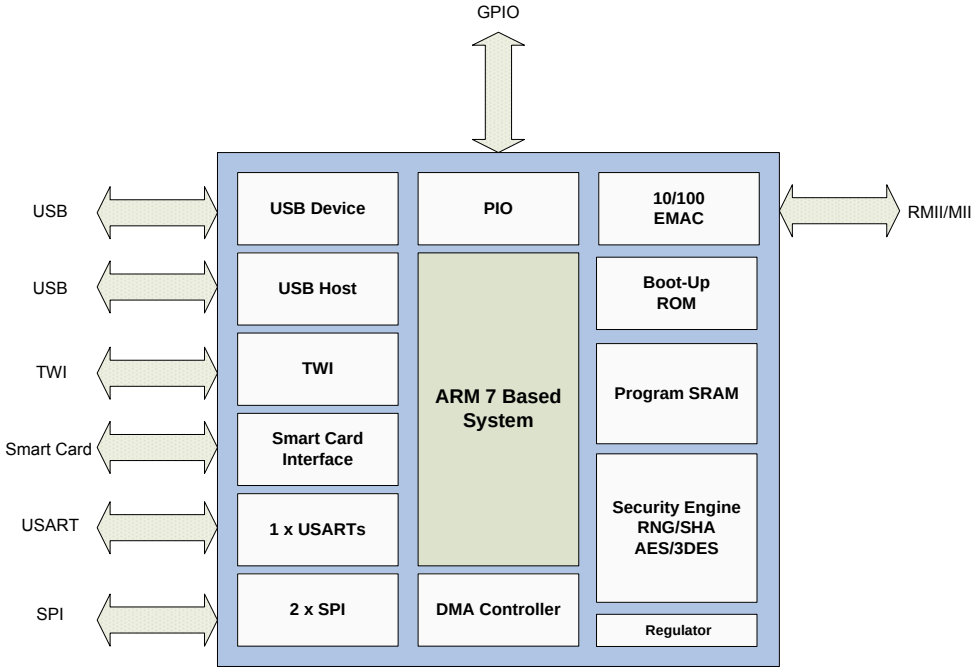


Figure 3-2: CO2064 Block Diagram

3.1 Interfaces Summary

Interface symbol	Description	Use for connection to
PIOA	General purpose IO pins group A [30:0]	General purpose IO lines
PIOB	General purpose IO pins group B [30:12] and [10:0]	General purpose IO lines
PIOC	General purpose IO pins group C [28:0]	General purpose IO lines
EBI	External bus interface	16 bit external memory (Flash, SRAM, etc)
MII	Media independent interface	10/100 BaseT Ethernet PHY component
RMII	Reduced media independent interface	10/100 BaseT Ethernet PHY component
HPI	Host port interface	8-bit parallel host processor
USB Host	USB v2.0 full speed device	12Mbps
USB Device	USB v2.0 full-speed host	12Mbps
USART0	Universal synchronous/asynchronous receiver transmitter	USART data terminal/data set, e.g. serial host processor
USART1	Universal asynchronous receiver transmitter	USART data terminal/data set
SPI0	Serial peripheral interface 0	
SPI1	Serial peripheral interface 1	
SC	Smart card reader interface	
TWI	Inter-integrated circuit	
ADC	Analog to digital converter	
SSC	Synchronous serial controller	
IRQ	Interrupt request	
TIMR	Timer interface	

Table 3-1: Summary of Interfaces

3.2 External Interface Multiplexing

Most general purpose IO ports of the device (PIOA, PIOB and PIOC) have been assigned multiple functions, selected under software control and external configuration pin setup. Up to two alternative functions and general purpose IO may be assigned to each external pin. The selection among the various choices is described in Figure 3-2.

3.2.1 CO2128/CO2144 Configuration Options

Eight different configuration options are possible by selecting the functions available per pin cluster. Figure 3-2 shows the pin cluster options.

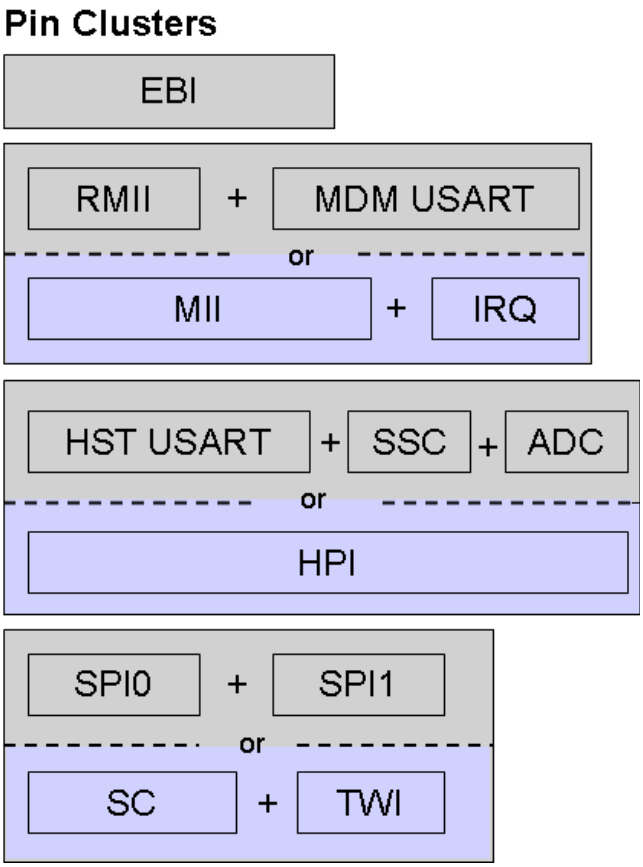


Figure 3-2: CO2128/CO2144 Configuration Options Block Diagram

Table 3-2 presents available chip configuration options for the CO2128/CO2144.

Conf. #	External Function Selection			
1	EBI	HPI	SC + TWI	MII (*)
2	EBI	HPI	SC + TWI	RMII, MDM USART
3	EBI	HPI	SPI0, SPI1	MII
4	EBI	HPI	SPI0, SPI1	RMII, MDM USART
5	EBI	HST USART, SSC, ADC	SC + TWI	MII
6	EBI	HST USART, SSC, ADC	SC + TWI	RMII, MDM USART
7	EBI	HST USART, SSC, ADC	SPI0, SPI1	MII
8	EBI	HST USART, SSC, ADC	SPI0, SPI1	RMII, MDM USART

Table 3-2: CO2128/CO2144 Configuration Options

* MII supported in Firmware 802 and above

3.2.2 CO2064 Configuration Options

Four different configuration options are possible by selecting the functions available per pin cluster. Figure 3-3 shows the pin cluster options.

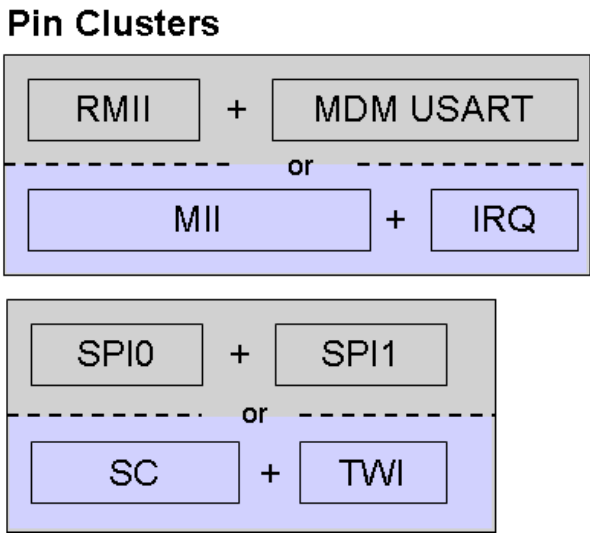


Figure 3-3: CO2064 Configuration Options Block Diagram

Table 3-3 presents available chip configuration options for the CO2064.

Conf. #	External Pin Function	
1	SC + TWI	MII(*)
2	SC + TWI	RMII, MDM USART
3	SPI0, SPI1	MII
4	SPI0, SPI1	RMII, MDM USART

Table 3-3: CO2064 Configuration Options

* MII supported in Firmware 802 and above

3.2.3 CO2064 and CO2128/CO2144 Pin Configuration Selection

On power-up, all IO ports (PIOA, PIOB, PIOC) assume general purpose input pins functionality whose state may be inspected or driven individually by software. Based on the application, the ports are reconfigured by software to assume the applicable functionality as part of the power-up system setup routine. The selection is determined by tying the following pins to either VDD (‘1’) or GND (‘0) via a pull-up or pull-down resistor, respectively, as detailed in Table 3-4.

Package	Pin Name	Pin Number	Functionality	Value	Effect
64+ 128/144	CONF1	PIOB[28]	EMDC	Low	Bypass internal ROM *
				High	Engage internal ROM
64 + 128/144	CONF2	PIOC[17]	SPI0_nCS / SC_RST	Low	SPI1 (slave)
				High	I2C
64+ 128/144	CONF3	PIOC[14]	SC_CLK / SPI0_MISO	High	SPI0 (master)
				Low	SC
64+ 128/144	CONF4	PIOB[15]	ETXER / USART1_TXD1	High	RMII, MDM USART
				Low	MII, IRQ *
128/144	CONF5	PIOC[12]	HPI_IBF / nDTR0	High	HPI
				Low	USART0, SSC, FIQ, ADC
64+ 128/144	CONF6	PIOB[29]	MII_EMDIO	Low	Enable load from LAN *
				High	Disable load from LAN
64+ 128/144	CONF7	PIOC[24]	iChip_ERR	Low	UHP Enabled
				High	UHP Disabled (default)

Table 3-4: Pin Configuration Setup

(*) MII supported in Firmware 802 and above

3.2.4 Pin-out for the 144-pin Package

For a detailed description of pin assignments, see the Pin Description Table.

Bottom View

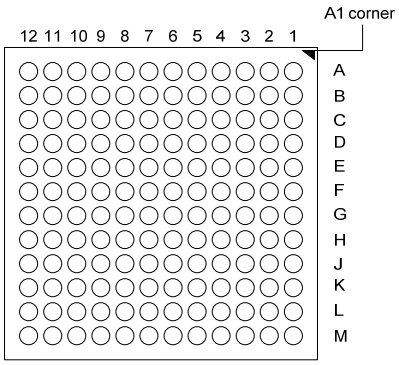


Figure 3-4: Pin-out for the 144-pin Package

3.2.5 Pin-out for the 128-pin Package

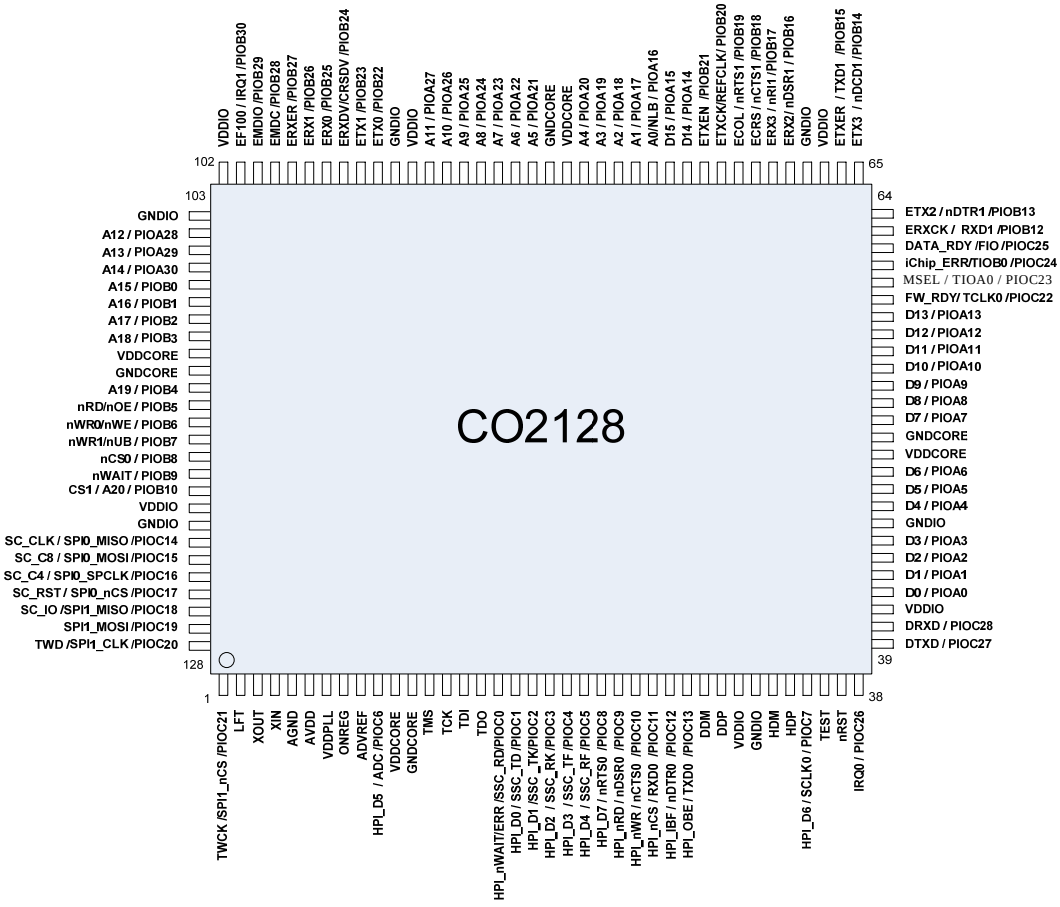


Figure 3-5: Pin-out for the 128-pin Package

3.2.6 Pin-out for the 64-pin Package

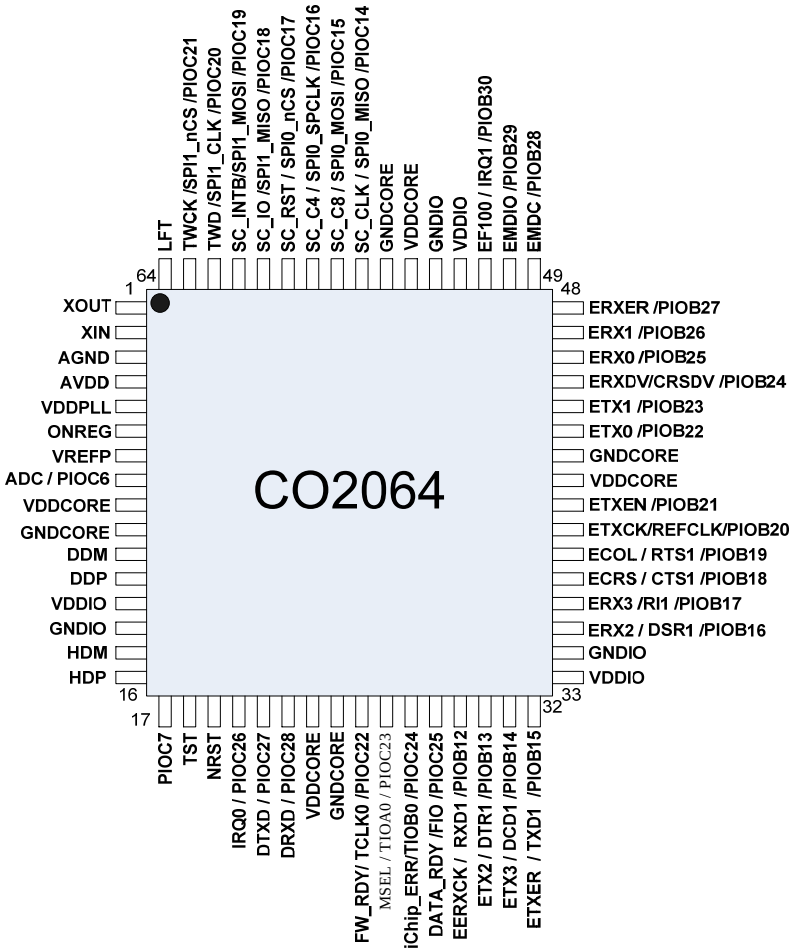


Figure 3-6: Pin-out for the 64-pin Package

3.2.6.1 Pin Description Table for CO2064/CO2128/CO2144

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
63	1	B2	PIOC21	IO	General purpose IO
			SPI1_CS	O	SPI1 chip select
			I2C_TWCK	I/0	TWI clock
64	2	C3	LFT	I	Leave unconnected
1	3	C2	XOUT	I	Crystal oscillator input
2	4	D3	XIN	O	Crystal oscillator output
3	5	D5	AGND	Analog	Low pass filter
4	6	E4	AVDD		A/D power supply
5	7	D4	VDDPLL		VDD PLL power supply (same voltage as VDDCORE)
6	8	A1	ONREG	I	'1' On-chip regulator enabled '0' On-chip regulator disabled
7	9	B1	ADVREF	I	VREF for ADC (same voltage as VDDIO)
8	10	C1	PIOC6	IO	General purpose IO
			HPI_D5	IO	HPI data line [5] (Only on CO2128/CO2144) (Not implemented)
			ADC	I	A/D analog input
9	11	D6	VDDCORE		VDD core power supply
10	12	H8	GNDCORE		GND core power supply
	13		NC		Leave unconnected
	14		NC		Leave unconnected
	15		NC		Leave unconnected
	16		NC		Leave unconnected
	17	F3	PIOC0	IO	General purpose IO
			nHPI_WAIT	O	HPI wait (Not implemented)
			ERR	O	Error indicator (Not implemented)
			SSC_RD	O	SSC receive data (Not implemented)
	18	F4	PIOC1	IO	General purpose IO
			HPI_D0	IO	HPI data line [0] (Not implemented)
			SSC_TD	O	SSC transmit data (Not implemented)
	19	F2	PIOC2	IO	General purpose IO
			HPI_D1	IO	HPI data line [1] (Not implemented)
			SSC_TK	O	SSC transmit clock (Not implemented)
	20	F1	PIOC3	IO	General purpose IO
			HPI_D2	IO	HPI data line [2] (Not implemented)
			SSC_RK	I	SSC receive clock (Not implemented)

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
	21	G4	PIOC4	IO	General purpose IO
			HPI_D3	IO	HPI data line [3] (Not implemented)
			SSC_TF	O	SSC transmit frame indicator (Not implemented)
	22	G3	PIOC5	IO	General purpose IO
			HPI_D4	IO	HPI data line [4] (Not implemented)
			SSC_RF	I	SSC receive frame indicator (Not implemented)
	23	G2	PIOC8	IO	General purpose IO
			HPI_D7	IO	HPI data line [7] (Not implemented)
			nRTS0	O	USART0 request to send
	24	G1	PIOC9	IO	General purpose IO
			nHPI_RD	O	HPI read, active low (Not implemented)
			nDSR0	I	USART0 data set ready
	25	H3	PIOC10	IO	General purpose IO
			nHPI_WR	O	HPI write, active low (Not implemented)
			nCTS0	I	USART0 clear to send
	26	H1	PIOC11	IO	General purpose IO
			nHPI_CS	O	HPI chip select, active low (Not implemented)
			RXD0	I	USART0 receive data
	27	H2	PIOC12	IO	General purpose IO
			HPI_IBF	O	HPI buffer full indicator (Not implemented)
			nDTR0	O	USART0 data terminal ready
	28	J1	PIOC13	IO	General purpose IO
			HPI_OBE	O	HPI Output Buffer Empty indicator (Not implemented)
			TXD0	O	USART0 transmit data
11	29	J2	DDM	Analog	USB device (+)
12	30	K1	DDP	Analog	USB device (–)
13	31	K3	VDDIO		VDD pad ring power supply
14	32	K4	GNDIO		GND pad ring power supply
15	33	L1	HDM	Analog	USB host (–)
16	34	L2	HDP	Analog	USB host (+)
17	35	M1	PIOC7	IO	General purpose IO
			HPI_D6	IO	HPI data line [6] (CO2128/CO2144 only) (Not implemented)
			SCLK0	O	USART0 synchronous Clock (Not implemented)
18	36	M2	TST	I	Test mode select

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
19	37	L3	nRST	I	Chip reset
20	38	M3	PIOC26	IO	General purpose IO
			IRQ0	I	External interrupt request [0]
21	39	L4	PIOC27	IO	General purpose IO
			TXD2	O	USART2 Transmit
22	40	M4	PIOC28	IO	General purpose IO
			RXD2	I	USART2 Receive
	41	J10	VDDIO		VDD power supply
	42	J5	PIOA0	IO	General purpose IO
			EBI_D0	IO	EBI data bus [0]
	43	K5	PIOA1	IO	General purpose IO
			EBI_D1	IO	EBI data bus [1]
	44	L5	PIOA2	IO	General purpose IO
			EBI_D2	IO	EBI data bus [2]
	45	M5	PIOA3	IO	General purpose IO
			EBI_D3	IO	EBI data bus [3]
	46	K2	GNDIO		GND power supply for IO pins
	47	K6	PIOA4	IO	General purpose IO
			EBI_D4	IO	EBI data bus [4]
	48	L6	PIOA5	IO	General purpose IO
			EBI_D5	IO	EBI data bus [5]
	49	M6	PIOA6	IO	General purpose IO
			EBI_D6	IO	EBI data bus [6]
23	50	D8	VDDCORE		VDD core power supply
24	51	G7	GNDCORE		GND core power supply
	52	K7	PIOA7	IO	General purpose IO
			EBI_D7	IO	EBI data bus [7]
	53	L7	PIOA8	IO	General purpose IO
			EBI_D8	IO	EBI data bus [8]
	54	M7	PIOA9	IO	General purpose IO
			EBI_D9	IO	EBI data bus [9]
	55	J7	PIOA10	IO	General purpose IO
			EBI_D10	IO	EBI data bus [10]
	56	K8	PIOA11	IO	General purpose IO
			EBI_D11	IO	EBI data bus [11]
	57	J8	PIOA12	IO	General purpose IO
			EBI_D12	IO	EBI data bus [12]
	58	L8	PIOA13	IO	General purpose IO
			EBI_D13	IO	EBI data bus [13]

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
25	59	M8	PIOC22	IO	General purpose IO
			TCLK0	I	External clock 0 input (Not implemented)
			FW_RDY	O	Firmware ready
26	60	L9	PIOC23	IO	General purpose IO
			TIOA0	IO	Timer I/O A0 (Not implemented)
			MSEL	I	Mode select
27	61	M9	PIOC24	IO	General purpose IO
			TIOB0	IO	Timer I/O B0 (Not implemented)
			iChip_ERR	O	iChip error indication
28	62	K9	PIOC25	IO	General purpose IO
			FIQ	I	External fast interrupt request (Not implemented)
			DATA_RDY	O	Data ready
29	63	L10	PIOB12	IO	General purpose IO
			MII_ERXCK	I	MII receive clock (MII only) (MII supported in Firmware 802 and above)
			RXD1	I	USART1 receive data
30	64	M10	PIOB13	IO	General purpose IO
			MII_ETX2	O	Transmit data (MII only) (MII supported in Firmware 802 and above)
			nDTR1	O	USART1 Data Terminal Ready
31	65	M11	PIOB14	IO	General purpose IO
			nDCD1	I	USART1 Data Carrier Detect
			MII_ETX3	O	Transmit data (MII only) (MII supported in Firmware 802 and above)
32	66	K10	PIOB15	IO	General purpose IO
			MII_ETXER	O	MII transmit coding error (MII only) (MII supported in Firmware 802 and above)
			TXD1	O	USART1 transmit data
33	67	J4	VDDIO		VDD power for IO pad ring
34	68	J9	GNDIO		GND power for IO pad ring
35	69	L11	PIOB16	IO	General purpose IO
			MII_ERX2	I	Receive data (MII only) (MII supported in Firmware 802 and above)
			nDSR1	I	USART1 Data Set Ready
36	70	K11	PIOB17	IO	General purpose IO
			MII_ERX3	I	Receive data (MII only) (MII supported in Firmware 802 and above)
			nRI1	I	USART1 Ring Indicator
37	71		PIOB18	IO	General purpose IO

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
		M12	MII_ECRS	I	Carrier sense (MII only) (MII supported in Firmware 802 and above)
			nCTS1	I	USART1 clear to send
38	72	L12	PIOB19	IO	General purpose IO
			MII_ECOL	I	Collision detected (MII only) (MII supported in Firmware 802 and above)
			nRTS1	O	USART1 request to send
39	73	K12	PIOB20	IO	General purpose IO
			MII_ETXCK	I	MII Transmit clock (MII supported in Firmware 802 and above)
			RMII_REFCLK	I	RMII reference clock
40	74	H10	PIOB21	IO	General purpose IO
			MII_ETXEN	O	Transmit enable
	75	J11	PIOA14	IO	General purpose IO
			EBI_D14	IO	EBI data bus [14]
	76	J12	PIOA15	IO	General purpose IO
			EBI_D15	IO	EBI data bus [15]
	77	H11	PIOA16	IO	General purpose IO
			EBI_A0	O	EBI address [0]
			NLB	O	EBI Lower Byte Select
	78	H12	PIOA17	IO	General purpose IO
			EBI_A1	O	EBI address [1]
	79	G10	PIOA18	IO	General purpose IO
			EBI_A2	O	EBI address [2]
	80	G11	PIOA19	IO	General purpose IO
			EBI_A3		EBI address [3]
	81	G12	PIOA20	IO	General purpose IO
			EBI_A4	O	EBI address [4]
41	82	E6	VDDCORE		VDD core power supply
42	83	G6	GNDCORE		GND core power supply
	84	F9	PIOA21	IO	General purpose IO
			EBI_A5	O	EBI address [5]
	85	F10	PIOA22	IO	General purpose IO
			EBI_A6	O	EBI address [6]
	86	F11	PIOA23	IO	General purpose IO
			EBI_A7	O	EBI address [7]
	87	F12	PIOA24	IO	General purpose IO
			EBI_A8	O	EBI address [8]
	88	E9	PIOA25	IO	General purpose IO

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
			EBI_A9	O	EBI address [9]
	89	E10	PIOA26	IO	General purpose IO
			EBI_A10	O	EBI address [0]
	90	E11	PIOA27	IO	General purpose IO
			EBI_A11	O	EBI address [11]
	91	H7	VDDIO		VDD power IO pad ring
	92	J6	GNDIO		GND power IO pad ring
43	93	E12	PIOB22	IO	General purpose IO
			MII_ETX0	O	MII/RMII transmit data [0]
44	94	D10	PIOB23	IO	General purpose IO
			MII_ETX1	O	MII/RMII transmit data [1]
45	95	D11	PIOB24	IO	General purpose IO
			MII_ERXDV	I	MII Receive data valid (MII supported in Firmware 802 and above)
			RMII_CRSDV	I	RMII carrier send and receive data valid
46	96	D12	PIOB25	IO	General purpose IO
			MII_ERX0	I	MII/RMII receive data[0]
47	97	C11	PIOB26	IO	General purpose IO
			MII_ERX1	I	MII/RMII receive data [1]
48	98	C12	PIOB27	IO	General purpose IO
			MII_ERXER	I	MII/RMII receive error
49	99	B12	PIOB28	IO	General purpose IO
			MII_EMDC	O	Management data clock
50	100	B11	PIOB29	IO	General purpose IO
			MII_EMDIO	IO	Management data IO
51	101	A12	PIOB30	IO	General purpose IO
			EF100	O	Force 100BaseT (RMII only)
			IRQ1	I	External interrupt request
52	102	H4	VDDIO		VDD power IO pad ring
53	103	J3	GNDIO		GND power IO pad ring
	104	C10	PIOA28	IO	General purpose IO
			EBI_A12	O	EBI address bus [12]
	105	B10	PIOA29	IO	General purpose IO
			EBI_A13	O	EBI address bus [13]
	106	A11	PIOA30	IO	General purpose IO
			EBI_A14	O	EBI address bus [14]
	107	B9	PIOB0	IO	General purpose IO
			EBI_A15	O	EBI address bus [15]

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
	108	A10	PIOB1	IO	General purpose IO
			EBI_A16	O	EBI address bus [16]
	109	B8	PIOB2	IO	General purpose IO
			EBI_A17	O	EBI address bus [17]
	110	A9	PIOB3	IO	General purpose IO
			EBI_A18	O	EBI address bus [18]
54	111	F5	VDDCORE		VDD core power supply
55	112	F8	GNDCORE		GND core power supply
	113	C7	PIOB4	IO	General purpose IO
			EBI_A19	O	EBI address bus [19]
	114	B7	PIOB5	IO	General purpose IO
			nEBI_RD	O	EBI read
			nEBI_OE	O	EBI output enable
	115	A7	PIOB6	IO	General purpose IO
			nEBI_RW0	O	EBI write 0
			nEBI_WE	O	EBI write enable
	116	B6	PIOB7	IO	General purpose IO
			nEBI_RW1	O	EBI write 1
			nEBI_UB	O	EBI upper byte
	117	A6	PIOB8	IO	General purpose IO
			nEBI_CS0	O	EBI chip select 0
	118	A5	PIOB9	IO	General purpose IO
			nEBI_WAIT	I	EBI wait indicator
	119	B5	PIOB10	IO	General purpose IO
			EBI_CS1	O	EBI chip select 1
			EBI_A20	O	EBI address bus [20]
	120	G8	VDDIO		VDD power supply IO pad ring
	121	H5	GNDIO		GND power supply IO pad ring
56	122	C5	PIOC14	IO	General purpose IO
			SPI0_MISO	IO	SPI0 MISO
			SC_CLK	O	Smart Card Clock (Not implemented)
57	123	A4	PIOC15	IO	General purpose IO
			SPI0_MOSI	IO	SPIO0 MOSI
			SC_C8	O	Smart Card C8 (Not implemented)
58	124	B4	PIOC16	IO	General purpose IO
			SPI0_SPCLK	IO	SPI0 Clock
			SC_C4	O	Smart Card C8 (Not implemented)
59	125		PIOC17	IO	General purpose IO

Pin# 64PP	Pin# 128PP	Pin# 144PP	Muxed Functions	Dir.	Description
		A3	SPI0_CS	IO	SPI0 Chip Select
			SC_RST	O	Smart Card Reset (Not implemented)
60	126	B3	PIOC18	IO	General purpose IO
			SPI1_MISO	IO	SPI1 MISO
			SC_IO	IO	Smart Card I/O (Not implemented)
61	127	C4	PIOC19	IO	General purpose IO
			SPI1_MOSI	IO	SPI1 MOSI
			SC_INTB	I	Smart Card Interrupt (Not implemented)
62	128	A2	PIOC20	IO	General purpose IO
			SPI1_CLK	IO	SPI1 Clock
			I2C_TWD	IO	TWI Data
		E8	VDDIO		VDD power supply IO pad ring
		D7	VDDIO		VDD power supply IO pad ring
		C9	VDDIO		VDD power supply IO pad ring
		G5	GNDIO		GND power supply IO pad ring
		E7	GNDIO		GND power supply IO pad ring
		D9	GNDIO		GND power supply IO pad ring
		C8	GNDIO		GND power supply IO pad ring
		C6	GNDIO		GND power supply IO pad ring
		G9	VDDCORE		VDD core power supply
		H6	VDDCORE		VDD core power supply
		H9	VDDCORE		VDD core power supply
		F7	GNDCORE		GND core power supply
		F6	GNDCORE		GND core power supply
		E5	GNDCORE		GND core power supply
		D2	JTAGSEL	I	JTAG Select: 0 – JTAG Enable 1 – JTAG Disable
		D1	TMS	I	JTAG Test Mode Select (Not implemented)
		E3	TCK	I	JTAG Test Clock (Not implemented)
		E2	TDI	I	JTAG Test Data Input (Not implemented)
		E1	TDO	O	JTAG Test Data Output (Not implemented)
		A8	VEXT_POR	I	For internal use (Not implemented)

Table 3-5: Pin-out for the 64/128/144-pin Packages

4 Typical Applications

4.1 CO2128/CO2144 Host interfaces and Internet Environment

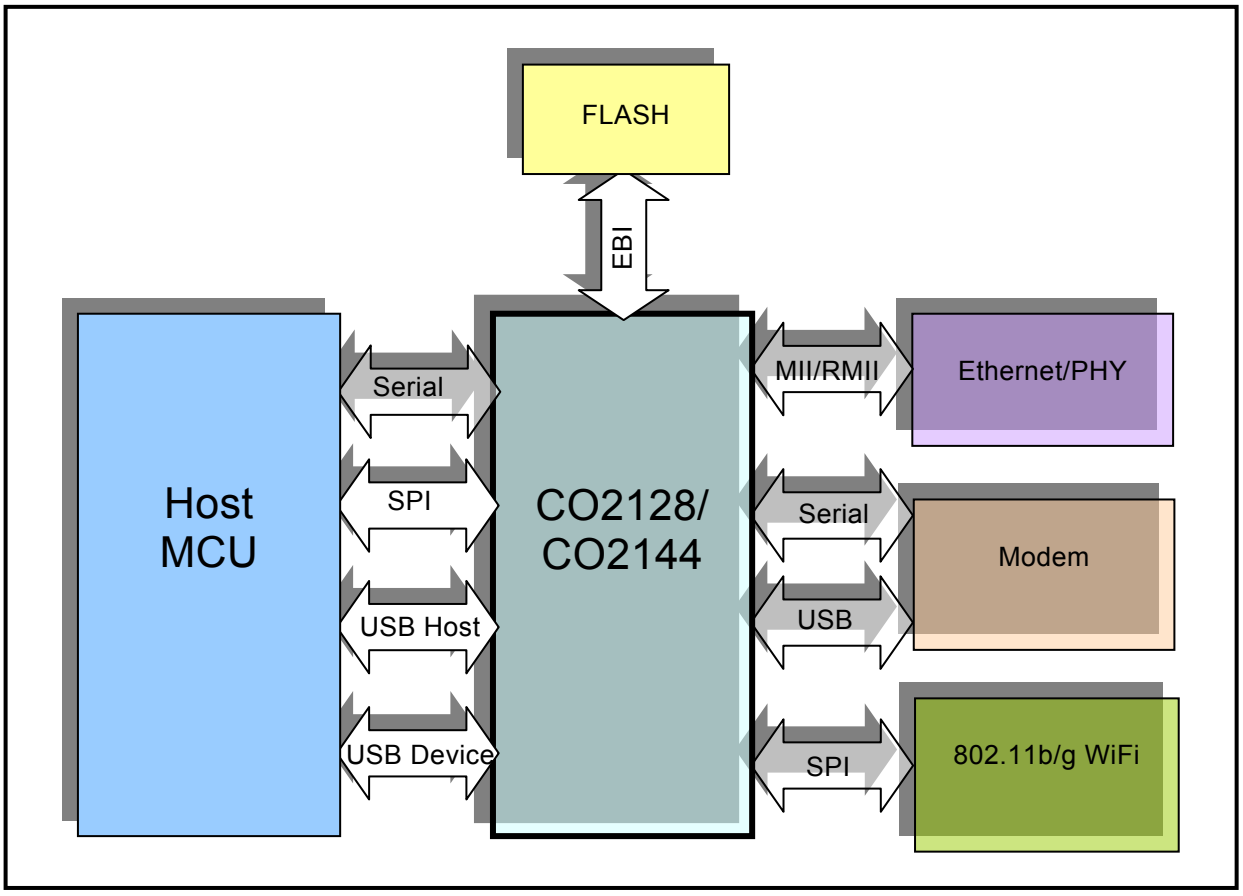


Figure 4-1: CO2128/CO2144 Typical Host and Internet Environment

4.2 CO2064 Host Interfaces and Internet Environment

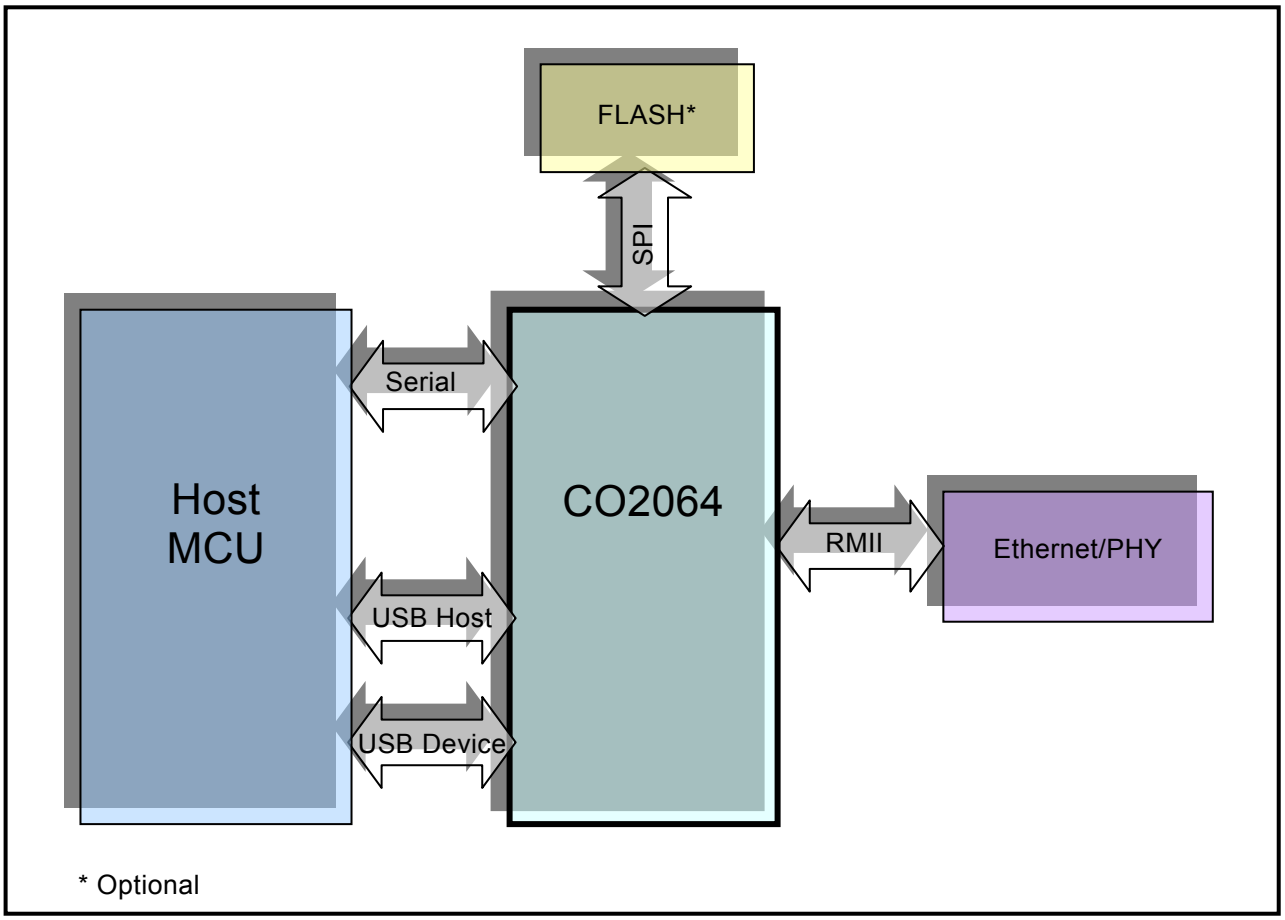


Figure 4-2: CO2064 Typical Host and Internet Environment

5 Functional Description

5.1 Overview

Connect One's iChip CO2064/CO2128/CO2144 IP communication controller is an integrated, firmware-driven, self-contained Internet engine. iChip accepts simple ASCII commands from a host CPU via a serial or parallel (CO2128/CO2144 only) communication channel and manages an Internet communication session to send and receive email, Web and WAP pages/files, utilize FTP and TELNET, serve as a serial-to-Internet router, or to manipulate sockets through a linked modem an Ethernet or Wireless LAN communications platform. CO2064/CO2128/CO2144 support a client SSL3/TLS secure socket, based on RFC2246. They support the following cipher suites:

- SSL_RSA_WITH_RC4_128_MD5 (0x0004)
- SSL_RSA_WITH_RC4_128_SHA (0x0005)
- SSL_RSA_WITH_3DES_EDE_CBC_SHA (0x000a)

CO2064/20128/CO2144 also support secure FTP using SSL3/TLS sockets for both command and data channels, based on RFC 2228 and the IETF Internet-draft "Securing FTP with TLS". For 10/100BaseT Ethernet applications, iChip includes the firmware and pin-out necessary to drive any external RMII or MII PHY (MII supported in Firmware 802 and above). For wireless LAN applications, iChip includes the firmware and pin-out necessary to drive a PCMCIA or CF WiFi card based on the Marvell 88W8686 802.11b/g chipset. Both WEP and WPA security over WiFi are supported.

5.2 Technical Specifications

5.2.1 General

iChip constitutes a complete Internet messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. One of several local communication links may be used to connect iChip to the host processor:

- An industry-standard asynchronous serial link
- TWI
- SPI
- USB
- High-speed 8-bit parallel port

Programming, monitoring and control are fully supported using Connect One's AT+i™ extension to the standard AT command set.
iChip connects to land-line or cellular modems and to an Ethernet PHY or WiFi chipset for Internet access. An AT+i command is provided to switch between the modem and Ethernet/WiFi.

5.2.2 Firmware Upload

iChip is based on an internal ROM-based boot loader and internal SRAM used for its functional implementation. The device does not include internal flash memory. As a result, iChip is designed to accept a firmware upload, using its built-in boot loader, after each power-on cycle. In addition, the CO2128/CO2144 have an external bus that allows them to run from an external memory device (such as flash).
iChip can receive the firmware upload from a series of interfaces, allowing embedded system designers a wide choice of alternatives that best suit each application.
iChip firmware sources are separated into two distinct categories: passive sources and active sources. Passive sources are generally storage devices, such as flash, EPROM or battery-backed RAM that are connected to iChip. iChip's boot loader detects passive sources and attempts to upload its firmware by directly accessing these devices. Active sources are envisioned to be other processor based devices that communicate with iChip over one of its available interfaces and actively download iChip's firmware.
Note that, in each application, only one firmware source need be employed.

5.2.2.1 Passive Devices

iChip CO2128/CO2144 support any memory device, such as flash, EPROM, EEPROM, battery-backed RAM, etc. that are attached and configured on their 16-bit local bus or SPI interface. iChip supports memory devices attached to the SPI interface. When a passive device is connected, iChip's boot loader detects it, uploads its firmware, and starts execution. In the case of CO2128/CO2144, a dedicated pin may be tied LOW during power on reset to force iChip to begin executing from a memory device configured on its external bus, rather than uploading firmware into its internal SRAM.

5.2.2.2 Active Devices

When passive devices are not detected, iChip waits for an active device over any one of its available interfaces. These include:

- USARTs

- SPI
- Two-wire
- USB host or device
- High speed parallel

The active device exchanges several handshaking transmissions with iChip to establish a connection, then uploads the firmware. Upon completion, iChip automatically boots from the uploaded application.

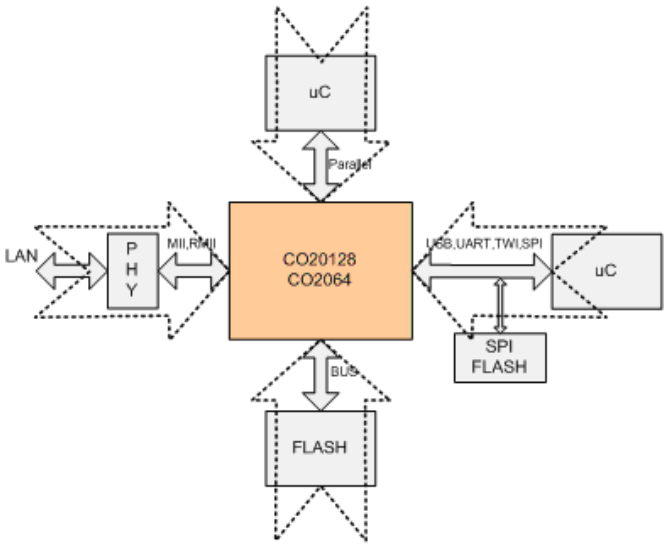


Figure 5-1: iChip Firmware Upload Sources

5.2.3 Default Parameter Values

iChip accepts local default parameter values via an upload following the firmware upload. After receiving a firmware upload following the power-up sequence, iChip's parameters are set to the factory default values. A dedicated upload may optionally follow the firmware upload with different default values for specific parameters. The upload source (whether passive or active) may be the same as the firmware source or a different one.

5.2.4 Operation

All iChip Internet and parameter operations are controlled by AT+i commands.

5.2.4.1 Transparent Mode

In modem communications mode, iChip defaults to transparent mode, allowing the host to control the modem device directly. Control is implemented by issuing standard AT commands to iChip. In this mode, iChip transparently echoes the AT commands to the modem, as well as echoing the modem responses back to the host. iChip supports interlacing AT+i and AT commands while the modem is in command mode. When the modem is put into data mode by issuing a dial command, transparent mode is sustained throughout the data mode session.

5.2.4.2 Command Mode

iChip commands are implemented using the AT+i command set. Command flow exists only on the link between the host and iChip.

5.2.4.3 Internet Mode

iChip enters Internet mode after being issued an Internet command such as to send or receive an email message, open a socket, etc. iChip attempts to establish an Internet connection and carry out the required activity through the communication platform link. While in this mode, AT+i commands are supported to monitor and control the process, as well as activate any of the supported protocols.

5.2.4.4 SerialNET Mode

iChip's SerialNET mode extends a local asynchronous serial link to a TCP or UDP socket across a LAN or Internet. Its main purpose is to allow simple devices, which normally interact over a serial line, to interact in a similar fashion across a network, without requiring any changes in the device itself. iChip contains a set of associated operational parameters, which define the nature of the desired network connection. iChip supports both Server and Client modes in SerialNET mode. AT+i commands are not required to operate SerialNET mode. Thus, SerialNET mode may be used in existing systems with little or no need to modify the application program.

5.2.4.5 Routing Mode

iChip supports routing of Internet packets among its various communication platforms. Available routing options are:

- Dial-Up/Cellular ⇔ 10/100 Ethernet
- Dial-Up/Cellular ⇔ 802.11b/g
- 10/100 Ethernet ⇔ 802.11b/g

To provide seamless routing, iChip comes equipped with Network Address Translation (NAT) capabilities and a DHCP server that supports up to 255 clients.
iChip performs routing as an operation mode in which, upon power-up or reset, only pre-configured routing rules from one communication platform to another are applicable. Alternatively, iChip can accept AT+i commands from the host while still maintaining uninterrupted routing between two communication platforms.
Typical configurations for the routing mode are:

- Wireless Access Point for LAN devices
- Cellular Gateway for LAN or WiFi network
- Dial-up/cellular link serves as a backup channel

5.2.4.6 USB Services Mode

In this mode, iChip provides the host application with USB services, thus offloading USB tasks and eliminating the need for the host to implement USB-related code. USB services can be provided over the USB Device Port or USB Host Port. Typical services can be bridging information from USB to another interface (Ethernet, for example), serving as a USB host or client while using a simple interface such as UART to send and receive information from the host application CPU.

5.2.5 Remote Internet Firmware Update

New firmware may be uploaded from a remote location using standard Internet protocols. When iChip boots from a local flash device, it accepts firmware updates from a remote FTP or HTTP server, as well as firmware uploads from a remote browser through iChip's web server.

5.2.6 10/100BaseT Ethernet LAN Connection

iChip interfaces an Ethernet LAN PHY device via a dedicated, fully compliant MII or RMII interface, as shown in Table 5-1. (**MII supported in Firmware 802 and above**)

MII Signals	RMII Signals	Function
MII_ETX0	MII_ETX0	MII transmit line 0
MII_ETX1	MII_ETX1	MII transmit line 1
MII_ETX2		MII transmit line 2
MII_ETX3		MII transmit line 3
MII_ETXCK	 EREFCK	Transmit clock (MII only) Reference clock (RMII only)
MII_ETXEN	MII_ETXEN	Transmit enable
MII_ETXER		MII transmit coding error
MII_ERX0	MII_ERX0	MII receive line 0
MII_ERX1	MII_ERX1	MII receive line 1
MII_ERX2		MII receive line 2
MII_ERX3		MII receive line 3
MII_ERXCK		MII receive clock
MII_ECOL		Collision detected
MII_ ERXDV	CRSDV	Receive data valid (MII only) Carrier send and receive data valid (RMII only)
MII_ERXER	MII_ERXER	Receive error
MII_ EMDC	MII_ EMDC	Management data clock
MII_ EMDIO	MII_ EMDIO	Management data IO

Table 5-1: MII / RMII Interface

5.2.7 Serial Host Connection

iChip supports a full-duplex serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR and DSR lines, is supported. iChip supports standard baud rate configurations from 2,400 bps up to 3Mbps on the host asynchronous serial communications channel. A fixed baud rate may be defined by using the AT+iBDRF command. Without a fixed baud rate setting, iChip defaults to auto baud rate detection.

128-pin	144-pin	Pin name	Function
26	H1	RXD0	USART0 receive data
28	J1	TXD0	USART0 transmit data
24	G1	nDSR0	USART0 data set ready
25	H3	nCTS0	USART0 clear to send
27	H2	nDTR0	USART0 data terminal ready

Table 5-2: Serial Host Interface

5.2.8 Parallel Host Connection

The high-speed parallel interface (HPI) is a glueless connection to an 8-bit parallel port.

128-pin	144-pin	Pin name	Function
18	F4	HPI_D0	HPI data line 0
19	F2	HPI_D1	HPI data line 1
20	F1	HPI_D2	HPI data line 2
21	G4	HPI_D3	HPI data line 3
22	G3	HPI_D4	HPI data line 4
10	C1	HPI_D5	HPI data line 5
35	M1	HPI_D6	HPI data line 6
23	G2	HPI_D7	HPI data line 7
24	G1	nHPI_RD	HPI read, active low
25	H3	nHPI_WR	HPI write, active low
26	H1	nHPI_CS	HPI chip select, active low
27	H2	HPI_IBF	HPI buffer full indicator
28	J1	HPI_OBE	HPI output buffer empty indicator

Table 5-3: Parallel Host Interface

5.2.9 Serial Connection to Analog Modem

iChip supports a full-duplex, TTL-level serial communications link with a modem device. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR, DSR, CD and RI lines, is supported.

64-pin	128-pin	144-pin	Pin name	Function
32	66	K10	TXD1	USART1 transmit data
29	63	L10	RXD1	USART1 receive data
37	71	M12	nCTS1	USART1 clear to send
38	72	L12	nRTS1	USART1 request to send
35	69	L11	nDSR1	USART1 data set ready
31	65	M11	nDCD1	USART1 data carrier detect
30	64	M10	nDTR1	USART1 data terminal ready
36	70	K11	nRI1	USART1 ring indicator

Table 5-4: Serial Modem Interface

5.2.10 Hardware and Software Flow Control

Hardware flow control is supported between the host serial connection and iChip. Flow control is programmed via the AT+iFLW command. The default flow control method is set to “wait/continue” software flow control (which is similar to XON/XOFF software flow control) between iChip and the host processor.

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip to either use hardware flow control or “wait/continue” software flow control. The flow control mechanism is based on the RTS/CTS signals.

Hardware flow control is supported on iChip’s serial and parallel (HPI) connections. The host parallel connection has built-in hardware flow control signals as part of the interface logic.

6 Hardware Interface

6.1 Power Connection

iChip supports a single 3.3V supply mode. The internal regulator input is connected to the 3.3V source and its 1.2V output feeds VDDCORE and VDDPLL, as shown in Figure 6-1. When ONREG=0, the internal power regulator is disabled and VDDCORE and VDDPLL need to be connected to an external power supply of 1.2V. When ONREG=1, the internal power regulator is enabled and a decoupling capacitor has to be connected to pin 5 (64PP), pin 7 (128PP), or pin D4 (144PP).

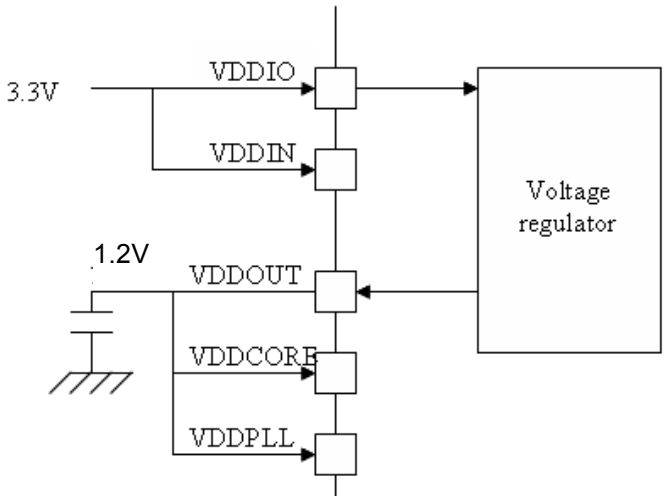


Figure 6-1: iChip Power Connection

6.2 Crystal Connection

The typical crystal connection is illustrated in the figure below.

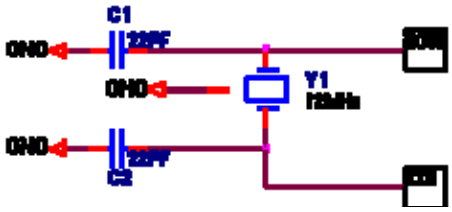


Figure 6-2: Crystal Connection

6.3 Serial Host Interface

iChip supports a full-duplex serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, DTR and DSR, is supported. iChip supports standard baud rate configurations from 2,400 bps up to 3Mbps on the host asynchronous serial communications channel. The default baud rate may be changed permanently by using the AT+iBDRF command. Auto baud rate setting is supported for all standard baud rates.
The host interface is a serial DTE interface. Speeds of up to 3Mbps are supported in the following data format:

Mode	Parity	Data Length (# of bits)	# of Stop Bits	Transmission Length (# of Bits)
Command	None	8	1	10
SerialNET	Even, Odd	7, 8	1, 1.5, 2	9, 10, 11

Table 6-1: Host Data Format

6.4 Parallel Host Interface

The parallel interface is a glueless connection mode, in which iChip connects to a host CPU through a parallel interface using a one byte, full-duplex mailbox latch, allowing the host to read or write a full byte to/from the iChip. The host software may transfer bytes one at a time or configure the interface to use DMA. Supported transfer rates are as high as 32 Mbps.
iChip is connected to the parallel interface through the following signals:

- nHPI_CS: Parallel chip select signal. When HPI_nCS is LOW, the iChip is selected.
- nHPI_RD: When –RD is LOW, iChip reads data from host.
- nHPI_WR: When – WR is LOW, iChip writes data to host.
- HPI_D0 — HPI_D7: Bi-directional data bus
- nHPI_WAIT: HPI wait request
- ERR: Parallel error. When HIGH, indicates error on the parallel interface.
- HPI_OBE: Parallel output buffer empty. When HIGH, indicates that the output buffer is empty and iChip can send additional data to host. When iChip sends a data byte, this signal goes LOW until the host reads the data.
- HPI_IBF: Parallel input buffer full. When HIGH, indicates that the input buffer is full and iChipc cany read a data byte from the host. When iChip reads the data byte, this signal goes LOW.

6.5 HPI Bus Interface

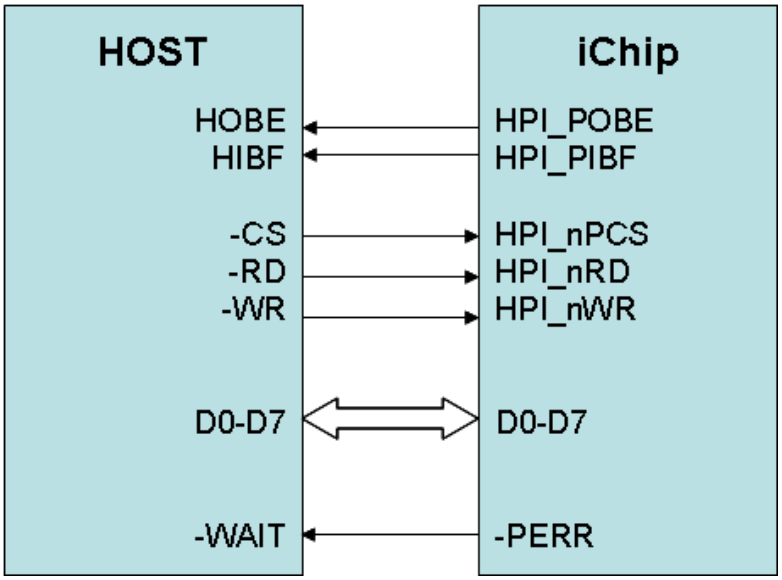


Figure 6-3: Bus Interface Connection

6.6 LAN/WiFi Interface

iChip directly interfaces an Ethernet LAN PHY device on its 8-bit local bus. Currently iChip supports the Davicom DM9161A Ethernet PHY for 10/100BaseT. For Wireless LAN applications, iChip supports a CF WiFi card based on the Marvell 88W8686 802.11b/g WiFi chipset.

6.7 Serial Modem Interface

iChip includes a dedicated port to interface a serial modem. The modem interface is a serial DCE interface. Speeds of 2400, 4800, 9600, 19200, 38400, 57600, 115200 and 230400 bps are supported in the following data format:

Mode	Parity	Data Length (# of bits)	# of Stop Bits	Transmission Length (# of Bits)
Command	None	8	1	10
SerialNET	None	8	1	10

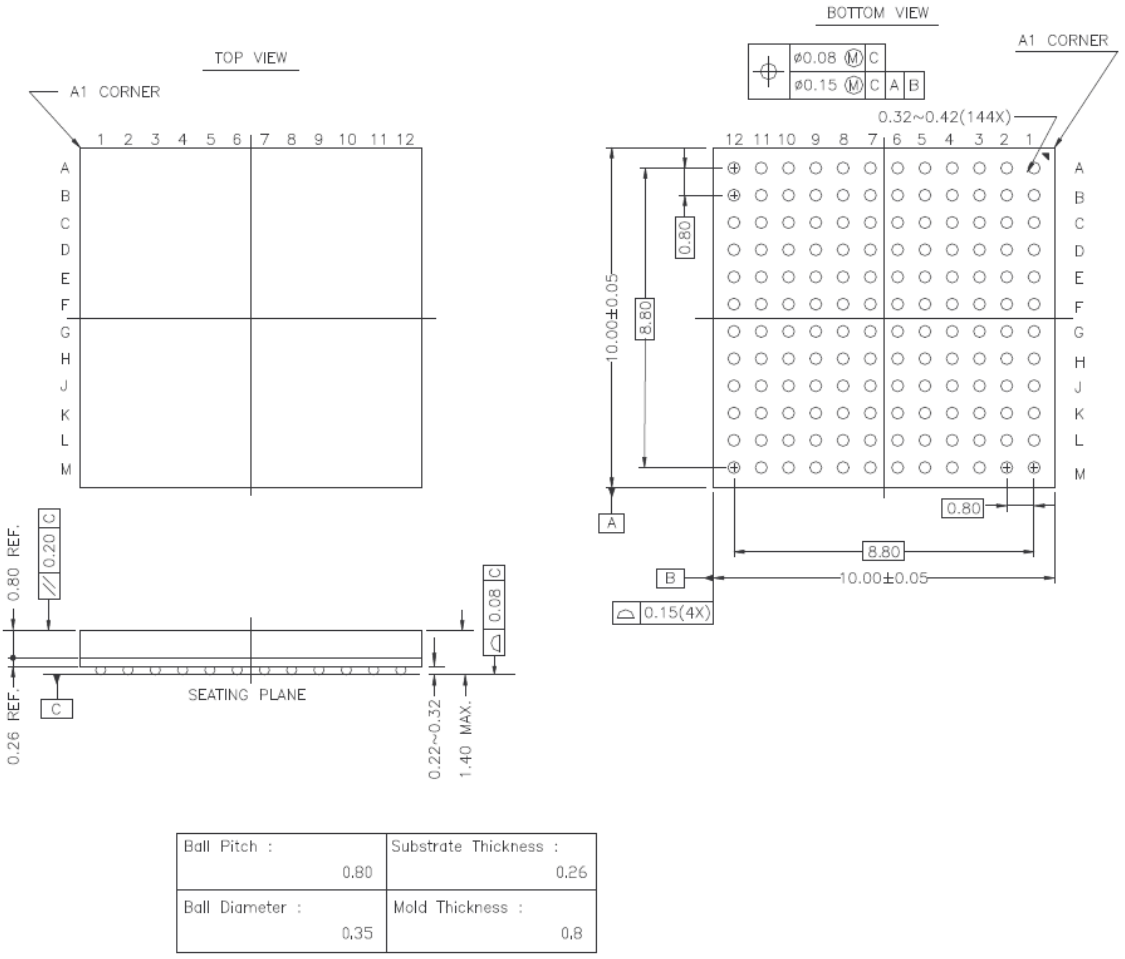
Table 6-2: Modem Data Format

Actual baud rate may be preprogrammed or dynamically defined as equal to the auto baud rate detected on the serial host interface (when the iChip operates in serial mode). When iChip operates in parallel mode, the modem interface baud rate must be preprogrammed.

7 Mechanical Characteristics

7.1 LFBGA 144-pin

- Body: 10.0 x 10.0 x 1.4 mm
- Pitch: 0.8 mm

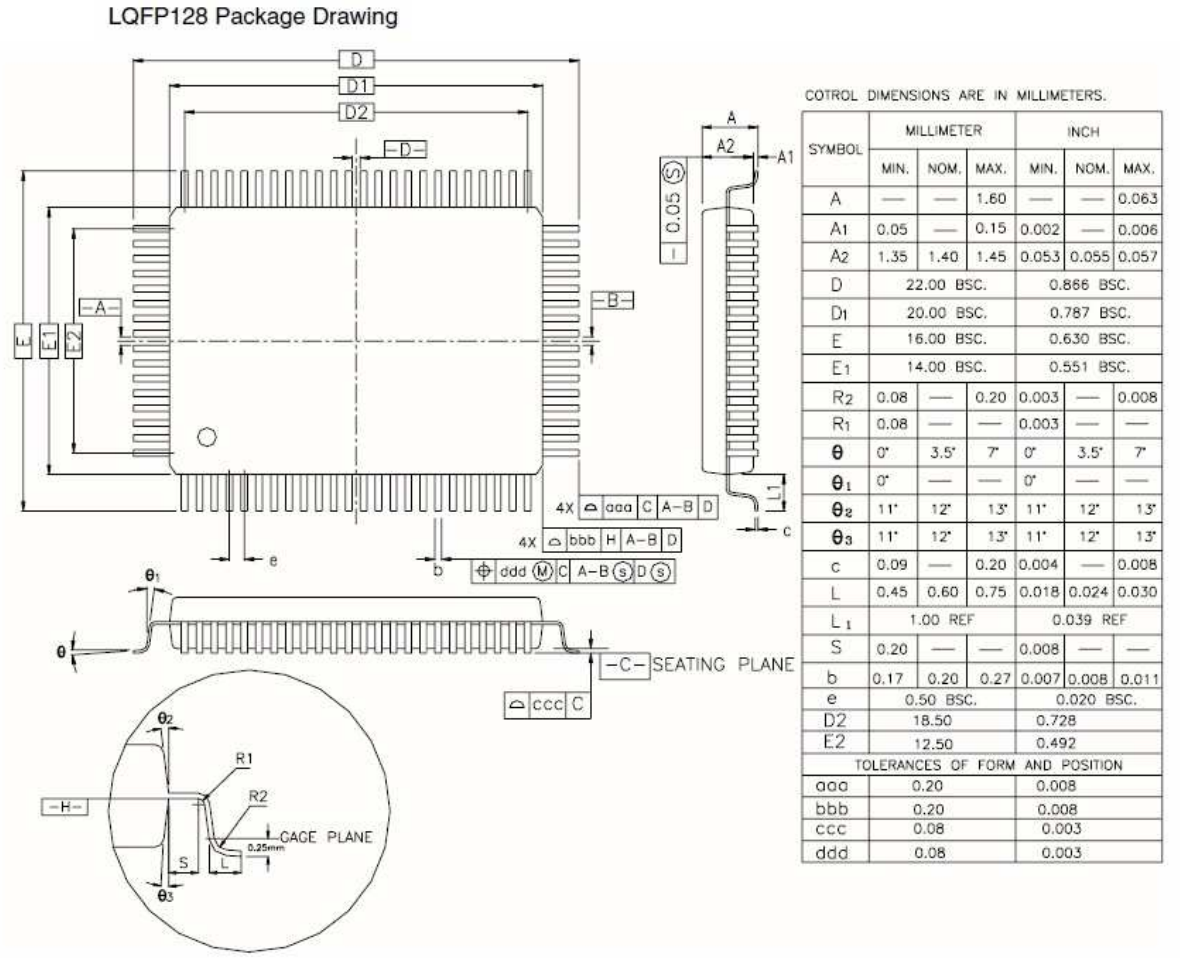


Ball Pitch : 0.80	Substrate Thickness : 0.26
Ball Diameter : 0.35	Mold Thickness : 0.8

Figure 7-1: LFBGA 144-pin

7.2 Low-profile Quad Flat Pack (LQFP), 128-pin

- Body: 14 x 20 x 1.4 mm
- Pitch: 0.5 mm



COTROL DIMENSIONS ARE IN MILLIMETERS.

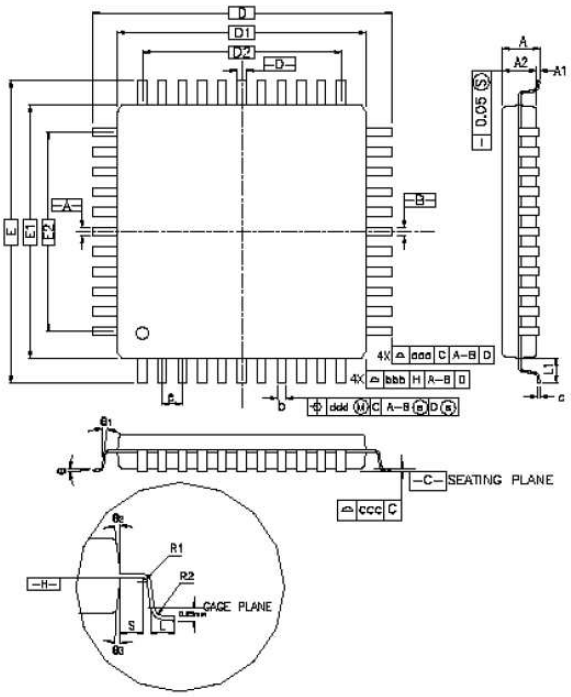
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 7-2: Low-profile Quad Flat Pack (LQFP), 128-pin

7.3 Low-profile Quad Flat Pack (LQFP), 64-pin

- Body: 10 x 10 x 1.4 mm
- Pitch: 0.5 mm

64-lead LQFP Package Drawing



Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 7-3: Low-profile Quad Flat Pack (LQFP), 64-pin

8 Electrical Specifications

8.1 Power Supply Connection

Figure 8-1 outlines the power supply connection required for iChip operation.

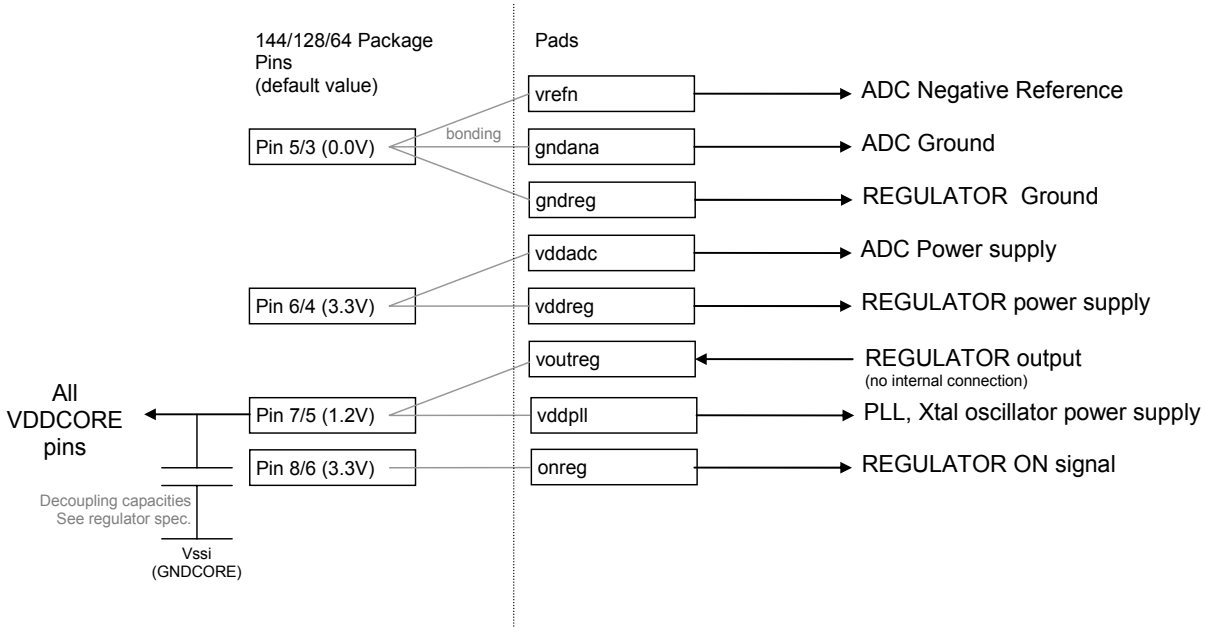


Figure 8-1: Power Supply Connection

All VDDCORE/GNDCORE pins are supplying glue logic, RC oscillator and POR. All 3.3V VDDIO/GNDIO pins are supplying all pad ring cells (pads).

8.2 Power Dissipation

The following parameters should be used for power dissipation calculation:
Worst case power dissipation 300mW
For 128-pin LQFP and 144-pin BGA Theta JA (C/W):

Air flow is 0 m/s : 44.4

Air flow is 1 m/s : 37.7

Air flow is 2 m/s : 35.8

For 64-pin LQFP Theta JA (C/W):

Air flow is 0 m/s : 47.9

Air flow is 1 m/s : 41.0

Air flow is 2 m/s : 39

8.3 I/O Line

8.3.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and are not 5V tolerant. TMS, TDI and TCK do not integrate a pull-up resistor. TDO is an output, driven at up to VDDIO, and has no pull-up resistor. The JTAGSEL pin is used only on the prototype. It enables or disables the JTAG debug functionality.

8.3.2 Reset Pin

The NRST pin is bidirectional with an open drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the NRST pin as system user reset, and the use of the signal NRST to reset all the components of the system. The NRST pin integrates a permanent pull-up resistor to VDDIO.

8.3.3 PIO Controller Lines

All the PIO lines spec to 3.3V with +/- 10% and have an integrated programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers. Driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled can lead to unpredictable results. Care should be taken, in particular at reset, as all the I/O lines default to input with pull-up resistor enabled at reset.

8.3.4 I/O Lines Current Drawing

All the PIO lines can draw up to 8 mA. However, the total current drawn by all the I/O lines must not exceed 150 mA.

8.4 Environmental Specifications

8.4.1 Absolute Maximum Ratings

Parameter	Rating
Voltage at any pin with respect to ground	-0.3 to +3.6 Volts
Operating temperature	-40°C to 85°C (-40°F to 185°F)
Storage temperature	-60°C to 150°C (-76°F to 302°F)

Table 8-1: Environmental Specifications – Maximum Ratings

8.4.2 DC Operating Characteristics

Table 8-2 displays the characteristics applicable to the operating temperature range (see Table 8-1), certified for a junction temperature up to TJ = 100°C.

Symbol	Parameter	Conditions		Min	Typical	Max	Units
V_{DDCORE}	DC Supply Core			1.08		1.32	V
V_{DDPLL}	DC Supply PLL			1.08		1.32	V
V_{DDIO}	DC Supply I/Os			3.0		3.6	V
V_{IL}	Input low-level voltage	V_{DDIO} from 3.0V to 3.6V		-0.3		0.8	V
V_{IH}	Input high-level voltage	V_{DDIO} from 3.0V to 3.6V		2.0		3.6	V
V_{OL}	Output low-level voltage	I_{Omax}, V_{DDIO} from 3.0V to 3.6V				0.4	V
V_{OH}	Output high-level voltage	I_{Omax}, V_{DDIO} from 3.0V to 3.6V		V_{DDIO}-0.4			V
I_{LEAK}	Input leakage current	Per PIO, pull-up resistors disabled (Typ: T_A=25°C, Max: T_A=85°C)			40	400	nA
I_{PULLUP}	Input pull-up current	Per PIOs (with pull-up), V_{DDIO} from 3.0V to 3.6V, PIOs connected to ground		120	321	600	µA
$I_{PULLDOWN}$	Input pull-down current, (TST, JTAGSEL)	Per PIOs (with pull-down), V_{DDIO} from 3.0V to 3.6V, pins connected to V_{DDIO}		120	295	550	µA
C_{IN}	Input capacitance	128 LQFP package				13.9	pF
I_{SC}	Static current	On V_{DDCORE}=1.32V, MCK=500Hz All inputs driven at 1 (including TMS, TDI, TCK, NRST) All peripherals off	T_A=25°C		200		µA
			T_A=85°C		1000		
I_O	Output current	V_{DDIO} from 3.0V to 3.6V				8	mA
T_{SLOPE}	Supply core slope			6			V/ms
$I_{VDDCORE}$	Current on V_{DDCORE}	V_{DDCORE}=1.2V			20		mA
		With internal oscillator operating at 32KHz, T_A=25°C			500		µA
I_{VDDIO}	Current on V_{DDIO}	V_{DDIO}=3.3V			50		mA

Table 8-2: DC Operating Characteristics

8.4.2.1 USB DC Parameters

Table 8-3 displays the USB DC parameters.

Code	Parameter	MIN	MAX	Unit
VIH	High Level Input Voltage	2.0		V
VIL	Low Level Input Voltage		0.8	V
Vhys	Hysteresis	0.2		V

Table 8-3: USB DC Parameters

8.4.2.2 ADC Electrical Specifications

Table 8-4 displays the Analog-to-Digital Converter electrical specifications.

- Junction temperature range: [-40°C to +100°C], worst cases of vdd and process, unless otherwise noted.
- Unless otherwise noted, Min/Max are 3σ values.

Code	Parameter	Conditions	Min	Typ	Max	Unit
R	Resolution			10		Bits
INL	Integral Non Linearity	End point method			±4	LSB
DNL	Differential Non Linearity				±2	LSB
OS	Offset Error	Not including V_{REFN} error	-1.5	0.5	+2.5	LSB
GE	Gain Error				±2	LSB
ENOB	Effective Number Of Bit	@4MHz			9	Bits
	Conversion Rate Conversion Time Track-and-Hold Acquisition Time Throughput Rate	 Clock Frequency=4MHz See ***Note 1*** @ f_{clk}=4MHz	 2.0	 2.5	 200	 µS µS kS/s
V_{refp} I_{refp}	Positive Reference Input V_{refp} Input Voltage Range V_{refp} Average Current		V_{refn}+2.6	3.3	a33vdd 1100	V µA
V_{refn} I_{refn}	Negative Reference Input V_{refn} Input Voltage Range V_{refn} Average Current		0		V_{refp}-2.6 1100	V µA
V_{in} Z_{in} I_{in} C_{in}	Analog Input V_{in} Input Voltage Range V_{in} Input Source Impedance V_{in} Peak Current DC Leakage Current Input Capacitance	 See ***Note 1*** See ***Note 2***	V_{refn}	 50 4	V_{refp} 6250 2.5 ±1 6	V Ω mA µA pF

Table 8-4: ADC Electrical Specifications

Note 1: In worst case, the Track-and-Hold Acquisition Time is given by: $T_{TH}(ns)=500+0.08*Z_{in}(\Omega)$. The full speed is obtained for T_{TH}=1000ns with an input source impedance of 6250Ω max, corresponding to 8 clock periods at maximum clock frequency, f_{clk}=8MHz.

Note 2: Maximum peak current specified is a function of differential input voltage (ΔVin) between two successive conversions and input impedance Z_{in}. In worst case, the maximum input peak current is given by: $I_{IN\ pk\ max} = \frac{V_{in}(n-1)-V_{in}(n)}{1200+Z_{in}}$

8.4.2.3 PLL Parameters

Table 8-5 displays the PLL parameters.

Temperature Range: [-40ºC to +85ºC], worst cases of vdd & Process unless otherwise noted.

Code	Parameter	Condition	Min	Typ	Max	Unit
Vdd	Supply voltage	See standard operating conditions below	1.08	1.2	1.32	V
ΔVdd	Supply ripple	rms value, 10 kHz to 10 MHz (1) rms value > 10MHz			30 10	mV mV
Idd on	Current consumption	***en*** = 1, ***test*** = 00, with Cload = 0.2pF on ***ck*** *Freq of* ***ck*** *@ 150MHz*		-	2.5	mA
Idd stdby	Standby current consumption	***en*** = 0, ***test*** = xx, + silent entries			TBD	µA
Fckr	Input Frequency	On ***ckr***	1		32	MHz
Fck	Output Frequency	On ***ck***	50		150	MHz
D	Duty Cycle	On ***ck.***	40		60	%
Skew	Static delay	Between ***ckr*** and ***ck***, lead or lag			500	ps
Jc	Cycle Jitter	peak value in percent of output clock period This parameter depends on vdd noise		2	5	%
Δϕ	Total Phase Error (Long Term Jitter)	rms value peak = 7*Δϕ*Ck_period /(2π) @100MHz	- -	- -	200 2.2	mrad ns
Tau	Settling Time	Depends on internal filter settings		0.3	1	ms
Os	Output frequency overshoot during startup	• Depends on the PLL settings, and the LFT filter used (Fckr=4MHz, Fck=96MHz, filter lft18f4x96)		-	15	%
Kv	VCO frequency gain	ivco=01 default at Fck=100MHz	150	260	350	MHz/V
Ip	Pump current	icp=00 not used **icp=01 default** icp=10 not used icp=11 not used	2 **3** 4 6	3 **4.5** 6 9	4 **6** 8 12	µA

(1) Additional notes versus are added bellow, concerning High Frequency Noise filtering

Table 8-5: PLL Parameters

8.4.2.4 Crystal Oscillator Parameters

Table 8-6 displays the crystal oscillator parameters.

Temperature Range: [-40ºC to +85ºC], worst cases of vdd & Process unless otherwise noted.

Code	Parameter	Condition	Min	Typ	Max	Unit
Avdd	Supply voltage	See standard operating conditions below	1.08	1.2	1.32	V
ΔAvdd	Supply ripple	rms value, 10 kHz to 10 MHz			20	mV
Idd on	Current consumption	@ 16 MHz		TBD	TBD	uA
Idd bypass	Current consumption	onosc = 0		TBD	TBD	uW/MHz
Freq	Operating frequency		8		16	MHz
Duty	Duty Cycle		40		60	%
Ton	Startup time	With crystal defined below			2	ms
Pon	Drive level				150	uW
ESR	Equivalent Serie Resistance	@ 16MHz			60	Ω
Cm	Motional capacitance		5		9	fF
Cshunt	Shunt capacitance				7	pF
Cload	Load capacitance	Max external capacitors: 40pF	15		20	pF
Idd stdby	Standby current consumption	***onosc*** = 0			TBD	µA

Table 8-6: Crystal Oscillator Parameters

8.4.2.5 POR Parameters

Table 8-7 displays the POR parameters.

Temperature Range: [-40ºC to +85ºC], worst cases of vdd & Process unless otherwise noted.

Code	Parameter	Condition	Min	Typ	Max	Unit
Vdd	Power supply range		1.08	1.2	1.32	V
Vdd sl	Vdd Slope		2V/30ms			
Vop	Vop (operating voltage rising)	Slope of +2.0V/200ms			TBD	V
Vth+	Vth+ (threshold voltage rising)	Slope of +2.0V/200ms		0.7		V
Vth-	Vth- (threshold voltage falling)	Slope of +2.0V/200ms		0.63		V
Hyst	Vth+ - Vth (hysteresis)	Slope of +2.0V/200ms		80		mV
Tres	Tres (reset time)	Vdd rising from 0 to 1.2V +/- 10%		200		µs
Tvddfall	Vdd fall time	Min fall time necessary to generate a reset signal	150			µs
Diglvl	Digital Level	on ***res***	1.08	1.2	1.32	V
Iddtran	Current surge consumption	During Tres			300	µA
Iddstat	Current consumption	After Tres		1.5		µA

Table 8-7: POR Parameters

8.4.2.6 32 KHz RC Oscillator Parameters

Table 8-8 displays the 32 KHz RC oscillator parameters.

Temperature Range : [-40ºC to +85ºC], worst cases of Vdd & Process unless otherwise noted.

	Parameter	Condition	Min	Typ	Max	Unit
Vddi	Supply voltage		1.08	1.2	1.32	V
F0	Frequency		20	32	44	KHz
F0sd	Frequency supply dependency	F0 is given @1.2V	-3	F0	+3	%
F0td	Frequency temperature dependency	F0 is given @25C	-10	F0	+10	%
ΔF0sd	Maximum frequency supply slope (see note 1)		-25		+25	%/V
ΔF0td	Maximum frequency temperature slope (see note 2)		-0.16		+0.16	%/C
Duty	Duty cycle		45	50	55	%
Idd on	Power consumption OSCILLATION	After startup time		0.65	1	uA
Ton	Startup time				75	us
Idd stdby	Standby consumption	onrc = 'L'			0.2	uA

Note 1 : Gives the maximal variation of the frequency on a small supply variation.
Note 2 : Gives the maximal variation of the frequency on a small temperature variation.

Table 8-8: 32 KHz RC oscillator parameters

8.4.2.7 1.2V Internal Regulator Parameters

Parameter	*Name*	*Conditions*	*Min*	*Typ*	*Max*	*Unit*
Input supply voltage	*mix33vdd*	*Slope<3V/µs*	*2.7*	*3.3*	*3.6*	*V*
Output supply voltage Normal Mode	*vddi*	*onreg33='1'*	*1.08*	*1.2*	*1.32*	*V*

Table 8-9: 1.2V Internal Regulator Parameters

8.4.3 AC Operating Characteristics

Master Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
1/(t_{CPMCK})	Master Clock Frequency			48	MHz

8.4.3.1 PIO Characteristics

Table 8-10 displays the PIO characteristics.

Symbol	Parameter	Conditions	Min	Max	Units
FreqMax[1][2]	Frequency (All PIO)	load: 40 pF		25	MHz
		load: 20 pF		30	MHz
PulseminH[1][2]	High Level Pulse Width (All PIO)	load: 40 pF	20		ns
		load: 20 pF	10		ns
PulseminL[1][2]	Low Level Pulse Width (All PIO)	load: 40 pF	20		ns
		load: 20 pF	10		ns

Table 8-10: PIO Characteristics

8.4.3.2 SPI Parameters

Table 8-11 and Figure 8-2 display the SPI parameters.

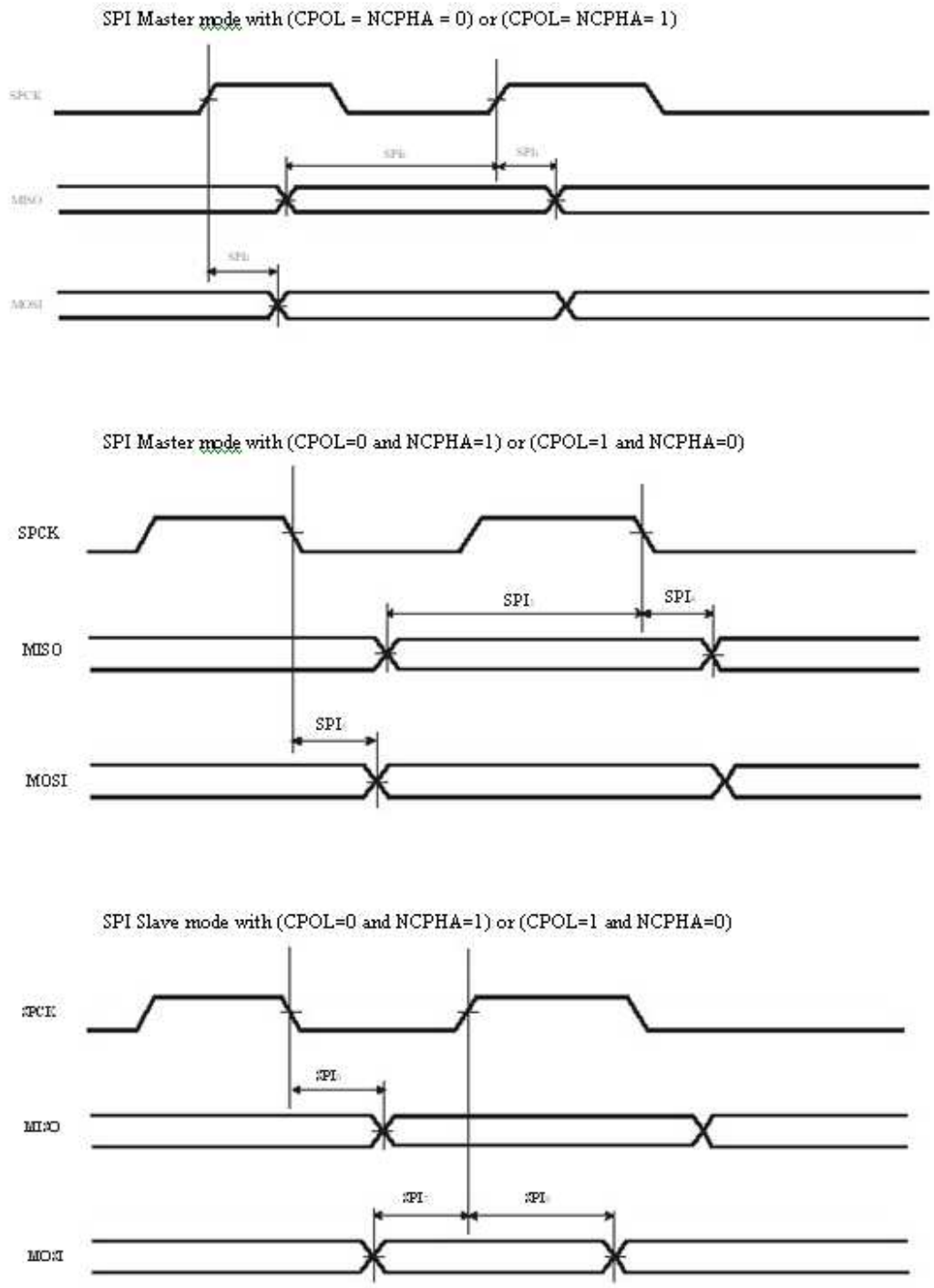


Figure 8-2: SPI Parameters

SPI Timings

Symbol	Parameter	Conditions	Min	Max	Units
SPI0	MISO Setup time before SPCK rises (master)	3.3V domain(1)		28.5	ns
SPI1	MISO Hold time after SPCK rises (master)	3.3V domain(1)	0		ns
SPI2	SPCK rising to MOSI Delay (master)	3.3V domain(1)		2	ns
SPI3	MISO Setup time before SPCK falls (master)	3.3V domain(1)		26.5	ns
SPI4	MISO Hold time after SPCK falls (master)	3.3V domain(1)	0		ns
SPI5	SPCK falling to MOSI Delay (master)	3.3V domain(1)		2	ns
SPI6	SPCK falling to MISO Delay (slave)	3.3V domain(1)		28	ns
SPI7	MOSI Setup time before SPCK rises (slave)	3.3V domain(1)	2		ns
SPI8	MOSI Hold time after SPCK rises (slave)	3.3V domain(1)	3		ns
SPI9	SPCK rising to MISO Delay (slave)	3.3V domain(1)		28	ns
SPI10	MOSI Setup time before SPCK falls (slave)	3.3V domain(1)	3		ns
SPI11	MOSI Hold time after SPCK falls (slave)	3.3V domain(1)	3		ns

Notes: 1. 3.3V domain: V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40 pF.

Table 8-11: SPI Parameters

8.4.3.3 EMAC Characterization

Table 8-12 and Figure 8-3 display the EMAC characterization.

EMAC Signals

Symbol	Parameter	Conditions	Min (ns)	Max (ns)
EMAC1	Setup for EMDIO from EMDC rising	Load: 20pF(2)		2
EMAC2	Hold for EMDIO from EMDC rising	Load: 20pF(2)		((1/f)-19) + 4(1)
EMAC3	EMDIO toggling from EMDC rising	Load: 20pF(2)		4.5

Notes: 1. f: MCK frequency (MHz)
2. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 20 pF

EMAC MII Specific Signals

Symbol	Parameter	Conditions	Min (ns)	Max (ns)
EMAC4	Setup for ECOL from ETXCK rising	Load: 20pF(1)	0	
EMAC5	Hold for ECOL from ETXCK rising	Load: 20pF(1)	2	
EMAC6	Setup for ECRS from ETXCK rising	Load: 20pF(1)	1.5	
EMAC7	Hold for ECRS from ETXCK rising	Load: 20pF(1)	2	
EMAC8	ETXER toggling from ETXCK rising	Load: 20pF(1)		25
EMAC9	ETXEN toggling from ETXCK rising	Load: 20pF(1)		25
EMAC10	ETX toggling from ETXCK rising	Load: 20pF(1)		25
EMAC11	Setup for ERX from ERXCK	Load: 20pF(1)	0	
EMAC12	Hold for ERX from ERXCK	Load: 20pF(1)	4	
EMAC13	Setup for ERXER from ERXCK	Load: 20pF(1)	0	
EMAC14	Hold for ERXER from ERXCK	Load: 20pF(1)	4	
EMAC15	Setup for ERXDV from ERXCK	Load: 20pF(1)	2	
EMAC16	Hold for ERXDV from ERXCK	Load: 20pF(1)	2	

Note: 1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 20 pF

Table 8-12: EMAC Characterization

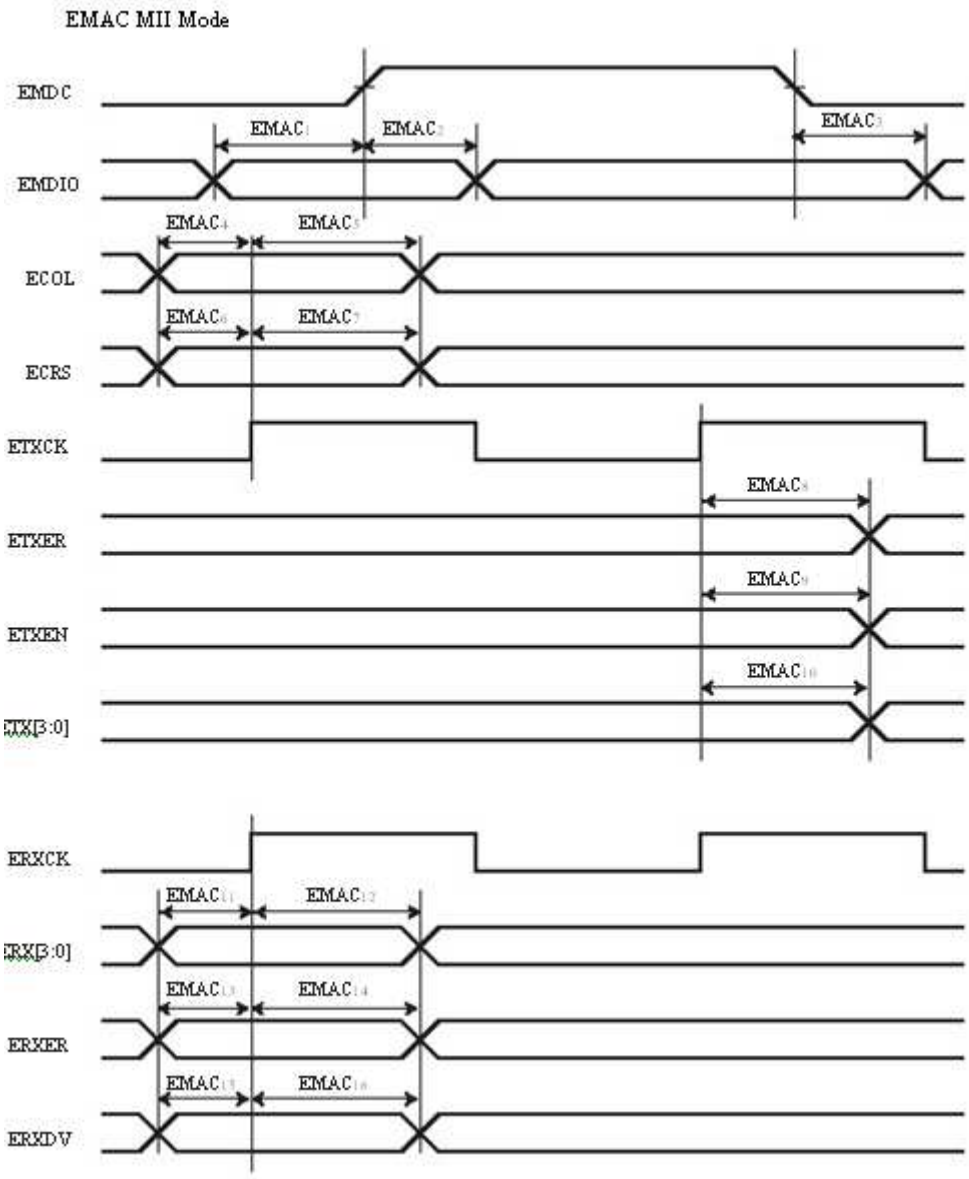


Figure 8-3: EMAC Characterization

8.4.3.4 JTAG/ICE Timings

Figure 8-4 and Table 8-13 display the ICE timings.

ICE Interface Timing Specification

Symbol	Parameter	Conditions	Min	Max	Units
ICE0	TCK Low Half-period	(1)	51		ns
ICE1	TCK High Half-period	(1)	51		ns
ICE2	TCK Period	(1)	102		ns
ICE3	TDI, TMS, Setup before TCK High	(1)	0		ns
ICE4	TDI, TMS, Hold after TCK High	(1)	3		ns
ICE5	TDO Hold Time	(1)	13		ns
ICE6	TCK Low to TDO Valid	(1)		20	ns

Note: 1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF

Table 8-13: ICE Timings

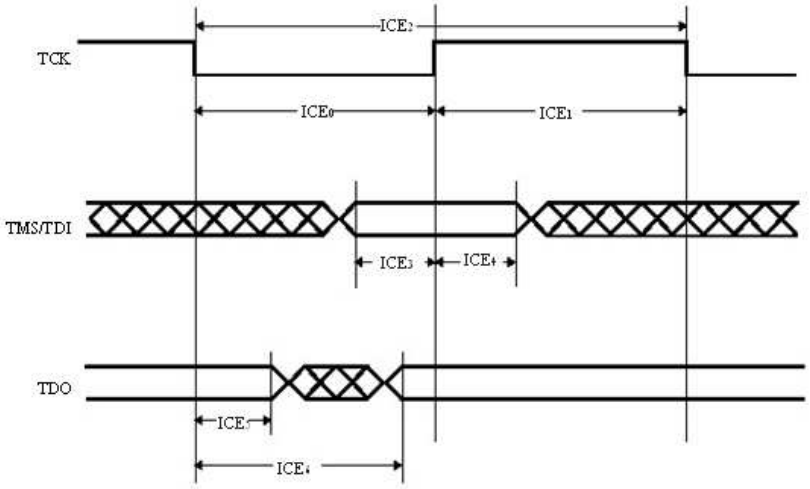


Figure 8-4: ICE Timings

Table 8-14 and Figure 8-5 display the JTAG timings.

JTAG Interface Timing specification

Symbol	Parameter	Conditions	Min	Max	Units
JTAG0	TCK Low Half-period	(1)	6.5		ns
JTAG1	TCK High Half-period	(1)	5.5		ns
JTAG2	TCK Period	(1)	12		ns
JTAG3	TDI, TMS Setup before TCK High	(1)	2		ns
JTAG4	TDI, TMS Hold after TCK High	(1)	3		ns
JTAG5	TDO Hold Time	(1)	4		ns
JTAG6	TCK Low to TDO Valid	(1)		16	ns
JTAG7	Device Inputs Setup Time	(1)	0		ns
JTAG8	Device Inputs Hold Time	(1)	3		ns
JTAG9	Device Outputs Hold Time	(1)	6		ns
JTAG10	TCK to Device Outputs Valid	(1)		18	ns

Note: 1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF

Table 8-14: JTAG Timings

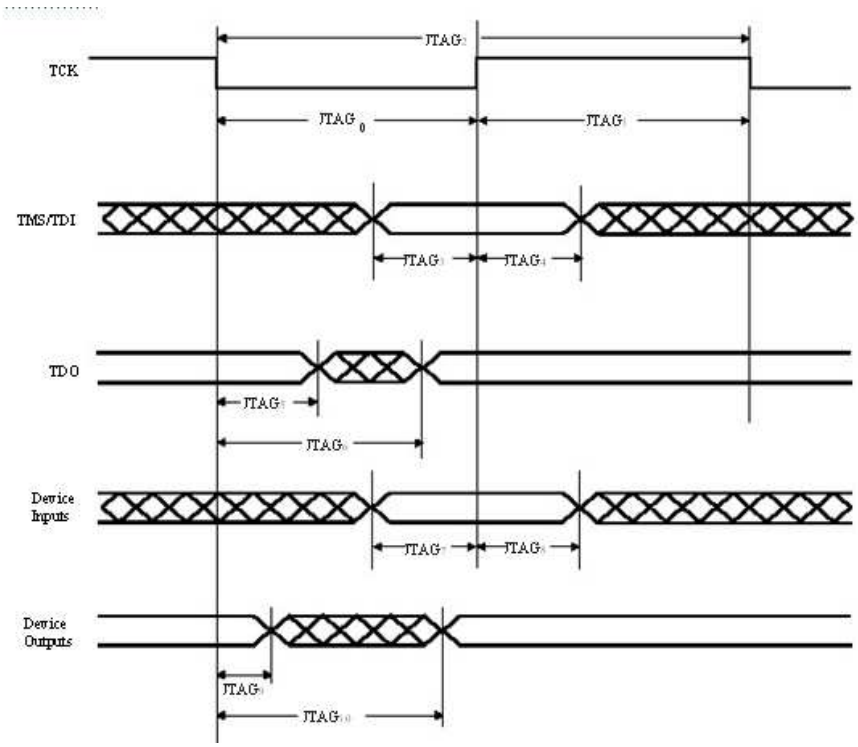


Figure 8-5: JTAG Timings

8.4.3.5 ADC Timing Characteristics

Figure 8-6 displays the ADC timing characteristics.

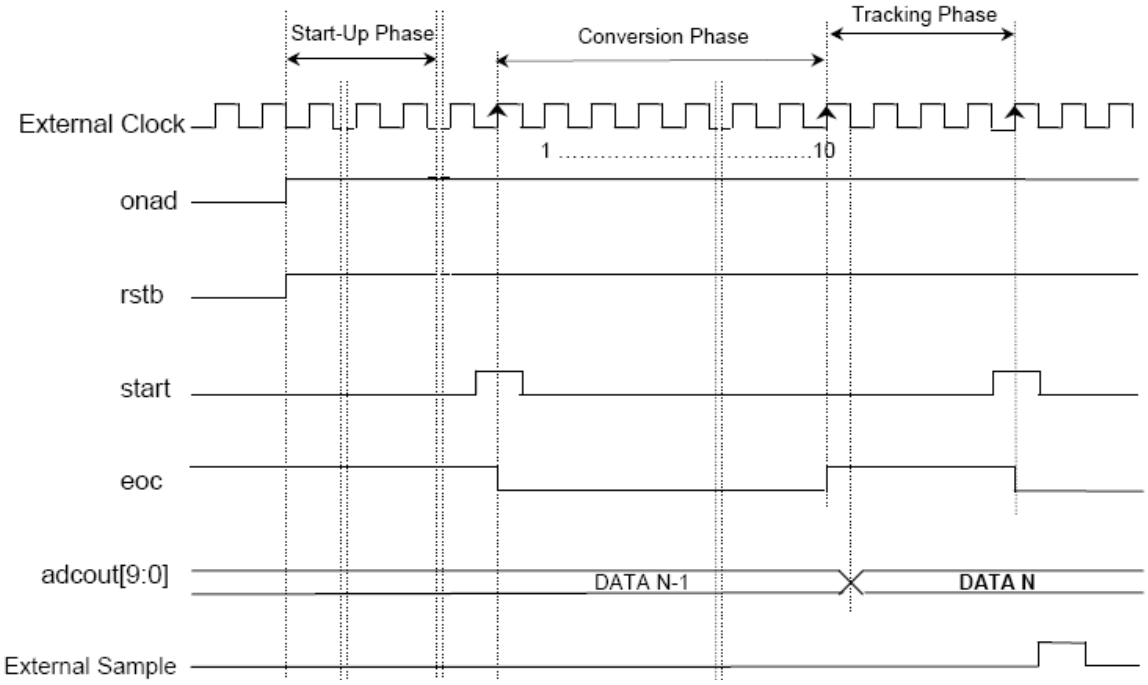


Figure 8-6: ADC Timing Characteristics

8.4.3.6 HPI Parameters

Figure 8-7 and Table 8-15 display the HPI parameters.

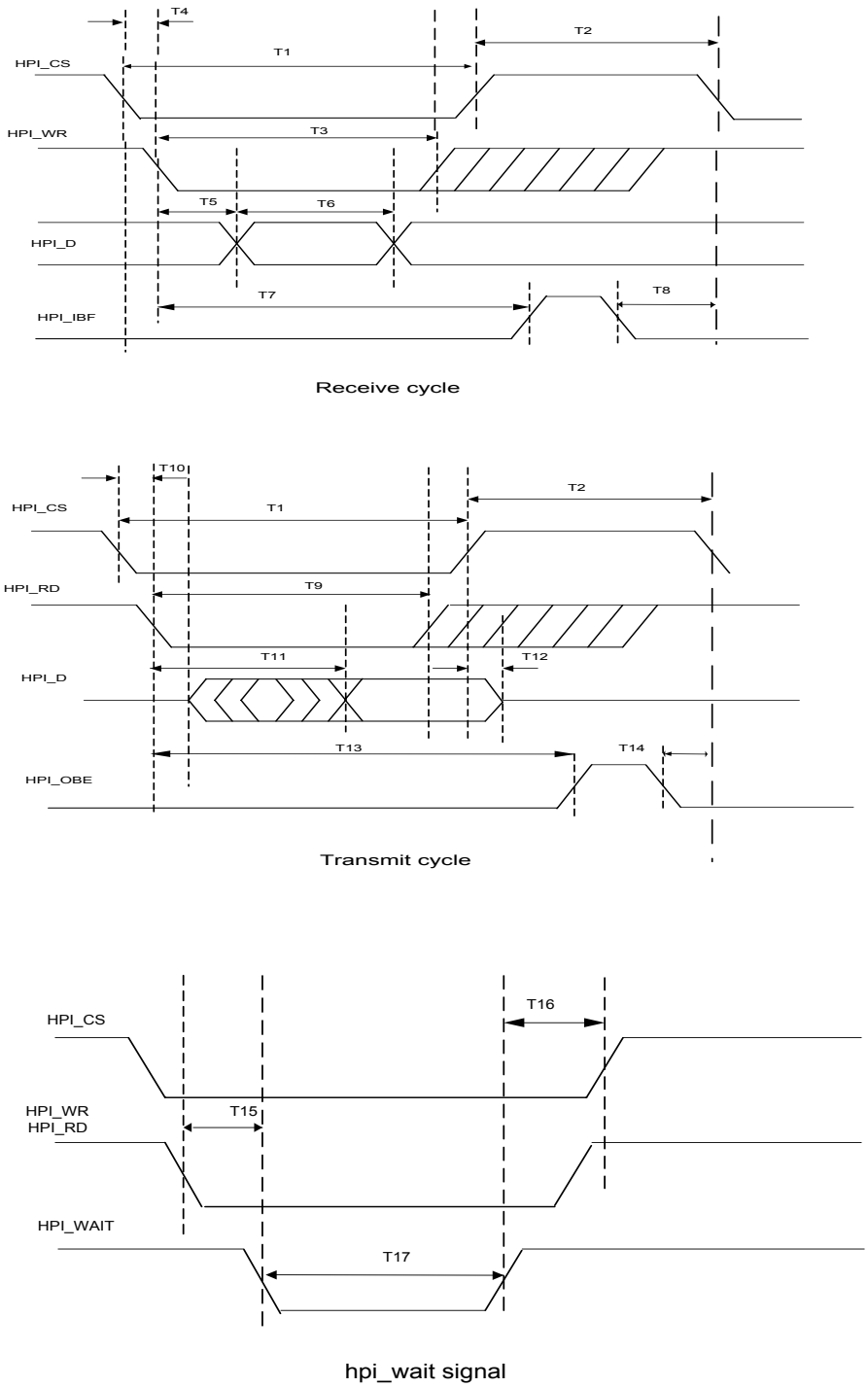


Figure 8-7: HPI Parameters

Symbol	Parameter	Min	Max	Units
T1	HPI_CS low time	60		ns
T2	HPI_CS high time	30		ns
T3	HPI_WR low time	60		ns
T4	HPI_WR falling after HPI_CS falling	0		ns
T5	HPI_D valid after HPI_WR falling		10	ns
T6	HPI_D stable	30		ns
T7	HPI_IBF rising after HPI_WR falling		80	ns
T8	HPI_CS falling after HPI_IBF falling	0		ns
T9	HPI_RD low time	60		ns
T10	HPI_RD falling after HPI_CS falling	0		ns
T11	HPI_D stable after HPI_RD falling		50	ns
T12	HPI_D hold time after CS rising	3		ns
T13	HPI_OBE rising after HPI_WR falling		80	ns
T14	HPI_CS falling after HPI_OBE falling	0		ns
T15	HPI_WAIT falling after HPI_RD or HPI_WR falling	10		ns
T16	HPI_CS rising after HPI_WAIT rising	0		ns
T17	HPI_WAIT low time	85	170	ns

Table 8-15: HPI Parameters

9 Recommended Soldering Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3°C/sec. max.	3°C/sec. max.
Preheat - Min. Temperature (Ts_{min}) - Max. Temperature (Ts_{max}) - Time (ts_{min} to ts_{max})	 100°C 150°C 60-120 sec.	 150°C 200°C 60-180 sec.
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60-150 sec.	 217°C 60-150 sec.
Peak/Classification Temperature (Tp)	See Table 9-2	See Table 9-3
Time within 5°C of actual Peak Temperature (tp)	10-30 sec.	20-40 sec.
Ramp-Down Rate	6°C/sec. max.	6°C/sec. max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package, measured on the package body surface.

Table 9-1: Classification Reflow Profiles

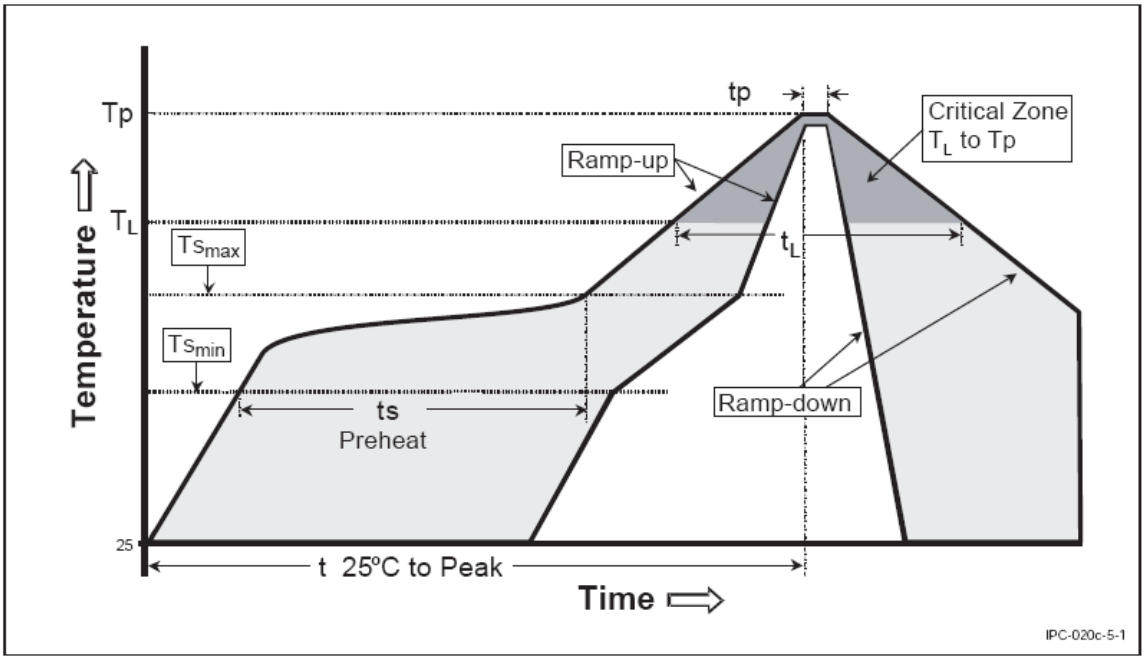


Figure 9-1: Classification Reflow Profile

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 9-2: SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C	260 +0°C	260 +0°C
1.6 mm – 2.5 mm	260 +0°C	250 +0°C	245 +0°C
≥2.5 mm	250 +0°C	245 +0°C	245 +0°C

Table 9-3: Pb-Free Process – Package Classification Reflow Temperatures

10 Ordering Information

Part Number	Description
CO2144-48LI-3	iChip CO2144
CO2144-48LI-3(SP)	iChip CO2144 Sample Package (2 chips)
CO2128-48LI-3	iChip CO2128
CO2128-48LI-3(SP)	iChip CO2128 Sample Package (2 chips)
II-EVB-630-3-110	Evaluation board for the CO2128, 110V
II-EVB-630-3-220	Evaluation board for the CO2128, 220V
CO2064-48LI-3	iChip CO2064
CO2064-48LI-3(SP)	iChip CO2064 Sample Package (2 chips)
II-EVB-600-3-110	Evaluation board for the CO2064, 110V
II-EVB-600-3-220	Evaluation board for the CO2064, 220V

11 Internet Protocol Compliance

iChip complies with the Internet standards listed in Table 11-1.

RFC 768	User datagram protocol (UDP)
RFC 791	Internet protocol (IP)
RFC 792	ICMP – Internet control message protocol
RFC 793	Transmission control protocol (TCP)
RFC 821	Simple mail transfer protocol (SMTP)
RFC 822	Standard for the format of ARPA Internet text messages
RFC 826	Ethernet address resolution protocol (ARP)
RFC 959	File transfer protocol (FTP)
RFC 854	TELNET protocol specification
RFC 857	TELNET ECHO option
RFC 858	TELNET suppress go-ahead option
RFC 1034	Domain names (DNS) - concepts and facilities
RFC 1035	Domain names (DNS) - implementation and specification
RFC 1073	TELNET window size option
RFC 1091	TELNET terminal type option
RFC 1321	MD5 message digest algorithm
RFC 1331	Point-to-point protocol (PPP)
RFC 1332	PPP Internet protocol control protocol (IPCP)
RFC 1334	PPP authentication protocol (PAP)
RFC 1570	PPP LCP extensions
RFC 1661	Point-to-point protocol (PPP)
RFC 1877	PPP IPCP extensions for name server addresses
RFC 1939	Post office protocol - version 3 (POP3)
RFC 1957	Some observations on the implementations of the post office protocol (POP3)
RFC 1994	PPP challenge handshake authentication protocol (CHAP)
RFC 2030	Simple network time protocol (SNTP)
RFC 2045	Multipurpose Internet mail extensions (MIME) part one: internet message body format
RFC 2046	MIME part two: media types
RFC 2047	MIME part three: message header extensions for non-ASCII text
RFC 2048	MIME part four: registration procedures
RFC 2049	MIME part five: conformance criteria and examples
RFC 2068	Hypertext transfer protocol HTTP/1.1
RFC 2131	Dynamic host configuration protocol (DHCP)
RFC 2132	DHCP options (only relevant parts)

RFC 2228	FTP security extensions
RFC 2246	The TLS protocol version 1.0

Table 11-1: Internet Protocol Compliance

12 List of Terms and Acronyms

AT+i™	Connect One's Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
Base64	Encoding scheme that converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
CHAP	Challenge Authentication Protocol. Extends the PAP procedure by introducing advanced elements of security.
DNS	Domain Name System. Defines the structure of Internet names and their association with IP addresses.
FTP	File Transfer Protocol. Used to provide file and directory services for remote server file systems.
iChip™	Connect One's Internet controller for embedded Internet connectivity.
iChipSec™	Connect One's Internet controller for embedded secure Internet connectivity.
ICMP	Internet Control Message Protocol. Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
IP	Internet Protocol. Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
IPCP	Internet Protocol Control Protocol. Establishes and configures the Internet protocol over PPP. Also negotiates Van Jacobson TCP/IP header compression with PPP.
ISP	Internet Service Provider. Commercial company that provides Internet access to end (mostly PC) users through a dialup connection.
LCP	Link Control Protocol. Negotiates data link characteristics and tests the integrity of the link.
"Leave on Server"	An option designating whether retrieved email messages are to be left intact on the server for subsequent downloads or are to be deleted from the server after a successful download.
MIME	Multipurpose Internet Mail Extensions. Extends the format of mail message bodies to allow multi-part textual and non-textual data to be represented and exchanged between Internet mail servers.
PAP	Password Authentication Protocol. Used optionally by the PPP protocol to identify the user to the ISP.
Ping	ICMP protocol ECHO message and its reply. Often used to debug IP networks and to test the accessibility of a network device.

POP3	Post Office Protocol Version 3. Allows a workstation/PC to dynamically retrieve mail from a mailbox kept on a remote server.
PPP	Point-to-Point Protocol. Communications protocol used to send data across serial communication links, such as modems.
RFC	Request For Comments. Collections of standards that define the way remote computers communicate over the Internet.
SMTP	Simple Mail Transfer Protocol. Provides for transferring mail reliably and efficiently over the Internet.
SNTP	Simple Network Time Protocol. Used to retrieve accurate time of day from a networked time server. The accurate UTC/GMT time is retrieved.
SSL3	Secure Socket Layer Version 3. Protocol that uses RSA public-key exchange to establish an encrypted secure socket.
TCP	Transmission Control Protocol. Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.
Telnet	Network Terminal Protocol. Provides remote terminal connectivity, enabling you to execute tasks on a remote application server.
TLS1	Transport Layer Security Version 1. Supersedes the SSL3 protocol.