

Normally – OFF Silicon Carbide Junction Transistor

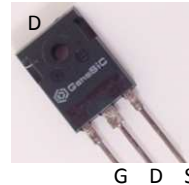
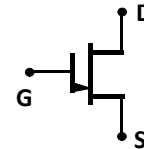
V_{DS}	=	1200 V
$V_{DS(ON)}$	=	1.4 V
I_D	=	20 A
$R_{DS(ON)}$	=	70 mΩ

Features

- 175 °C maximum operating temperature
- Temperature independent switching performance
- Gate oxide free SiC switch
- Suitable for connecting an anti-parallel diode
- Positive temperature coefficient for easy paralleling
- Low gate charge
- Low intrinsic capacitance

Package

- RoHS Compliant


TO-247AB


Advantages

- Low switching losses
- Higher efficiency
- High temperature operation
- High short circuit withstand capability

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Maximum Ratings unless otherwise specified

Parameter	Symbol	Conditions	Values	Unit
Drain – Source Voltage	V_{DS}	$V_{GS} = 0 V$	1200	V
Continuous Drain Current	I_D	$T_{C,MAX} = 95 °C$	20	A
Gate Peak Current	I_{GM}		10	A
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 175 °C, I_G = 1 A,$ Clamped Inductive Load	$I_{D,max} = 20$ @ $V_{DS} \leq V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 175 °C, I_G = 1 A, V_{DS} = 800 V,$ Non Repetitive	20	μs
Reverse Gate – Source Voltage	V_{SG}		30	V
Reverse Drain – Source Voltage	V_{SD}		25	V
Power Dissipation	P_{tot}	$T_C = 95 °C$	151	W
Storage Temperature	T_{stg}		-55 to 175	$°C$

Electrical Characteristics at $T_j = 175 °C$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
On Characteristics						
Drain – Source On Voltage	$V_{DS(ON)}$	$I_D = 20 A, I_G = 400 mA, T_j = 25 °C$	1.4			V
		$I_D = 20 A, I_G = 800 mA, T_j = 125 °C$	1.6			
		$I_D = 20 A, I_G = 1600 mA, T_j = 175 °C$	2.2			
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 20 A, I_G = 400 mA, T_j = 25 °C$	70			mΩ
		$I_D = 20 A, I_G = 800 mA, T_j = 125 °C$	80			
		$I_D = 20 A, I_G = 1600 mA, T_j = 175 °C$	110			
Gate Forward Voltage	$V_{GS(FWD)}$	$I_G = 500 mA, T_j = 25 °C$	3.3			V
		$I_G = 500 mA, T_j = 175 °C$	3.1			
DC Current Gain	β	$V_{DS} = 5 V, I_D = 20 A, T_j = 25 °C$	TBD			
		$V_{DS} = 5 V, I_D = 20 A, T_j = 175 °C$	TBD			
Off Characteristics						
Drain Leakage Current	I_{DSS}	$V_R = 1200 V, V_{GS} = 0 V, T_j = 25 °C$	1.1			μA
		$V_R = 1200 V, V_{GS} = 0 V, T_j = 125 °C$	1.6			
		$V_R = 1200 V, V_{GS} = 0 V, T_j = 175 °C$	2.1			
Gate Leakage Current	I_{SG}	$V_{SG} = 20 V, T_j = 25 °C$	20			nA

Electrical Characteristics at $T_j = 175\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit	
			min.	typ.	max.		
Capacitance Characteristics							
Gate-Source Capacitance	C_{GS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		tbd		pF	
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_D = 1\text{ V}, f = 1\text{ MHz}$		tbd		pF	
Reverse Transfer/Output Capacitance	C_{RSS}/C_{OSS}	$V_D = 1\text{ V}, f = 1\text{ MHz}$		tbd		pF	
Switching Characteristics							
Turn On Delay Time	$t_{d(on)}$	$V_{DD} = 800\text{ V}, I_D = 20\text{ A},$ $R_{G(on)} = R_{G(off)} = 44\ \Omega,$ $V_{GS} = -8/15\text{ V}, L = 1.1\text{ mH},$ FWD = GB40SLT12, $T_j = 25\text{ }^\circ\text{C}$ Refer to Figure 15 for gate current waveform		tbd		ns	
Rise Time	t_r			tbd		ns	
Turn Off Delay Time	$t_{d(off)}$			tbd		ns	
Fall Time	t_f			tbd		ns	
Turn-On Energy Per Pulse	E_{on}			tbd		μJ	
Turn-Off Energy Per Pulse	E_{off}			tbd		μJ	
Total Switching Energy	E_{ts}			tbd		μJ	
Turn On Delay Time	$t_{d(on)}$		$V_{DD} = 800\text{ V}, I_D = 20\text{ A},$ $R_{G(on)} = R_{G(off)} = 44\ \Omega,$ $V_{GS} = -8/15\text{ V}, L = 1.1\text{ mH},$ FWD = GB40SLT12, $T_j = 175\text{ }^\circ\text{C}$ Refer to Figure 15 for gate current waveform		tbd		ns
Rise Time	t_r				tbd		ns
Turn Off Delay Time	$t_{d(off)}$				tbd		ns
Fall Time	t_f			tbd		ns	
Turn-On Energy Per Pulse	E_{on}			tbd		μJ	
Turn-Off Energy Per Pulse	E_{off}			tbd		μJ	
Total Switching Energy	E_{ts}			tbd		μJ	
Thermal Characteristics							
Thermal resistance, junction - case	R_{thJC}			0.53		$^\circ\text{C/W}$	

Figures

TBD

TBD

Figure 1: Typical Output Characteristics at 25 °C

Figure 2: Typical Output Characteristics at 125 °C

TBD

Figure 3: Typical Output Characteristics at 175 °C

TBD

Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

TBD

Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

TBD

Figure 6: Typical Blocking Characteristics

TBD

Figure 7: Capacitance Characteristics

TBD

Figure 8: Capacitance Characteristics

TBD

Figure 9: Typical Hard-switched Turn On Waveforms

TBD

Figure 10: Typical Hard-switched Turn Off Waveforms

TBD

Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

TBD

Figure 13: Typical Turn On Energy Losses vs. Drain Current

TBD

Figure 14: Typical Turn Off Energy Losses vs. Drain Current

TBD

Figure 15: Typical Gate Current Waveform

TBD

Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency¹

TBD

Figure 17: Power Derating Curve

TBD

Figure 18: Forward Bias Safe Operating Area

TBD

Figure 19: Turn-Off Safe Operating Area

TBD

Figure 20: Transient Thermal Impedance

¹ – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

Gate Drive Technique (Option #1)

To drive the GA20JT12-247 with the lowest gate drive losses, please refer to the dual voltage source gate drive configuration described in Application Note AN-10B (<http://www.genesicsemi.com/index.php/references/notes>).

Gate Drive Technique (Option #2)

The GA20JT12-247 can be effectively driven using the IXYS IXDN614 / IXDD614 non-inverting gate driver IC or a comparable product. A typical gate driver configuration along with component values using this driver is offered below. Additional information is available in GeneSiC Application Note AN-10A and from the manufacturer at www.ixys.com.

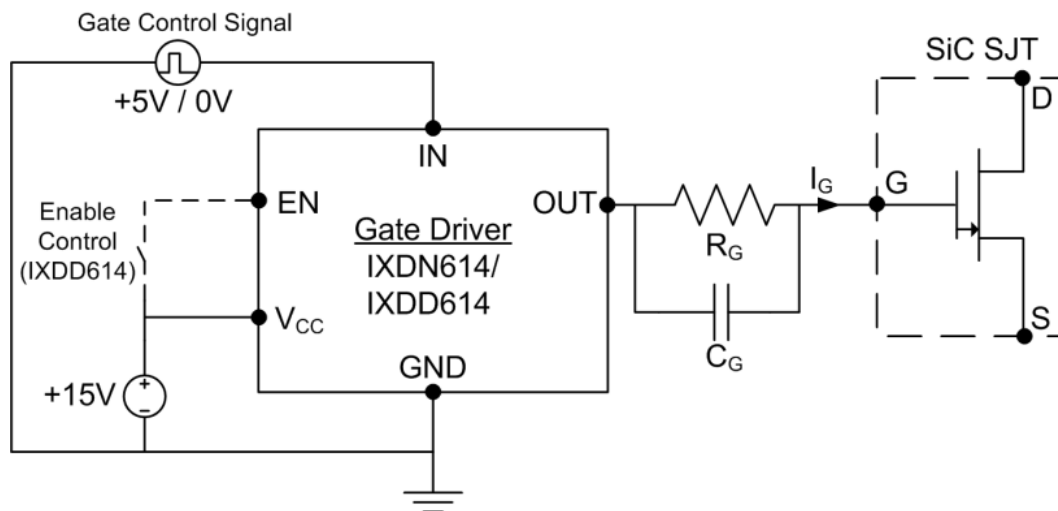
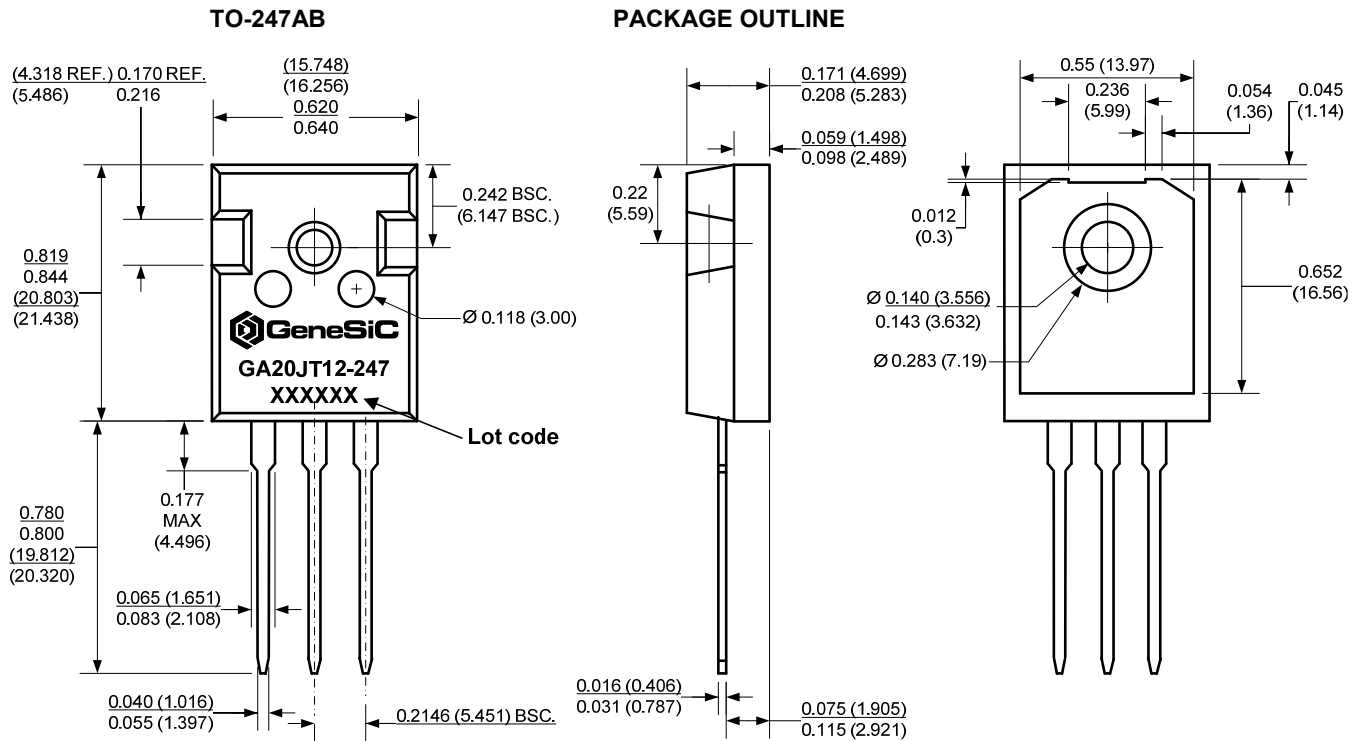


Figure 21: Recommended Gate Driver Configuration (Option #2)

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Option #2 Gate Drive Conditions (IXDD614/IXDN614)						
Supply Voltage	V_{CC}		-0.3	15	40	V
Gate Control Input Signal, Low	IN		-5.0	0	0.8	V
Gate Control Input Signal, High	IN		3.0	5.0	$V_{CC}+0.3$	V
Enable, Low	EN	IXDD614 Only			$1/3 * V_{CC}$	V
Enable, High	EN	IXDD614 Only	$2/3 * V_{CC}$			V
Output Voltage, Low	V_{OUT}				0.025	V
Output Voltage, High	V_{OUT}		$V_{CC}-0.025$			V
Output Current, Peak	I_{OUT}	Package Limited		tbd	14	A
Output Current, Continuous	I_{OUT}			tbd	4.0	A
Passive Gate Components						
Gate Resistance	R_G	$I_G \approx 0.5$ A	5	tbd		Ω
Gate Capacitance	C_G	$I_G \approx 0.5$ A		tbd		nF

Package Dimensions:

NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2013/09/12	0	Initial release	

Published by
 GeneSiC Semiconductor, Inc.
 43670 Trade Center Place Suite 155
 Dulles, VA 20166

GeneSiC Semiconductor, Inc. reserves right to make changes to the product specifications and data in this document without notice.

GeneSiC disclaims all and any warranty and liability arising out of use or application of any product. No license, express or implied to any intellectual property rights is granted by this document.

Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

SPICE Model Parameters

Copy the following code into a SPICE software program for simulation of the GA20JT12 SJT device.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   1.0           $
*      $Date:      26-AUG-2013   $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*      http://www.genesicsemi.com/index.php/sic-products/sjt
*
*      COPYRIGHT (C) 2013 GeneSiC Semiconductor Inc.
*      ALL RIGHTS RESERVED
*
*      These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
*      OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model GA20JT12 NPN
+ IS      5.00E-47
+ ISE     1.26E-28
+ EG      3.2
+ BF      100
+ BR      0.55
+ IKF     700
+ NF      1
+ NE      2
+ RB      0.26
+ RC      0.055
+ CJC     6.98E-10
+ VJC     3
+ MJC     0.5
+ CJE     2.22E-9
+ VJE     3
+ MJE     0.5
+ XTI     3
+ XTB     -1.2
+ TRC1    7.00E-3
+ VCEO    1200
+ ICRATING 20
+ MFG      GeneSiC_Semiconductor
*
*      End of GA20JT12 SPICE Model
```