swissbit®

Product data sheet

Industrial MultiMedia Card M-100 Series

MMCA 3.31, 4.1, and 4.2 compliant

Extended and industrial temperature grade

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Multimedia card (MMC)

1 Feature summary

- Custom-designed, highly-integrated memory controller
  - Fully compliant with MMC Card specification 3.31, 4.1, and 4.2
  - Four integrated 4KByte Sector Buffers for fast data transfer
- Standard MMC form factor
  - 32.0mm x 24.0mm x 1.4mm
- 2.7...3.6V normal operating voltage
- Low-power CMOS technology
- Performance
  - 1 bit MMC or SPI data transfer
  - MMC and SPI burst up to 52Mbit/s (6.5MB/s)
- Patented power-off reliability
  - No data loss of older sectors
  - Max. 16 sectors data loss (old data kept)
  - All data were written to the flash, if the card is ready after the last write command
- Wear Leveling: equal wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Write Endurance: Due to intelligent wear leveling an even use of the entire flash is guaranteed, regardless how much "static" (OS) data is stored.
- Data Retention: 10 year (JEDEC)
- High reliability
  - Designed for embedded market
  - MTBF > 4,000,000 hours
  - Number of card insertions/removals: >10,000
  - Extended Temperature range -25° up to 90°C
  - Industrial Temperature range available -40° up to 90°C (optional)
- Hot swappable
- Life Time Monitoring over special vendor command set
- Controlled BOM
- Life Cycle Management

2 Order Information

2.1 Extended Temperature range -25°C to +90°C

Table 1: Product list

Density	Part Number
128MB	SFMM0128O1BN1NX-E-M0-1x1-STD
128MB	SFMM0128O1BN1SA-E-M0-1x1-STD

2.2 Industrial Temperature range -40°C to +90°C

Table 2: Industrial Product List

Density	Part Number
128MB	SFMM0128O1BN1NX-I-M0-1x1-STD
128MB	SFMM0128O1BN1SA-I-M0-1x1-STD

x will define the latest FW

2.3 Offered options for customer projects

- Customer specified strings and IDs (OID, PNM, PRV)
- Customer specified capacities
- Preload service
- Customized labels
- Option for special FW like:
  - write protection with password (on request)
  - SMART-like read out current bad blocks and wear level distribution for life time estimation
  - Smaller capacities with higher random write speed
  - Single sector erase commands (MMC Spec 2.11 compatible)

Contents

3 Product Specification

The MMC is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The Card operates in two basic modes:

- **1-bit MMC card mode**
- **SPI mode**

The MMC also supports MMC **High Speed mode** with up to 52MHz clock frequency.
The cards are compliant with

- MMCA Specification Rev. 3.31, 4.1, 4.2
- On request special Firmware compatible with MMCA specification 2.11

The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware RS-code **Error Correction Code (ECC), defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware RS-code ECC allows to detect and correct **4 symbols per 528 Bytes**.

The Card has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The power consumption is very low.

The cards are offered in 2 temperature ranges

- Extended -25°C ...90°C
- Industrial -40°C ...90°C on request

The cards are RoHS compliant and lead-free.

3.1 System Performance

Table 3: Performance

System Performance		Typ.	Max.	Unit
Burst Data transfer Rate (max clock 52MHz)			6.5	MB/s
Sustained Sequential Read (NX Flash)	128MB	5.5 (1)	5.7 (2)	
Sustained Sequential Write (NX Flash)	128MB	5.4 (1)	5.9 (2)	
Single Sector Random Read (NX Flash)	128MB	0.67(1)		
Single Sector Random Write (NX Flash)	128MB	0.024(1)		
Sustained Sequential Read (SA Flash)	128MB	5.5 (1)	5.7 (2)	
Sustained Sequential Write (SA Flash)	128MB	5.4 (1)	5.9 (2)	
Single Sector Random Read (SA Flash)	128MB	0.66(1)		
Single Sector Random Write (SA Flash)	128MB	0.027(1)		

1. The speed was measured with an Sandisk USB-SD/MMC card reader Mobile Mate with a interface speed of 50MHz in 1-bit MMC mode, cycle time 20ns, write/read file sequential 128 sectors per transfer or random 1 sector per command Sustained Speed depends on burst speed, flash type, and number, and file size.
2. Measured with Testmetrix Compliance tester (1-Bit, 50MHz)

3.2 Environmental Specifications

3.2.1 Recommended Operating Conditions

Table 4: MMC Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Extended Operating Temperature	-25	25	90	°C
Industrial Operating Temperature	-40	25	90	°C
Power Supply VCC (3.3V)	2.7	3.3	3.6	V

Table 5: Current consumption

Current Consumption (type)	typ	max	Unit
Write (MMC mode)	15	20	mA
Read (MMC mode)	9	15	
Idle Mode (MMC mode)	0.1	0.2	

3.2.2 Recommended Storage Conditions

Table 6: MMC Recommended Storage Conditions

Parameter	Min	Typ	Max	Unit
Commercial Storage Temperature	-40	25	90	°C
Industrial Storage Temperature	-40	25	100	°C

3.2.3 Humidity & ESD

Table 7: Humidity & ESD

Parameter	Operating	Non Operating
Humidity (non-condensing)	max 95%	
ESD according to IEC61000-4-2 Human body model ±4 kV 100 pf/1.5 kOhm Machine model ±0.25 kV 200 pf/0 Ohm	**Non Contact Pads area:** ±8 kV (coupling plane discharge) ±8 kV (air discharge) Human body model according to IEC61000-4-2	**Contact Pads:** ±4 kV, Human body model according to IEC61000-4-2

3.2.4 Durability

Table 8:Durability

Parameter	Operating	Non Operating
Salt water spray	3% NaCl/35°C; 24h acc. MIL STD Method 1009	
Impermeability	IP67	
UV Light Exposure	UV: 254nm, 15Ws/cm2	
Insertions	>10,000	
Drop test	1.5m free fall	
Bending	10N	
Torque	0.15Nm or ±2.5deg	
Bump	25g; 6ms; ±3 x 4000 shocks	
Shock	1000 g max.	
Vibration (peak -to-peak)	15G max.	

3.3 Physical Dimensions

Table 9: Physical Dimensions

Physical Dimensions	Value	Unit
Length	32.00±0.1	mm
Width	24.00±0.1	
Thickness	1.40±0.1	
Weight (typ.)	2	g

3.4 Reliability

Table 10: Reliability

Parameter	Value
Data Retention	10 years (according JEDEC)

4 Capacity specification

Table 11: MMC capacity specification

Capacity	Sectors_card	Total addressable capacity (Byte)
128MB	244,224	125,042,688

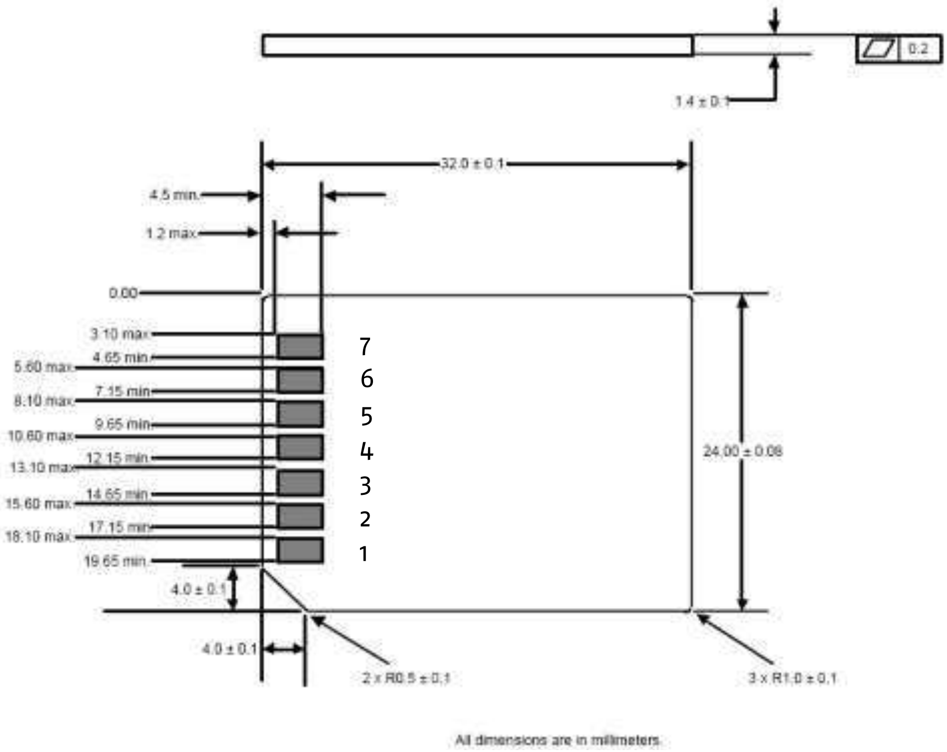
5 Card physical

5.1 Physical description

The MMC contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).
Fehler! Verweisquelle konnte nicht gefunden werden. shows the MMC housing. The rectangular region around the contact is filled with the PCB.

Figure 1 shows general card dimensions and contact positions.
The MMC dimension is defined according the MMCA (JEDEC) Specification.

Figure 1: Mechanical Dimensions of card and contacts



6 Electrical interface

6.1 Electrical description

Table 12: MMC Memory Card Pad Assignment

Pin #	MMC Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	Not used[3]	I	Not used in 1-bit MMC mode	CS	I[2]	Chip Select (neg true)
2	CMD	I/O/PP/OD	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line	DO	O/PP	Data Out

Notes:

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) At power up this line has a pull up resistor (about 50kOhm) enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select MMC mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high.
3) Must be open or high at the first CMD0 for selection MMC mode. If it is low, SPI mode is selected (see 7.1.3)

6.2 DC characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 13: DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Peak Voltage on all Lines	-0.3		VDD+0.3	V	
VIL	Input LOW Voltage	-0.3		0.25*VDD	V	
VIH	Input HIGH Voltage	0.625*VDD		VDD+0.3	V	
VOL	Output LOW Voltage			0.125*VDD	V	at 100µA
VOH	Output HIGH Voltage	0.75*VDD			V	at -100µA
VOL (OD)	Output LOW Voltage, open drain			0.3	V	at 2mA
VOH (OD)	Output HIGH Voltage, open drain	VDD-0.2			V	at -100µA
IDD	Operating Current		8	15	mA	
	Pre-initialization Standby Current			3	mA	
	Post-initialization Standby Current		100	200	µA	
ILI	Input Leakage Current before init	-100		100	µA	without pull-up R
	Input Leakage Current	-10		10	µA	
ILO	Output Leakage Current before init	-100		100	µA	
	Output Leakage Current	-10		10	µA	

Table 14: MMC Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	2.7		3.6	V
VSS1 VSS2	Supply Voltage Differentials	-0.5		0.5	V
-	Power Up Time (from 0V to VDD min)			250	ms

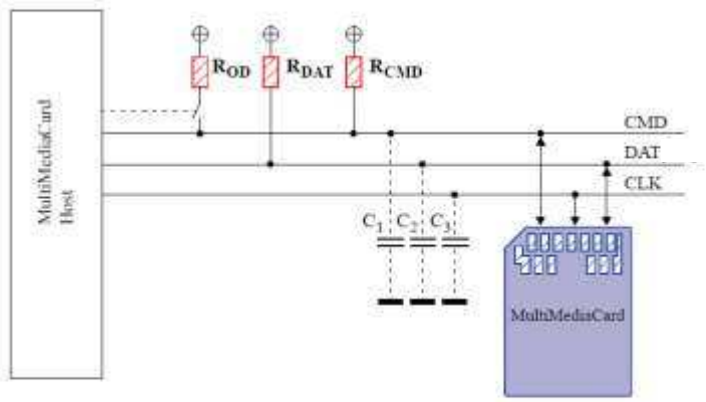
6.3 Signal Loading

The total capacitance C_L is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS}, and the capacitance C_{CARD} of the card connected to the line:
$C_L = C_{HOST} + C_{BUS} + C_{CARD}$
To allow the sum of the host and bus capacitances to be up to 20pF for the card, the following conditions in the table below are met by the card.

Table 15: Signal loading

Parameter	Symbol	Min	Max	Unit	Notes
Pull up resistance	R_{CMD}	4.7	100	kOhm	To prevent bus floating
Pull up resistance	R_{DAT}	50	100	kOhm	To prevent bus floating
Bus signal line capacitance	C_L		30	pF	Single card
Signal card capacitance	C_{card}		7	pF	
Signal line inductance			16	nH	f≤52MHz

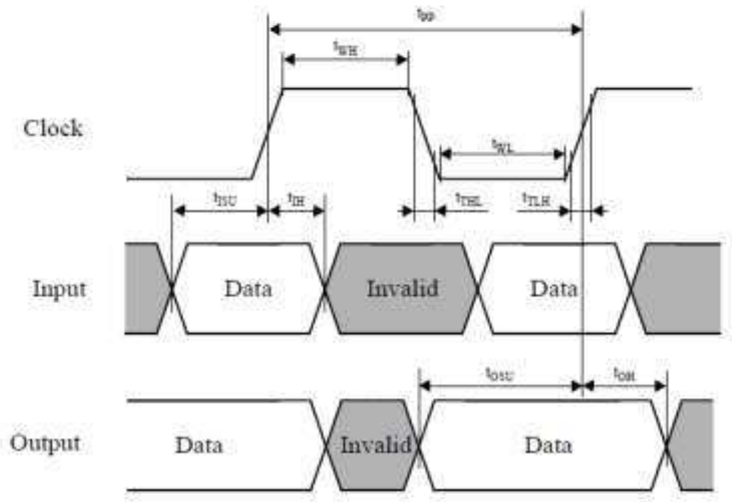
Figure 2: Bus circuitry diagram



The ROD is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the ROD. RDAT and RCMD are pull-up resistors protecting the CMD and the DAT lines against bus floating when no card is inserted or when all card drivers are in a high-impedance mode. A constant current source can replace the ROD by achieving a better performance (constant slopes for the signal rising and falling edges).
If the host does not allow the switchable ROD implementation, a fixed RCMD can be used (the minimum value is defined in Table 15). Consequently the maximum operating frequency in the open drain mode has to be reduced if the used RCMD value is higher than the minimal one given in Table 15.

6.4 AC characteristics

Figure 3: Timing diagram data input/output



Data must always be sampled on the rising edge of the clock.

Table 16: Card interface timing 26/52MHz

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode (2)	fPP	0	26/52	MHz	CL≤30pF, Tolerance +100kHz
Clock frequency in card identification mode	f0D	0	400	kHz	CL≤30pF, Tolerance +20kHz
Clock low time	tWL	6.5		ns	CL≤30pF
Clock rise time (3)	tTLH		3	ns	
Clock fall time (3)	tTHL		3	ns	
CMD, DAT input setup time	tISU	3		ns	
CMD, DAT input hold time	tIH	3		ns	
CMD, DAT output setup time	t0SU	5		ns	
CMD, DAT output hold time	t0H	5		ns	
Signal rise time (3)	trise		3	ns	
Signal fall time (3)	tfall		3	ns	

Notes

1. All timing values are measured relative to 50% of voltage level
2. The card supports the full frequency range 0-52MHz
3. Rise and fall times are measured from 10% to 90% of voltage level.

Table 17: Card interface timing 20MHz

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode	fPP	0	20	MHz	CL≤30pF
Clock frequency in card identification mode	f0D	0	400	kHz	CL≤30pF, Tolerance +20kHz
Clock low time	tWL	10		ns	CL≤30pF
Clock rise time	tTLH		10	ns	
Clock fall time	tTHL		10	ns	
CMD, DAT input setup time	tISU	3		ns	
CMD, DAT input hold time	tIH	3		ns	
CMD, DAT output setup time	t0SU	13.1		ns	
CMD, DAT output hold time	t0H	9.7		ns	

Notes

1. All timing values are measured relative to 50% of voltage level
2. Rise and fall times are measured from 10% to 90% of voltage level.

7 Host access Specification

The following chapters summarize how the host accesses the card:

- Chapter 7.1 summarizes the MMC and SPI buses.
- Chapter 7.2 summarizes the registers.
- Chapter 7.3 summarizes the supported commands.

7.1 MMC and SPI Bus Modes

The card supports MMC and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The MMC mode uses a 1-bit data transfer with bidirectional CMD and DAT line, and the SPI mode a Data-In (CMD-line) and Data-Out (DAT-line).

7.1.1 MMC Bus Mode Protocol

The MMC Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the MMC Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width of 1 bit (DAT)
Communication over the MMC bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the DAT line.

The MMC bus signals are listed in Table 18:

Table 18: MMC Bus Signals

Signal	Description
CLK	Host to card clock signal
CMD	Bidirectional Command/Response signal
DAT	Bidirectional data signal
Vdd, Vss	Power and Ground

7.1.2 SPI Bus Mode Protocol

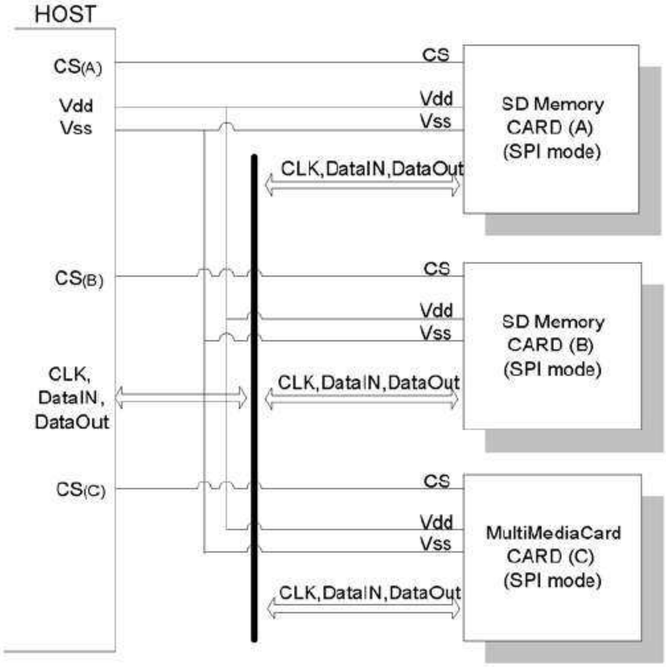
The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the MMC channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed Table 19 and the SPI bus topology is illustrated in Figure 4.

Table 19: SPI Bus Signals

Signal	Description
CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

Figure 4: SPI bus topology



7.1.3 Mode Selection

The MMC Card wakes up in the MMC mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle_state*. If the card recognizes that the MMC mode is required it will not respond to the command and remain in the MMC mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the MMC mode is by entering the power cycle. In SPI mode the MMC protocol state machine is not observed. All the MMC commands supported in SPI mode are always available.
During the initialization sequence of an MMC card host, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is MultiMediaCard. In that case it should re-start the card as MMC using CMD0 and CMD1.

7.2 Card Registers

The MMC has five registers. Refer to Table 20 to Table 25 for detail.

Table 20: MMC registers

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
RCA	16	Relative Card Address	This register carries the card address in MMC mode.
Ext_CSD	512	Card specific information	This register defines the card properties and selected modes.

Table 21: CID register

CID = fb00004f 31424e31 2001xxxx xxxxmyss

Register Name	Bit Width	Description	typ. value
MID	8	Manufacture ID	0xFB
OID	16	OEM/Application ID	0x0000
PNM	48	Product Name	e.g. "01BN1 " 0x4F 31 42 4E 31 20 *)
PRV	8	Product Version	e.g. 0x01 *)
PSN	32	Product Serial Number	xxxxxxxx
MDT	8	Manufacture Date	0xmy (y=c→2009)
CRC	7	Check sum of CID contents	chksm
–	1	Not used; always=1	1

*) Can be changed in future

Table 22: OCR register

OCR = 00ff8000

OCR bit position	VDD voltage window	typ. value	OCR bit position	VDD voltage window	typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24-30	Reserved	
13	2.5-2.6	0	31		0=busy; 1=ready *1)
14	2.6-2.7	0			

Notes

1. This bit is set to LOW if the card has not finished the power up routine.

Table 23: CSD register according MMC Spec 4.2

CSD = 9026002a 1f5980ee 76db7ce0 9640002d

Register Name	Bit Width	Description	Initial Value
CSD_STRUCTURE	2	CSD structure	10
SPEC_VERS	4	System specification version	0100
–	2	Reserved	00
TAAC	8	Data read access time 1	00100110
NSAC	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	8	Data transfer rate 0x2A	00101010
CCC	12	Card command classes	000111110101
READ_BL_LEN	4	Read data block length	1001
READ_BL_PARTIAL	1	Partial blocks for read allowed	1
WRITE_BLK_MISALIGN	1	Write block misalignment	0
READ_BLK_MISALIGN	1	Read block misalignment	0
DSR_IMP	1	DSR implemented	0
–	2	Reserved	00
C_SIZE	12	Device size	0x3B9
VDD_R_CURR_MIN	3	VDD min read current	110
VDD_R_CURR_MAX	3	VDD max read current	110
VDD_W_CURR_MIN	3	VDD min write current	110
VDD_W_CURR_MAX	3	VDD max write current	110
C_SIZE_MULT	3	Device size multiplier	110
SECTOR_SIZE	5	Erase sector size	11111
ERASE_GRP_SIZE	5	Erase group size	00111
WP_GRP_SIZE	5	Write protect group size	00000
WP_GRP_ENABLE	1	Write protect group enable	1
DEFAULT_ECC	2	Manufcaturer default ECC	00
R2W_FACTOR	3	Write speed factor	101
WRITE_BL_LEN	4	Write data block length	1001
WRITE_BL_PARTIAL	1	Partial blocks for write allowed	0
–	4	Reserved	0000
CONTENT_PROT_APP	1	Content protection application	0
FILE_FORMAT_GRP	1	File format group	0 W(1)
COPY	1	Copy flag	0 W(1)
PERM_WRITE_PROTECT	1	Permanent write protection	0 W(1)
TMP_WRITE_PROTECT	1	Temporary write protection	0 W
FILE_FORMAT	2	File format	00 W(1)
ECC	2	ECC code	00 W
CRC	7	Checksum of CSD contents	0010110 W
–	1	Always=1	1

W / W(1)value can be changed (ONCE) with CMD27 (PROGRAM_CSD)
checksum is calculated automatically by the card

Table 24: RCA register

Field	Bit Width	typ Value
RCA	16	0x0000*)

***) After Initialization the host can change the RCA register.**

Table 25: Extended CSD register according MMC Spec 4.2

Register Name	Field	Byte Width	Bytes	Cell Type	Initial Value
Properties Segment					
Reserved		7	[511:505]		0
Supported Command Sets	S_CMD_SET	1	[504]	R	0
Reserved		288	[503:216		0
Sector Count	SEC_COUNT	4	[215:212]	R	244224
Reserved		1	[211		0
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	[210]	R	0x0f
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	[209]	R	0x0f
Minimum Write Performance for 8bit @26MHz/ 4bit @52MHz	MIN_PERF_W_8_26_4_52	1	[208]	R	0x0f
Minimum Read Performance for 8bit @26MHz/ 4bit @52MHz	MIN_PERF_R_8_26_4_52	1	[207]	R	0x0f
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	[206]	R	0x0f
Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	[205]	R	0x0f
Reserved		1	[204]		0
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	[203]	R	0
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	[202]	R	0
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	[201]	R	0
Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	[200]	R	0
Reserved		3	[199:197]		0
Card Type	CARD_TYPE	1	[196]	R	3
Reserved		1	[195]		0
CSD Structure Version	CSD_STRUCTURE	1	[194]	R	3
Reserved		1	[193]		0
Extended CSD Revision	EXT_CSD_REV	1	[192]	R	0
Modes Segment					
Command Set	CMD_SET	1	[191]	R/W	0
Reserved		1	[190]		0
Command Set Revision	CMD_SET_REV	1	[189]	RO	0
Reserved		1	[188]		0
Power Class	POWER_CLASS	1	[187]	R/W	0
Reserved		1	[186]		0
High Speed Interface Timing	HS_TIMING	1	[185]	R/W	0 or 1
Reserved		1	[184]		0
Bus Width Mode	BUS_WIDTH	1	[183]	WO	0
Reserved		1	[182]		0
Erased Memory Content	ERASED_MEM_CONT	1	[181]	RO	0
Reserved		181	[180:0]		0

7.3 Supported commands

Following commands were supported with the standard Firmware in MMC and SPI mode:

Table 26: Supported commands

Nr.	Command	MMC	SPI
CMD 0	GO_IDLE_STATE	Yes	Yes
CMD 1	SEND_OP_COND	Yes	Yes
CMD 2	ALL_SEND_CID	Yes	---
CMD 3	SET_RELATIVE_ADDR	Yes	---
CMD 4	SET_DSR	NOP*	---
CMD 5	Reserved	---	---
CMD 6	SWITCH	Yes	Yes
CMD 7	SELECT_CARD	Yes	---
CMD 8	SEND EXT CSD	Yes	Yes
CMD 9	SEND_CSD	Yes	Yes
CMD 10	SEND_CID	Yes	Yes
CMD 11	READ_DAT_UNTIL_STOP	---	---
CMD 12	STOP_TRANSMISSION	Yes	Yes
CMD 13	SEND_STATUS	Yes	Yes
CMD 14	BUSTEST_R	Yes	---
CMD 15	GO_INACTIVE_STATE	Yes	---
CMD 16	SET_BLOCKLEN	Yes	Yes
CMD 17	READ_SINGLE_BLOCK	Yes	Yes
CMD 18	READ_MULTIPLE_BLOCK	Yes	Yes
CMD 19	BUSTEST_W	Yes	---
CMD 20	WRITE_DATA_UNTIL_STOP	---	---
CMD 21	Reserved	---	---
CMD 22	Reserved	---	---
CMD 23	SET_BLOCK_COUNT	Yes	Yes
CMD 24	WRITE_SINGLE_BLOCK	Yes	Yes
CMD 25	WRITE_MULTIPLE_BLOCK	Yes	Yes
CMD 26	PROGRAMM_CID	Yes	---
CMD 27	PROGRAMM_CSD	Yes	Yes
CMD 28	SET_WRITE_PROT	Yes	Yes
CMD 29	CLR_WRITE_PROT	Yes	Yes
CMD 30	SEND_WRITE_PROT	Yes	Yes
CMD 31	Reserved	---	---
CMD 32	TAG_SECTOR_START	---	---
CMD 33	TAG_SECTOR_END	---	---

Nr.	Command	MMC	SPI
CMD 34	UNTAG_SECTOR	---	---
CMD 35	ERASE_GROUP_START	Yes	Yes
CMD 36	ERASE_GROUP_END	Yes	Yes
CMD 37	UNTAG_ERASE_GROUP	---	---
CMD 38	ERASE	Yes	Yes
CMD 39	FAST_IO	---	---
CMD 40	GO_IRQ_STATE	---	---
CMD 41	Reserved	---	---
CMD 42	LOCK_UNLOCK	Yes	Yes
CMD 43	Reserved	---	---
CMD 44	Reserved	---	---
CMD 45	Reserved	---	---
CMD 46	Reserved	---	---
CMD 47	Reserved	---	---
CMD 48	Reserved	---	---
CMD 49	Reserved	---	---
CMD 50	Reserved	---	---
CMD 51	Reserved	---	---
CMD 52	Reserved	---	---
CMD 53	Reserved	---	---
CMD 54	Reserved	---	---
CMD 55	APP_CMD	NOP*	NOP*
CMD 56	GEN_CMD	Yes	Yes
CMD 57	Reserved	---	---
CMD 58	READ_OCR	---	Yes
CMD 59	CRC_ON_OFF	---	Yes
CMD 60	Reserved for manufacturer	Mfktr	Mfktr
CMD 61	Reserved for manufacturer	---	---
CMD 62	Reserved for manufacturer	---	---
CMD 63	Reserved for manufacturer	---	---

* Command 4 is a no-operation command because the card has no DSR register
* Command 55 is a no-operation command, because no APP commands are defined.

swissbit®

8 Declaration of Conformity

Product Type: Multimedia Card

Brand Name: SWISSMEMORY™ MMC

Model Designation: SFMMxxxx0xxxxxx-x-xx-xxx-xxx

Manufacturer: Swissbit AG
Industriestrasse 4
CH-9552 Bronschhofen
Switzerland

The product complies with the requirements of the following directives:

EN55022 :2006 +A1:2007 Class B
FCC47 Part15 Subpart B
EN61000-4-2 :2001
EN61000-4-3 :2006
EN61000-6-2 :2005

following the provisions of directive

Electromagnetic compatibility 2004/108/EC

The product was tested according all EMC requirements necessary for CE-mark

Year of the first marking: 2009

Silvio Muschter
Vice President
Engineering & Development

Bronschhofen, 17 June 2011

9 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that CompactFlash Cards must comply with both Directives in order for them to be sold on the European market:

- RoHS – Restriction of Hazardous Substances
- WEEE – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2002/96/EC)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space. «In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty»
(WEEE Directive 2002/96/EC)

When does the WEEE Directive take effect?

The Directive came into effect internationally on 13 August, 2005.

What is RoHS (2002/95/EC)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**

- **Checking the components and raw materials:**
  - Replacing non-RoHS-compliant components and raw materials in the supply chain
  - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit

- **Modifying the manufacturing processes and procedures**
  - Successfully adapting and optimizing the new management-free integration process in the supply chain
  - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials

- **Carrying out the quality process**
  - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of 1 July, 2006, only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

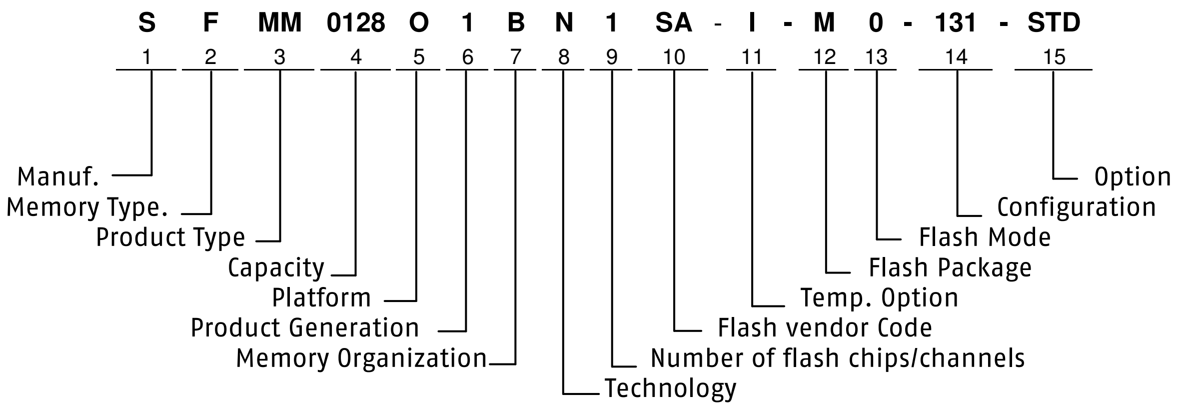
Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

Contact details:
Swissbit AG
Industriestrasse 4
CH 9552 Bronschhofen
Tel: +41 71 913 03 03 – Fax: +41 71 913 03 15
E-mail: info@swissbit.com – Website: www.swissbit.com

10 Part Number Decoder



1. Manufacturer

Swissbit code	S

2. Memory Type

Flash	F

3. Product Type

Multi media card (MMC)	MM

4. Capacity

128 MB	0128

5. Platform

MMC	O

6. Generation

1st Generation	1

7. Memory Organization

x8	B

8. Technology

MMC controller	M-100	N

9. Channels

1 Flash Channel	1

10. Flash Code

Numonyx	NX
Samsung	SA

11. Temperature Option

Industrial Temp. Range -40°C – 90°C	I
Extended Temp. Range -25°C – 90°C	E

12. DIE Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q

13. PIN Mode

Normal nCE & R/nB	0
Dual nCE & Dual R/nB	1

14. Configuration XYZ

X→ Configuration

default	1

Y → FW Revision

1st Revision	1
2nd Revision	2
3rd Revision	3

Z → optional

optional	1

15. Option

Swissbit / Standard	STD

11 Swissbit Label specification

11.1 Front side label

128MB MMC

11.2 Back side lasering

SWISSBIT	
SFMM012801BN1	Part-
SA-E-M0-131-STD	number
1009-60035328	Date-Lot Code

12 Revision History

Table 27: Document Revision History

Date	Revision	Revision Details
11-Dec-2009	1.00	First final release
28-Mar-2011	1.10	Retention specification according JEDEC
22-June-2011	1.20	New Product added with Samsung NAND Flash, updated product picture
31-August-2011	1.30	Idle current 0.1mA