

# 8GB DDR3 – SDRAM ECC SO-DIMM

## 204 Pin ECC SO-UDIMM

## SGN08G72G1BB2SA-xx(E/W)RT

## 8GByte in FBGA Technology

## RoHS compliant

### Options:

- |                             |                   |               |
|-----------------------------|-------------------|---------------|
| ▪ Data Rate / Latency       |                   | Marking       |
| DDR3 1333 MT/s CL9          |                   | -CC           |
| DDR3 1600 MT/s CL11         |                   | -DC           |
| ▪ Module density            |                   |               |
| 8GB with 18 dies and 2 rank |                   |               |
| ▪ Standard Grade            | (T <sub>A</sub> ) | 0°C to 70°C   |
|                             | (T <sub>C</sub> ) | 0°C to 85°C   |
| ▪ Grade E                   | (T <sub>A</sub> ) | 0°C to 85°C   |
|                             | (T <sub>C</sub> ) | 0°C to 95°C   |
| ▪ Grade W                   | (T <sub>A</sub> ) | -40°C to 85°C |
|                             | (T <sub>C</sub> ) | -40°C to 95°C |

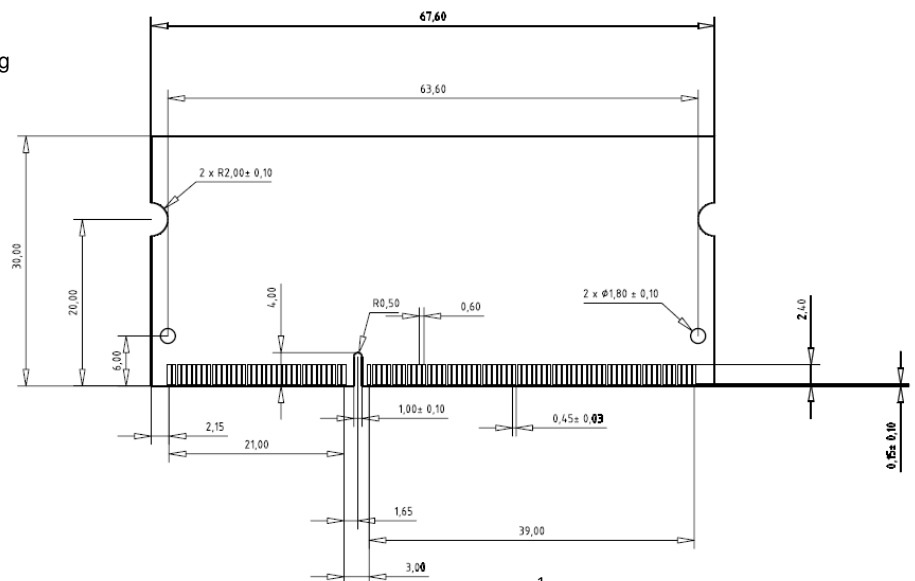
### Environmental Requirements:

- Operating temperature (ambient)
  - Standard Grade 0°C to 70°C
  - E-Grade 0°C to 85°C
  - W-Grade -40°C to 85°C
- Operating Humidity 10% to 90% relative humidity, noncondensing
- Operating Pressure 105 to 69 kPa (up to 10000 ft.)
- Storage Temperature -55°C to 100°C
- Storage Humidity 5% to 95% relative humidity, noncondensing
- Storage Pressure 1682 PSI (up to 5000 ft.) at 50°C

### Features:

- 204-pin 72-bit DDR3 Small Outline, Dual-In-Line Double Data Rate synchronous DRAM Module
- Module organization: dual rank 1024M x 72
- V<sub>DD</sub> = 1.5V ±0.075V, V<sub>DDQ</sub> 1.5V ±0.075V
- 1.5V I/O ( SSTL\_15 compatible)
- Fly-by-bus with termination for C/A & CLK bus
- On-board I<sup>2</sup>C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC EP3-12800 DDR3 SDRAM 72bit-SO-DIMM design spec. and JEDEC- Standard MO-268. (see [www.jedec.org](http://www.jedec.org))
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- DDR3 - SDRAM component Samsung K4B4G0846B**
- 512Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit prefetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh, Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.

Figure: mechanical dimensions<sup>1</sup>



<sup>1</sup> If no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 204-pin 8-byte DDR3 SDRAM ECC Small Outline Dual-In-line Memory Module (SO-UDIMM) which is organized as x72 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL\_15 compatible.

The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I<sup>2</sup>C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-UDIMM manufacturer (Swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

### Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
1G x 72bit	18 x 512M x 8bit (4Gbit)	16	BA0, BA1, BA2	10	8k	S0#, S1#

### Module Dimensions

in mm

67.60 (long) x 30(high) x 3.80 [max] (thickness)

### Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SGN08G72G1BB2SA-CC[E/W]RT	8 GByte	10.6 GB/s	1.5ns / 1333MT/s	9-9-9
SGN08G72G1BB2SA-DC[E/W]RT	8 GByte	12.8 GB/s	1.25ns / 1600MT/s	11-11-11

### Pin Name

A0-9, A11 – A15	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
CB0 – CB07	ECC check bits
DM0-DM8	Input Data Mask
DQS0 – DQS8	Data Strobe, positive line
DQS0# - DQS8#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
S0#, S1#	Chip Select
CK0 – CK1	Clock Inputs, positive line
CK0# - CK1#	Clock Inputs, negative line

Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
V <sub>DD</sub>	Supply Voltage (1.5V± 0.075V)
V <sub>REFDQ</sub>	Reference voltage: DQ, DM (V <sub>DD</sub> /2)
V <sub>REFCA</sub>	Reference voltage: Control, command, and address (V <sub>DD</sub> /2)
V <sub>SS</sub>	Ground
V <sub>TT</sub>	Termination voltage: Used for control, command, and address (V <sub>DD</sub> /2).
V <sub>DDSPD</sub>	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

**Pin Configuration**

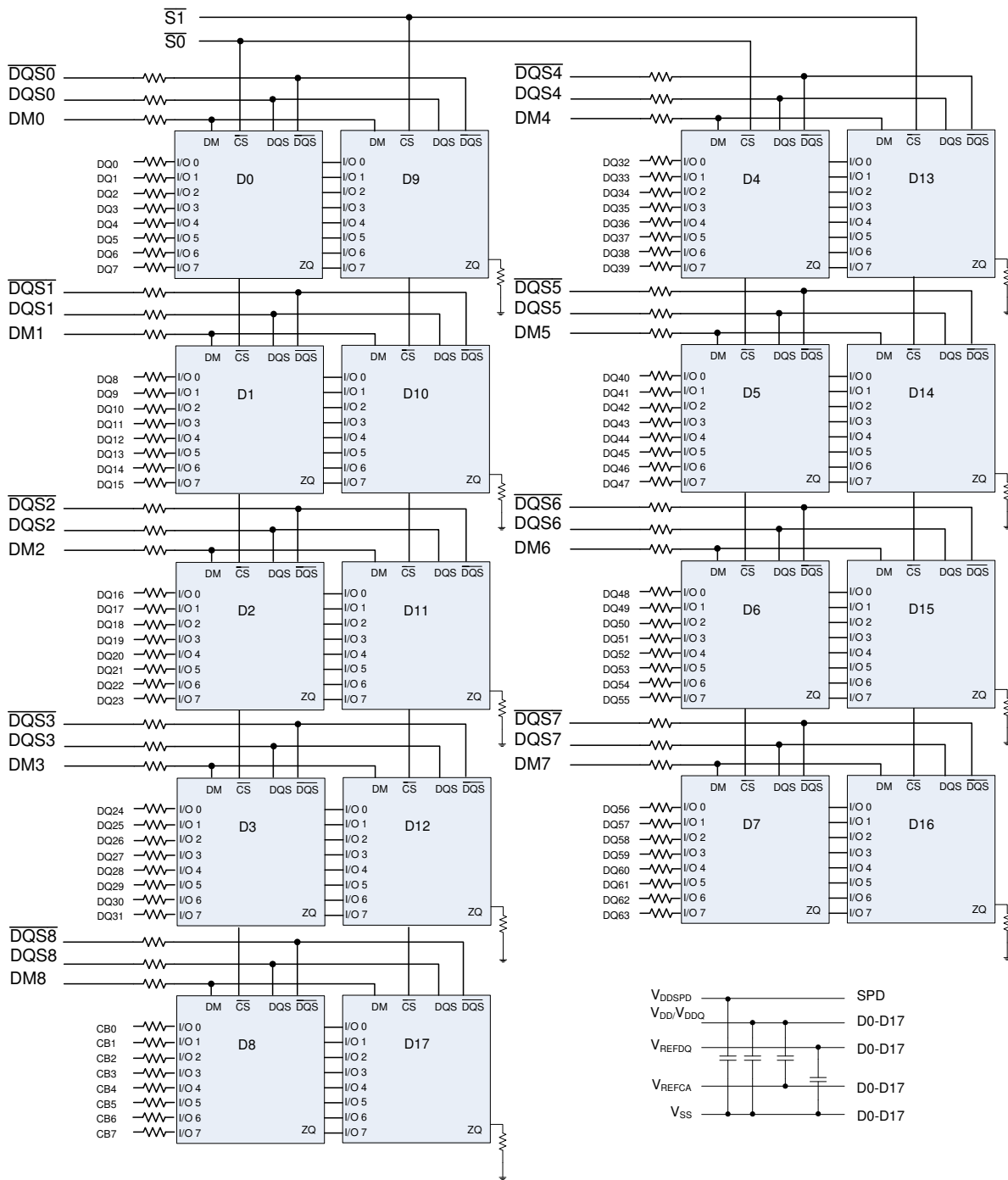
Frontside							
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	V <sub>REFDQ</sub>	53	V <sub>SS</sub>	103	A3	155	V <sub>SS</sub>
3	V <sub>SS</sub>	55	DQ24	105	A1	157	DM5
5	DQ0	57	DQ25	107	A0	159	DQ42
7	DQ1	59	DM3	109	V <sub>DD</sub>	161	DQ43
9	V <sub>SS</sub>	61	V <sub>SS</sub>	111	CK0	163	V <sub>SS</sub>
11	DM0	63	DQ26	113	CK0#	165	DQ48
13	DQ2	65	DQ27	115	V <sub>DD</sub>	167	DQ49
15	DQ3	67	V <sub>SS</sub>	117	A10/AP	169	V <sub>SS</sub>
17	V <sub>SS</sub>	69	CB0	119	BA0	171	DQS6#
19	DQ8	71	CB1	121	WE#	173	DQS6
21	DQ9	Key		123	V <sub>DD</sub>	175	V <sub>SS</sub>
23	V <sub>SS</sub>	73	V <sub>SS</sub>	125	CAS#	177	DQ50
25	DQS1#	75	DQS8#	127	S0#	179	DQ51
27	DQS1	77	DQS8	129	S1#	181	V <sub>SS</sub>
29	V <sub>SS</sub>	79	V <sub>SS</sub>	131	V <sub>DD</sub>	183	DQ56
31	DQ10	81	CB2	133	DQ32	185	DQ57
33	DQ11	83	CB3	135	DQ33	187	V <sub>SS</sub>
35	V <sub>SS</sub>	85	V <sub>DD</sub>	137	V <sub>SS</sub>	189	DM7
37	DQ16	87	CKE0	139	DQS4#	191	DQ58
39	DQ17	89	CKE1	141	DQS4	193	DQ59
41	V <sub>SS</sub>	91	BA2	143	V <sub>SS</sub>	195	V <sub>SS</sub>
43	DQS2#	93	V <sub>DD</sub>	145	DQ34	197	SA0
45	DQS2	95	A12/BC#	147	DQ35	199	V <sub>DDSPD</sub>
47	V <sub>SS</sub>	97	A8	149	V <sub>SS</sub>	201	SA1
49	DQ18	99	A5	151	DQ40	203	V <sub>TT</sub>
51	DQ19	101	V <sub>DD</sub>	153	DQ41		

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

Backside							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	V <sub>SS</sub>	54	DQ28	104	A4	156	DQS5
4	DQ4	56	DQ29	106	A2	158	V <sub>SS</sub>
6	DQ5	58	V <sub>SS</sub>	108	BA1	160	DQ46
8	V <sub>SS</sub>	60	DQS3#	110	V <sub>DD</sub>	162	DQ47
10	DQS0#	62	DQS3	112	CK1	164	V <sub>SS</sub>
12	DQS0	64	V <sub>SS</sub>	114	CK1#	166	DQ52
14	V <sub>SS</sub>	66	DQ30	116	V <sub>DD</sub>	168	DQ53
16	DQ6	68	DQ31	118	NC(S3#)	170	V <sub>SS</sub>
18	DQ7	70	V <sub>SS</sub>	120	NC(S2#)	172	DM6
20	V <sub>SS</sub>	72	CB4	122	RAS#	174	DQ54
22	DQ12	Key		124	V <sub>DD</sub>	176	DQ55
24	DQ13	74	CB5	126	ODT0	178	V <sub>SS</sub>
26	V <sub>SS</sub>	76	DM8	128	ODT1	180	DQ60
28	DM1	78	V <sub>SS</sub>	130	A13	182	DQ61
30	Reset#	80	CB6	132	V <sub>DD</sub>	184	V <sub>SS</sub>
32	V <sub>SS</sub>	82	CB7	134	DQ36	186	DQS7#
34	DQ14	84	V <sub>REFCA</sub>	136	DQ37	188	DQS7
36	DQ15	86	V <sub>DD</sub>	138	V <sub>SS</sub>	190	V <sub>SS</sub>
38	V <sub>SS</sub>	88	A15	140	DM4	192	DQ62
40	DQ20	90	A14	142	DQ38	194	DQ63
42	DQ21	92	A9	144	DQ39	196	V <sub>SS</sub>
44	DM2	94	V <sub>DD</sub>	146	V <sub>SS</sub>	198	EVENT#
46	V <sub>SS</sub>	96	A11	148	DQ44	200	SDA
48	DQ22	98	A7	150	DQ45	202	SCL
50	DQ23	100	A6	152	V <sub>SS</sub>	204	V <sub>TT</sub>
52	V <sub>SS</sub>	102	V <sub>DD</sub>	154	DQS5#		

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

**FUNCTIONAL BLOCK DIAGRAM 8GB DDR3 SDRAM SO-UDIMM,  
2 RANK AND 18 COMPONENTS**



- BA0-BA2 → BA0-BA2: SDRAM D0-D17
- A0-A15 → A0-A15: SDRAM D0-D17
- RAS → RAS: SDRAM D0-D17
- CAS → CAS: SDRAM D0-D17
- WE → WE: SDRAM D0-D17
- ODT0 → ODT: SDRAM D0-D8
- ODT1 → ODT: SDRAM D9-D17
- CKE0 → CKE: SDRAM D0-D8
- CKE1 → CKE: SDRAM D9-D17
- CK0,CK1 → CK: SDRAM D0-D17
- CK0,CK1 → CK: SDRAM D0-D17
- RESET → RESET: SDRAM D0-D17

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationship must be maintained as shown.
3. DQ, DM, DQS/DQS resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDEC document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

**MAXIMUM ELECTRICAL DC CHARACTERISTICS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{DD}$	-0.4	1.975	V
I/O Supply Voltage	$V_{DDQ}$	-0.4	1.975	V
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.4	1.975	V
<b>INPUT LEAKAGE CURRENT</b> Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	$I_I$			$\mu A$
Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
CK, CK#		-16	16	
DM		-2	2	
<b>OUTPUT LEAKAGE CURRENT</b> (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )	$I_{OZ}$	-5	5	$\mu A$
DQ, DQS, DQS#				
$V_{REF}$ LEAKAGE CURRENT ; $V_{REF}$ is on a valid level	$I_{VREF}$	-8	8	$\mu A$

**DC OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	$V_{DD}$	1.425	1.5	1.575	V
I/O Supply Voltage	$V_{DDQ}$	1.425	1.5	1.575	V
I/O Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	$V_{TT}$	$0.49 \times V_{DDQ} - 20mV$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ} + 20mV$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.1$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.1$	V

**AC INPUT OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.175$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.175$	V

**CAPACITANCE**

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

**I<sub>DD</sub> Specifications and Conditions**

(0°C ≤ T<sub>CASE</sub> ≤ + 85°C; V<sub>DDQ</sub> = +1.5V ± 0.075V, V<sub>DD</sub> = +1.5V ± 0.075V)

Parameter & Test Condition	Symbol	max.		Unit	
		12800-11-11-11	10600-9-9-9		
<b>OPERATING CURRENT *) :</b> One device bank Active-Precharge; t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	540	495	mA	
<b>OPERATING CURRENT *) :</b> One device bank; Active-Read-Precharge; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MIN (I <sub>DD</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I <sub>DD4W</sub>	I <sub>DD1</sub>	630	585	mA	
<b>PRECHARGE POWER-DOWN CURRENT:</b> All device banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	Fast Exit	I <sub>DD2P</sub>	270	270	mA
	Slow Exit		270	270	
<b>PRECHARGE QUIET STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	I <sub>DD2Q</sub>	360	360	mA	
<b>PRECHARGE STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD2N</sub>	450	450	mA	
<b>ACTIVE POWER-DOWN CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub> (always fast exit)	I <sub>DD3P</sub>	360	360	mA	
<b>ACTIVE STANDBY CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD3N</sub>	540	540	mA	
<b>OPERATING READ CURRENT:</b> All device banks open, Continuous burst reads; One module rank active; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD4R</sub>	1035	900	mA	

Parameter & Test Condition	Symbol	max.		Unit
		12800-11-11-11	10600-9-9-9	
<b>OPERATING WRITE CURRENT:</b> All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD4W</sub>	1125	945	mA
<b>BURST REFRESH CURRENT:</b> t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); refresh command at every t <sub>RFC</sub> (I <sub>DD</sub> ) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD5</sub>	2610	2610	mA
<b>SELF REFRESH CURRENT:</b> CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V <sub>REF</sub> ; DQ's are floating at V <sub>REF</sub>	I <sub>DD6</sub>	270	270	mA
<b>OPERATING CURRENT*) :</b> Four device bank interleaving READs, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = t <sub>RCD</sub> (I <sub>DD</sub> ) - 1 x t <sub>CK</sub> (I <sub>DD</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ), t <sub>RRD</sub> = t <sub>RRD</sub> (I <sub>DD</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I <sub>DD7</sub>	1710	1665	mA

\*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

**TIMING VALUES USED FOR I<sub>DD</sub> MEASUREMENT**

I <sub>DD</sub> MEASUREMENT CONDITIONS			
SYMBOL	12800-11-11-11	10600-9-9-9	Unit
CL (I <sub>DD</sub> )	11	9	t <sub>CK</sub>
t <sub>RCD</sub> (I <sub>DD</sub> )	13.75	13.5	ns
t <sub>RC</sub> (I <sub>DD</sub> )	48.75	49.5	ns
t <sub>RRD</sub> (I <sub>DD</sub> )	6	6	ns
t <sub>CK</sub> (I <sub>DD</sub> )	1.25	1.5	ns
t <sub>RAS</sub> MIN (I <sub>DD</sub> )	35	36	ns
t <sub>RAS</sub> MAX (I <sub>DD</sub> )	70'200	70'200	ns
t <sub>RP</sub> (I <sub>DD</sub> )	13.75	13.5	ns
t <sub>RFC</sub> (I <sub>DD</sub> )	260	260	ns



**DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

 (0°C ≤ T<sub>CASE</sub> ≤ +85°C; V<sub>DDQ</sub> = +1.5V ± 0.075V, V<sub>DD</sub> = +1.5V ± 0.075V)

AC CHARACTERISTICS		12800-11-11-11		10600-9-9-9		Unit	
PARAMETER	SYMBOL	MIN	MAX	Min	MAX		
Clock cycle time	CL = 11	t <sub>CK</sub> (11)	1.25	-	-	-	ns
	CL = 10	t <sub>CK</sub> (10)	1.5	<1.875	1.5	<1.875	
	CL = 9	t <sub>CK</sub> (9)	1.5	<1.875	1.5	<1.875	
	CL = 8	t <sub>CK</sub> (8)	1.875	<2.5	1.875	<2.5	
	CL = 7	t <sub>CK</sub> (7)	1.875	<2.5	1.875	<2.5	
	CL = 6	t <sub>CK</sub> (6)	2.5	3.3	2.5	3.3	
	CL = 5	t <sub>CK</sub> (5)	3.0	3.3	3.0	3.3	
Internal READ command to first data	t <sub>AA</sub>	13.75	-	13.5	-		
CK high-level width	t <sub>CH</sub> (AVG)	0.47	0.53	0.47	0.53	t <sub>CK</sub>	
CK low-level width	t <sub>CL</sub> (AVG)	0.47	0.53	0.47	0.53	t <sub>CK</sub>	
Data-out high-impedance window from CK/CK#	t <sub>HZ</sub>	-	225	-	250	ps	
Data-out low-impedance window from CK/CK#	t <sub>LZ</sub>	-450	225	-500	250	ps	
DQ and DM input setup time relative to DQS V <sub>REF</sub> =1V/ns	t <sub>DS1V</sub>	160	-	180	-	ps	
DQ and DM input hold time relative to DQS V <sub>REF</sub> =1V/ns	t <sub>DH1V</sub>	145	-	165	-	ps	
DQ and DM input pulse width ( for each input )	t <sub>DIPW</sub>	360	-	400	-	ps	
DQS, DQS# to DQ skew, per access	t <sub>DQSQ</sub>	-	100	-	125	ps	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t <sub>QH</sub>	0.38	-	0.38	-	t <sub>CK</sub> (AVG)	
DQS input high pulse width	t <sub>DQSH</sub>	0.45	0.55	0.45	0.55	t <sub>CK</sub>	
DQS input low pulse width	t <sub>DQSL</sub>	0.45	0.55	0.45	0.55	t <sub>CK</sub>	
DQS, DQS# rising to/from CK, CK#	t <sub>DQSCK</sub>	-225	225	-255	255	ps	
DQS, DQS# rising to/from CK, CK# when DLL disabled	t <sub>DQSCK</sub> DLL DIS	1	10	1	10	ns	
DQS falling edge to CK rising - setup time	t <sub>DSS</sub>	0.18	-	0.2	-	t <sub>CK</sub>	
DQS falling edge from CK rising - hold time	t <sub>DSH</sub>	0.18	-	0.2	-	t <sub>CK</sub>	
DQS read preamble	t <sub>RPRE</sub>	0.9	Note1	0.9	Note1	t <sub>CK</sub>	
DQS read postamble	t <sub>RPST</sub>	0.3	Note2	0.3	Note2	t <sub>CK</sub>	
DQS write preamble	t <sub>WPRE</sub>	0.9	-	0.9	-	t <sub>CK</sub>	
DQS write postamble	t <sub>WPST</sub>	0.3	-	0.3	-	t <sub>CK</sub>	
Positive DQS latching edge to associated clock edge	t <sub>DQSS</sub>	- 0.27	+ 0.27	- 0.25	+ 0.25	t <sub>CK</sub>	
Address and control input pulse width ( for each input )	t <sub>IPW</sub>	560	-	620	-	ps	
CTRL, CMD, Addr setup to CK, CK#	t <sub>IS(Base)</sub>	45	-	65	-	ps	
CTRL, CMD, Addr setup to CK, CK# V <sub>REF</sub> @ 1V/ns	t <sub>IS(1V)</sub>	220	-	240	-	ps	

 1 The maximum preamble is bound by t<sub>LZDQS</sub> (MAX)

 2 The maximum postamble is bound by t<sub>HZDQS</sub> (MAX)

**DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.5\text{V} \pm 0.075\text{V}, V_{\text{DD}} = +1.5\text{V} \pm 0.075\text{V})$ 

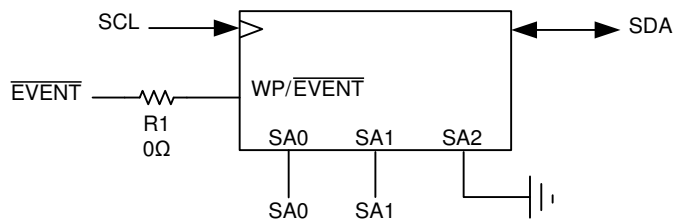
AC CHARACTERISTICS		12800-11-11-11		10600-9-9-9		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
CTRL, CMD, Addr hold to CK, CK#	$t_{\text{IH(Base)}}$	120	-	140	-	ps
CTRL, CMD, Addr hold to CK, CK# $V_{\text{REF}} @ 1\text{V/ns}$	$t_{\text{IH(1V)}}$	220	-	240	-	ps
CAS# to CAS# command delay	$t_{\text{CCD}}$	4	-	4	-	$t_{\text{CK}}$
ACTIVE to ACTIVE (same bank) command period	$t_{\text{RC}}$	48.75	-	49.5	-	ns
ACTIVE to ACTIVE minimum command period	$t_{\text{RRD}}$	max 4nCK,6ns	-	max 4nCK,6ns	-	ns
ACTIVE to READ or WRITE delay	$t_{\text{RCD}}$	13.75	-	13.5	-	ns
Four bank Activate period	$t_{\text{FAW}}$	1K Page size 30	-	30	-	ns
2K Page size		40	-	45	-	
ACTIVE to PRECHARGE command	$t_{\text{RAS}}$	35	70'200	36	70'200	ns
Internal READ to precharge command delay	$t_{\text{RTP}}$	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
Write recovery time	$t_{\text{WR}}$	15	-	15	-	ns
Auto precharge write recovery + precharge time	$t_{\text{DAL}}$	$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$	-	$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$	-	ns
Internal WRITE to READ command delay	$t_{\text{WTR}}$	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
PRECHARGE command period	$t_{\text{RP}}$	13.75	-	13.5	-	ns
LOAD MODE command cycle time	$t_{\text{MRD}}$	4	-	4	-	$t_{\text{CK}}$
REFRESH to ACTIVE or REFRESH to REFRESH command interval	$t_{\text{RFC}}$	260	70'200	260	70'200	ns
Average periodic refresh interval $0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	$t_{\text{REFI}}$	-	7.8	-	7.8	$\mu\text{s}$
$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	$t_{\text{REFI(IT)}}$	-	3.9	-	3.9	
RTT turn-on from ODTL on reference	$t_{\text{AON}}$	-225	225	-250	250	ps
RTT turn-on from ODTL off reference	$t_{\text{AOF}}$	0.3	0.7	0.3	0.7	$t_{\text{CK}}$
Asynchronous RTT turn-on delay (power Down with DLL off)	$t_{\text{AONPD}}$	2	8,5	2	8,5	ns
Asynchronous RTT turn-off delay (power Down with DLL off)	$t_{\text{AOFPD}}$	2	8,5	2	8,5	ns
RTT dynamic change skew	$t_{\text{ADC}}$	0.3	0.7	0.3	0.7	$t_{\text{CK}}$
Exit self refresh to commands not requiring a locked DLL	$t_{\text{XS}}$	max 5nCK,tR FC + 10ns	-	max 5nCK,tR FC + 10ns	-	ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	$t_{\text{WLS}}$	165	-	195	-	ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing	$t_{\text{WLH}}$	165	-	195	-	ps
First DQS, DQS# rising edge	$t_{\text{WLMRD}}$	40	-	40	-	$t_{\text{CK}}$
DQS, DQS# delay	$t_{\text{WLDQSEN}}$	25	-	25	-	$t_{\text{CK}}$

**DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**

(0°C ≤ T<sub>CASE</sub> ≤ + 85°C; V<sub>DDQ</sub> = +1.5V ± 0.075V, V<sub>DD</sub> = +1.5V ± 0.075V)

AC CHARACTERISTICS		12800-11-11-11		10600-9-9-9		
PARAMETER	SYMBOL	MIN	MAX	Min	MAX	Unit
Exit reset from CKE HIGH to a valid command	t <sub>XPR</sub>	max 5nCK, t <sub>RFC</sub> + 10ns	-	max 5nCK, t <sub>RFC</sub> + 10ns	-	t <sub>CK</sub>
Begin power supply ramp to power supplies stable	t <sub>VDDPR</sub>	-	200	-	200	ms
RESET# LOW to power supplies stable	t <sub>RPS</sub>	0	200	0	200	ms
RESET# LOW to I/O and RTT High-Z	t <sub>IOz</sub>	-	20	-	20	ns
Exit precharge power-down to any non-READ command	t <sub>XP</sub>	max 3nCK,6ns	-	max 3nCK,6ns	-	t <sub>CK</sub>
CKE minimum high/low time	t <sub>CKE</sub>	max 3nCK, 5ns	-	max 3nCK, 5.625ns	-	t <sub>CK</sub>

**Temperature Sensor with Serial Presence-Detect EEPROM**



**Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions**

Parameter / Condition	Symbol	Min	Max	Unit
Supply voltage	V <sub>DDSPD</sub>	+3	+3.6	V
Supply current: V <sub>dd</sub> = 3.3V	I <sub>DD</sub>		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V <sub>IH</sub>	+1.45	V <sub>DDSPD</sub> + 1	V
Input low voltage: Logic 0; SCL, SDA	V <sub>IL</sub>	-	550	mV
Output low voltage: I <sub>out</sub> = 2.1mA	V <sub>OL</sub>	-	400	mV
Input current	I <sub>IN</sub>	-5.0	5.0	μA
Temperature sensing range		TBD	TBD	°C
Temperature sensor accuracy		TBD	TBD	°C

**A.C. Characteristics of Temperature Sensor**
 $V_{CC} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ 

Symbol	Parameter / Condition	Min	Max	Unit
f <sub>SCL</sub>	SCL clock frequency	10	400	kHz
t <sub>BUF</sub>	Bus Free Time Between STOP and START	1300	-	ns
t <sub>F</sub>	SDA fall time	-	300	ns
t <sub>R</sub>	SDA rise time	-	300	ns
t <sub>HD:DAT</sub>	Data hold time (accepted for Input Data)	0	-	ns
	Data Hold Time (guaranteed for Output Data)	300	900	ns
t <sub>H:STA</sub>	Start condition hold time	600	-	ns
t <sub>HIGH</sub>	High Period of SCL	600	-	ns
t <sub>LOW</sub>	Low Period of SCL	1300	-	ns
t <sub>SU:DAT</sub>	Data setup time	100	-	ns
t <sub>SU:STA</sub>	Start condition setup time	600	-	ns
t <sub>SU:STO</sub>	Stop condition setup time	600	-	ns
t <sub>TIMEOUT</sub>	SMBus SCL Clock Low Timeout	25	35	ms
t <sub>I</sub>	Noise Pulse Filtered at SCL and SDA Inputs	-	100	ns
t <sub>WR</sub>	Write Cycle Time	-	5	ms
t <sub>PU</sub>	Power-up Delay to Valid Temperature Recording	-	100	ms

**Temperature Characteristics of Temperature Sensor**
 $V_{CC} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ 

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ T <sub>A</sub> ≤ +95°C, active range	±1.0	°C
	+40°C ≤ T <sub>A</sub> ≤ +125°C, monitor range	±2.0	°C
	-40°C ≤ T <sub>A</sub> ≤ +125°C, sensing range	±3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Conversion Time		100	Ms
Thermal Resistance <sup>1</sup> θ <sub>JA</sub>	Junction-to-Ambient (Still Air)	92	°C/W

<sup>1</sup> Power Dissipation is defined as  $P_J = (T_J - T_A)/\theta_{JA}$ , where T<sub>J</sub> is the junction temperature and T<sub>A</sub> is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

**Slave Address Bits of Temperature Sensor**

Device	Device Type Identifier				Select Address Signals			R/W#
	b7 <sup>1</sup>	b6	b5	b4	b3	b2	b1	b0
EEPROM	1	0	1	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/W#
Temp. Sensor	0	0	1	1	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/W#

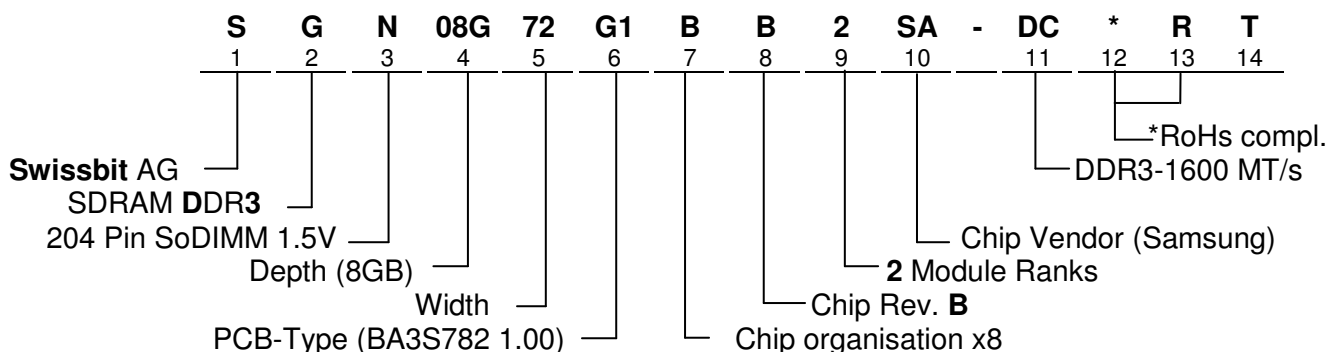
<sup>1</sup> The most significant bit, b7, is sent first.

**SERIAL PRESENCE-DETECT MATRIX**

Byte	Byte Description	12800-11-11-11	10600-9-9-9
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISION	0x11	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x08	
4	SDRAM DEVICE DENSITY & BANKS	0x04	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x21	
6	DDR3 MODULE NOMINAL VDD	0x00	
7	MODULE RANKS & DEVICE DQ COUNT	0x09	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x0B	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x11	0x52
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME ( $t_{CK\ MIN}$ )	0x0A	0x0C
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0xFE	0x3E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME ( $t_{AA\ MIN}$ )	0x69	
17	MIN WRITE RECOVERY TIME ( $t_{WR\ MIN}$ )	0x78	
18	MIN RAS# TO CAS# DELAY ( $t_{RCD\ MIN}$ )	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY ( $t_{RRD\ MIN}$ )	0x30	
20	MIN ROW PRECHARGE DELAY ( $t_{RP\ MIN}$ )	0x69	
21	UPPER NIBBLE FOR $t_{RAS}$ & $t_{RC}$	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY ( $t_{RAS\ MIN}$ )	0x18	0x20
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY ( $t_{RCMIN}$ )	0x81	0x89
24	MIN REFRESH RECOVERY DELAY ( $t_{RFC\ MIN}$ ) LSB	0x20	
25	MIN REFRESH RECOVERY DELAY ( $t_{RFC\ MIN}$ ) MSB	0x08	
26	MIN INTERNAL WRITE TO READ CMD DELAY ( $t_{WTR\ MIN}$ )	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY ( $t_{RTP\ MIN}$ )	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY ( $t_{FAW\ MIN}$ ) MSB	0x00	
29	MIN FOUR ACTIVE WINDOW DELAY ( $t_{FAW\ MIN}$ ) LSB	0xF0	
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x83	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x01	

Byte	Byte Description	12800-11-11-11	10600-9-9-9
32	DDR3-MODULE THERMAL SENSOR	0x80	
33-59	BYTES 33-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x0F	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x03	0x1F
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x00	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0x1880	0x9A12
128-145	MODULE PART NUMBER	"SGN08G72G1BB2SA-xx"	
146	MODULE DIE REV	X	
147	MODULE PCB REV	X	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0xCE	
150-175	MFR RESERVED BYTES 150-175	0x00	
176-255	CUSTOMER RESERVED BYTES 176-255	0xFF	

**Part Number Code**



\* optional / additional information  
 T= Thermal Sensor

Revision History		
Revision	Changes	Date
0.95	initial revision	20.10.2011
0.96	removed DDR3-1066 speed, added DDR3-1600 speed	11.11.2011
1.00	added E-grade	14.06.2012
1.1	Correction SPD-Table	20.06.2012
1.2	Declaration of Conformity	14.12.2012

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# CE Declaration of Conformity

We

**Manufacturer:** Swissbit AG  
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Switzerland

declare under our sole responsibility that the product

**Product Type:** 8GB DDR3 SO-UDIMM  
**Brand Name:** SWISSMEMORY™  
**Product Series:** DDR3 SO-UDIMM  
**Part Number:** SGN08G72G1BB2SA-xxxRT

to which this declaration relates is in conformity with the following directives:

**2002/96/EC Category 3 (WEEE)**

following the provisions of Directive

**2011/65/EU** **Restriction of the use of certain hazardous substances**

Swissbit AG, Dezember 2012



Manuela Kögel  
Head of Quality Management