8GB DDR3 – SDRAM ECC SO-DIMM

204 Pin ECC SO-UDIMM

SLN08G72G2BE2MT-xxRT

8GByte in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency — Marking
  - DDR3 1333 MT/s CL9 — -CC
  - DDR3 1600 MT/s CL11 — -DC
- Module density
  8GB with 18 dies and 2 rank
- Standard Grade (T_A) 0℃ to 70℃; (T_C) 0℃ to 85℃

Environmental Requirements:

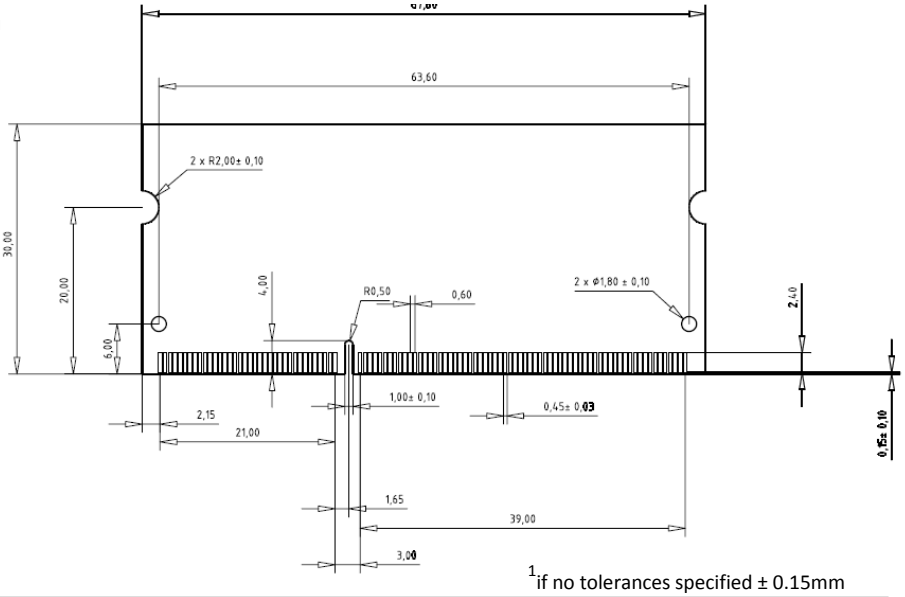
- Operating temperature (ambient)
  Standard Grade 0℃ to 70℃
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55℃ to 100℃
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50℃

Features:

- 204-pin 72-bit DDR3 Small Outline, Dual-In-Line Double Data Rate synchronous DRAM Module
- Module organization: dual rank 1024M x 72
- V_{DD} = 1.35V and 1.5V
- V_{DDQ} = 1.35V and 1.5V
- 1.5V I/O (SSTL_15 compatible)
- Fly-by-bus with termination for C/A & CLK bus
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC EP3-12800 DDR3 SDRAM 72bit-SO-DIMM design spec. and JEDEC- Standard MO-268. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification
  [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR3 - SDRAM component Micron MT41K512M8RH-125:E**
- 512Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit prefetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh, Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write

Figure: mechanical dimensions[1]



[1] if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 204-pin 8-byte DDR3 SDRAM ECC Small Outline Dual-In-line Memory Module (SO-UDIMM) which is organized as x72 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.
The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-UDIMM manufacturer (Swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
1G x 72bit	18 x 512M x 8bit (4Gbit)	16	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions in mm
67.60 (long) x 30(high) x 3.80 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SLN08G72G2BE2MT-CCRT	8GByte	10.6 GB/s	1.5ns/1333MT/s	9-9-9
SLN08G72G2BE2MT-DCRT	8GByte	12.8 GB/s	1.25ns/1600MT/s	11-11-11

Pin Name

A0-9, A11 – A15	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
CB0 – CB07	ECC check bits
DM0-DM8	Input Data Mask
DQS0 – DQS8	Data Strobe, positive line
DQS0# - DQS8#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
S0#, S1#	Chip Select
CK0 – CK1	Clock Inputs, positive line
CK0# - CK1#	Clock Inputs, negative line

Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
V_{DD}	Supply Voltage (1.5V± 0.075V)
$V_{REF}DQ$	Reference voltage: DQ, DM ($V_{DD}/2$)
$V_{REF}CA$	Reference voltage: Control, command, and address ($V_{DD}/2$)
V_{SS}	Ground
V_{TT}	Termination voltage: Used for control, command, and address ($V_{DD}/2$).
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

Pin Configuration

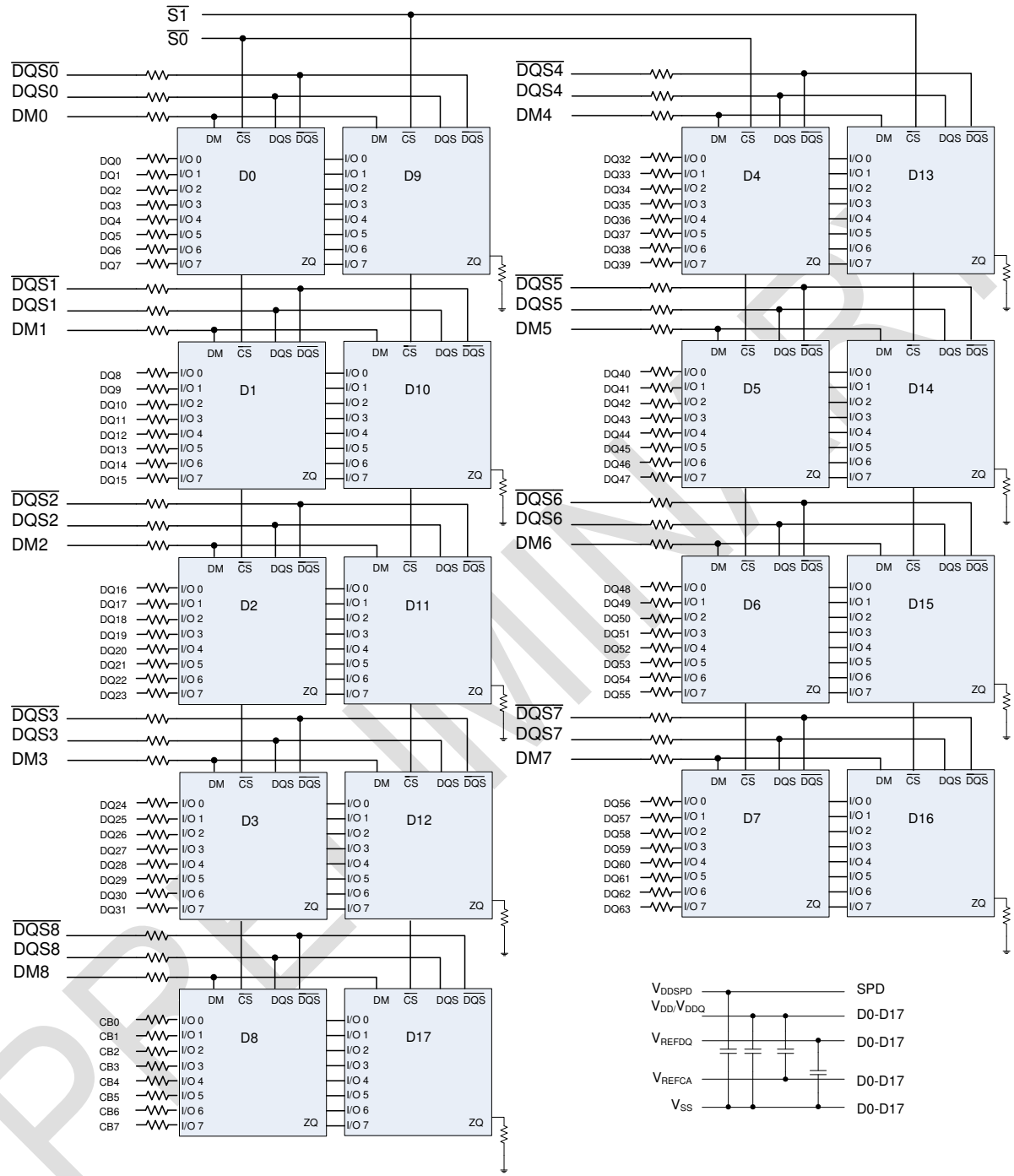
Frontside							
PIN	**Symbol**	**PIN**	**Symbol**	**PIN**	**Symbol**	**PIN**	**Symbol**
1	V_{REFDQ}	53	V_{SS}	103	A3	155	V_{SS}
3	V_{SS}	55	DQ24	105	A1	157	DM5
5	DQ0	57	DQ25	107	A0	159	DQ42
7	DQ1	59	DM3	109	V_{DD}	161	DQ43
9	V_{SS}	61	V_{SS}	111	CK0	163	V_{SS}
11	DM0	63	DQ26	113	CK0#	165	DQ48
13	DQ2	65	DQ27	115	V_{DD}	167	DQ49
15	DQ3	67	V_{SS}	117	A10/AP	169	V_{SS}
17	VSS	69	CB0	119	BA0	171	DQS6#
19	DQ8	71	CB1	121	WE#	173	DQS6
21	DQ9	Key		123	V_{DD}	175	V_{SS}
23	V_{SS}	73	V_{SS}	125	CAS#	177	DQ50
25	DQS1#	75	DQS8#	127	S0#	179	DQ51
27	DQS1	77	DQS8	129	S1#	181	V_{SS}
29	V_{SS}	79	V_{SS}	131	V_{DD}	183	DQ56
31	DQ10	81	CB2	133	DQ32	185	DQ57
33	DQ11	83	CB3	135	DQ33	187	V_{SS}
35	V_{SS}	85	V_{DD}	137	V_{SS}	189	DM7
37	DQ16	87	CKE0	139	DQS4#	191	DQ58
39	DQ17	89	CKE1	141	DQS4	193	DQ59
41	V_{SS}	91	BA2	143	V_{SS}	195	V_{SS}
43	DQS2#	93	V_{DD}	145	DQ34	197	SA0
45	DQS2	95	A12/BC#	147	DQ35	199	V_{DDSPD}
47	V_{SS}	97	A8	149	V_{SS}	201	SA1
49	DQ18	99	A5	151	DQ40	203	V_{TT}
51	DQ19	101	V_{DD}	153	DQ41		

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

Backside							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
2	V_{SS}	54	DQ28	104	A4	156	DQS5
4	DQ4	56	DQ29	106	A2	158	V_{SS}
6	DQ5	58	V_{SS}	108	BA1	160	DQ46
8	V_{SS}	60	DQS3#	110	V_{DD}	162	DQ47
10	DQS0#	62	DQS3	112	CK1	164	V_{SS}
12	DQS0	64	V_{SS}	114	CK1#	166	DQ52
14	V_{SS}	66	DQ30	116	V_{DD}	168	DQ53
16	DQ6	68	DQ31	118	NC(S3#)	170	V_{SS}
18	DQ7	70	V_{SS}	120	NC(S2#)	172	DM6
20	V_{SS}	72	CB4	122	RAS#	174	DQ54
22	DQ12	Key		124	V_{DD}	176	DQ55
24	DQ13	74	CB5	126	ODT0	178	V_{SS}
26	V_{SS}	76	DM8	128	ODT1	180	DQ60
28	DM1	78	V_{SS}	130	A13	182	DQ61
30	Reset#	80	CB6	132	V_{DD}	184	V_{SS}
32	V_{SS}	82	CB7	134	DQ36	186	DQS7#
34	DQ14	84	V_{REFCA}	136	DQ37	188	DQS7
36	DQ15	86	V_{DD}	138	V_{SS}	190	V_{SS}
38	V_{SS}	88	A15	140	DM4	192	DQ62
40	DQ20	90	A14	142	DQ38	194	DQ63
42	DQ21	92	A9	144	DQ39	196	V_{SS}
44	DM2	94	V_{DD}	146	V_{SS}	198	EVENT#
46	V_{SS}	96	A11	148	DQ44	200	SDA
48	DQ22	98	A7	150	DQ45	202	SCL
50	DQ23	100	A6	152	V_{SS}	204	V_{TT}
52	V_{SS}	102	V_{DD}	154	DQS5#		

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

FUNCTIONAL BLOCK DIAGRAMM 8GB DDR3 SDRAM SO-UDIMM, 2 RANK AND 18 COMPONENTS



BA0-BA2 → BA0-BA2: SDRAM D0-D17
A0-A15 → A0-A15: SDRAM D0-D17
$\overline{RAS}$ → $\overline{RAS}$: SDRAM D0-D17
$\overline{CAS}$ → $\overline{CAS}$: SDRAM D0-D17
$\overline{WE}$ → $\overline{WE}$: SDRAM D0-D17
ODT0 → ODT: SDRAM D0-D8
ODT1 → ODT: SDRAM D9-D17
CKE0 → CKE: SDRAM D0-D8
CKE1 → CKE: SDRAM D9-D17
CK0,CK1 → CK: SDRAM D0-D17
$\overline{CK0,CK1}$ → $\overline{CK}$: SDRAM D0-D17
$\overline{RESET}$ → $\overline{RESET}$: SDRAM D0-D17

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationship must be maintained as shown.
3. DQ, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDED document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-0.4	1.975	V
I/O Supply Voltage	V_{DDQ}	-0.4	1.975	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.975	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	I_I			µA
Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
CK, CK#		-16	16	
DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-5	5	µA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-8	8	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.425	1.5	1.575	V
I/O Supply Voltage	V_{DDQ}	1.425	1.5	1.575	V
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51x V_{DDQ}	V
I/O Termination Voltage (system)	V_{TT}	0.49 x V_{DDQ}-20mV	0.50 x V_{DDQ}	0.51x V_{DDQ}+20mV	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1		V_{DDQ} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.1	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.175	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.175	V

CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

Parameter & Test Condition		Symbol	max. 12800 CL11	max. 10600 CL9	Unit
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	495	495	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	585	585	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast Exit	I_{DD2P}	270	270	mA
	Slow Exit		270	270	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	360	360	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	450	360	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF} (always fast exit)		I_{DD3P}	360	360	mA
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	540	540	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD4R}	900	765	mA

Parameter & Test Condition	Symbol	max.		Unit
		12800 CL11	10600 CL9	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	945	810	mA
BURST REFRESH CURRENT: $t_{CK} = t_{CK}$ (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	2610	2160	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	270	270	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); $t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$ (I_{DD}), $t_{RRD} = t_{RRD}$ (I_{DD}), $t_{RCD} = t_{RCD}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	1665	1305	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS			
SYMBOL	**128000 CL11**	**10600 CL9**	**Unit**
CL (I_{DD})	11	9	t_{CK}
t_{RCD} (I_{DD})	13.75	13.5	ns
t_{RC} (I_{DD})	48.75	49.5	ns
t_{RRD} (I_{DD})	5	6	ns
t_{CK} (I_{DD})	1.25	1.5	ns
t_{RAS} MIN (I_{DD})	35	36	ns
t_{RAS} MAX (I_{DD})	70'200	70'200	ns
t_{RP} (I_{DD})	13.75	13.5	ns
t_{RFC} (I_{DD})	260	260	ns

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS			12800 CL11		10600 CL9		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
	CL = 11	t_{CK} (11)	1.25	<1.5	-	-	
	CL = 10	t_{CK} (10)	1.5	<1.875	1.5	<1.875	
	CL = 9	t_{CK} (9)	1.5	<1.875	1.5	<1.875	
	CL = 8	t_{CK} (8)	1.875	<2.5	1.875	<2.5	
	CL = 7	t_{CK} (7)	1.875	<2.5	1.875	<2.5	ns
	CL = 6	t_{CK} (6)	2.5	3.3	2.5	3.3	
Internal READ command to first data		t_{AA}	13.5	-	13.125	-	
CK high-level width		$t_{CH\ (AVG)}$	0.47	0.53	0.47	0.53	t_{CK}
CK low-level width		$t_{CL\ (AVG)}$	0.47	0.53	0.47	0.53	t_{CK}
Data-out high-impedance window from CK/CK#		t_{HZ}	-	250	-	300	ps
Data-out low-impedance window from CK/CK#		t_{LZ}	-500	250	-600	300	ps
DQ and DM input setup time relative to DQS		$t_{DS\ (base)}$	30	-	25	-	ps
DQ and DM input holt time relative to DQS		$t_{DH\ (base)}$	65	-	100	-	ps
DQ and DM input setup time relative to DQS V_{REF}=1V/ns		t_{DS1V}	180	-	200	-	ps
DQ and DM input hold time relative to DQS V_{REF}=1V/ns		t_{DH1V}	165	-	200	-	ps
DQ and DM input pulse width (for each input)		t_{DIPW}	400	-	490	-	ps
DQS, DQS# to DQ skew, per access		t_{DQSQ}	-	125	-	150	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	0.38	-	0.38	-	$t_{CK\ (AVG)}$
DQS input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}
DQS input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}
DQS, DQS# rising to/from CK, CK#		t_{DQSCK}	-255	255	-300	300	ps
DQS, DQS# rising to/from CK, CK# when DLL disabled		$t_{DQSCK\ DLL\ DIS}$	1	10	1	10	ns
DQS falling edge to CK rising - setup time		t_{DSS}	0.2	-	0.2	-	t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2	-	0.2	-	t_{CK}
DQS read preamble		t_{RPRE}	0.9	Note1	0.9	Note1	t_{CK}
DQS read postamble		t_{RPST}	0.3	Note2	0.3	Note2	t_{CK}
DQS write preamble		t_{WPRE}	0.9	-	0.9	-	t_{CK}
DQS write postamble		t_{WPST}	0.3	-	0.3	-	t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	620	-	780	-	ps
CTRL, CMD, Addr setup to CK, CK#		$t_{IS(Base)}$	65	-	125	-	ps
CTRL, CMD, Addr setup to CK, CK#	V_{REF} @ 1V/ns	$t_{IS(1V)}$	240	-	300	-	ps

1 The maximum preamble is bound by tLZDQS (MAX)

2 The maximum postamble is bound by tHZDQS (MAX)

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

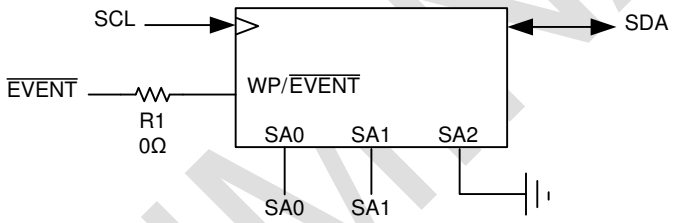
AC CHARACTERISTICS			12800 CL11		10600 CL9		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
CTRL, CMD, Addr hold to CK, CK#		$t_{IH(Base)}$	140	-	200	-	ps
CTRL, CMD, Addr hold to CK, CK# V_{REF} @ 1V/ns		$t_{IH(1V)}$	240	-	300	-	ps
CAS# to CAS# command delay		t_{CCD}	4	-	4	-	t_{CK}
ACTIVE to ACTIVE (same bank) command period		t_{RC}	49.5	-	50.625	-	ns
ACTIVE to ACTIVE minimum command period		t_{RRD}	max 4nCK,10ns	-	max 4nCK,10ns	-	ns
ACTIVE to READ or WRITE delay		t_{RCD}	13.5	-	13.125	-	ns
Four bank Activate period	1K Page size	t_{FAW}	30	-	37.5	-	ns
	2K Page size		45	-	50	-	
ACTIVE to PRECHARGE command		t_{RAS}	36	70'200	37.5	70'200	ns
Internal READ to precharge command delay		t_{RTP}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
Write recovery time		t_{WR}	15	-	15	-	ns
Auto precharge write recovery + precharge time		t_{DAL}	t_{WR} + t_{RP}/t_{CK}	-	t_{WR} + t_{RP}/t_{CK}	-	ns
Internal WRITE to READ command delay		t_{WTR}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
PRECHARGE command period		t_{RP}	13.5	-	13.125	-	ns
LOAD MODE command cycle time		t_{MRD}	4	-	4	-	t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval		t_{RFC}	260	70'200	260	70'200	ns
Average periodic refresh interval 0 °C ≤ T_{CASE} ≤ 85°C		t_{REFI}	-	7.8	-	7.8	µs
85 °C < T_{CASE} ≤ 95°C		$t_{REFI\ (IT)}$	-	3.9	-	3.9	
RTT turn-on from ODTL on reference		t_{AON}	-250	250	-300	300	ps
RTT turn-on from ODTL off reference		t_{AOF}	0.3	0.7	0.3	0.7	t_{CK}
Asynchronous RTT turn-on delay (power Down with DLL off)		t_{AONPD}	2	8,5	2	8,5	ns
Asynchronous RTT turn-off delay (power Down with DLL off)		t_{AOFPD}	2	8,5	2	8,5	ns
RTT dynamic change skew		t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}
Exit self refresh to commands not requiring a locked DLL		t_{XS}	max 5nCK,tR FC + 10ns	-	max 5nCK,tR FC + 10ns	-	ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing		t_{WLS}	195	-	245	-	ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing		t_{WLH}	195	-	245	-	ps
First DQS, DQS# rising edge		t_{WLMRD}	40	-	40	-	t_{CK}
DQS, DQS# delay		$t_{WLDQSEN}$	25	-	25	-	t_{CK}

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS		12800-11-11-11		10600-9-9-9		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
Exit reset from CKE HIGH to a valid command	t_{XPR}	max 5nCK, t_{RFC} + 10ns	-	max 5nCK, t_{RFC} + 10ns	-	t_{CK}
Begin power supply ramp to power supplies stable	t_{VDDPR}	-	200	-	200	ms
RESET# LOW to power supplies stable	t_{RPS}	0	200	0	200	ms
RESET# LOW to I/O and RTT High-Z	t_{IOz}	-	20	-	20	ns
Exit precharge power-down to any non-READ command	t_{XP}	max 3nCK,6ns	-	max 3nCK,7.5ns	-	t_{CK}
CKE minimum high/low time	t_{CKE}	max 3nCK, 5.625ns	-	max 3nCK, 5.625ns	-	t_{CK}

Temperature Sensor with Serial Presence-Detect EEPROM



Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter / Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DDSPD}	+3	+3.6	V
Supply current: Vdd = 3.3V	I_{DD}		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	+1.45	V_{DDSPD} +1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	-	550	mV
Output low voltage: Iout = 2.1mA	V_{OL}	-	400	mV
Input current	I_{IN}	-5.0	5.0	µA
Temperature sensing range		TBD	TBD	℃
Temperature sensor accuracy		TBD	TBD	℃

A.C. Characteristics of Temperature Sensor

V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C

Symbol	Parameter / Condition	Min	Max	Unit
f_{SCL}	SCL clock frequency	10	400	kHz
t_{BUF}	Bus Free Time Between STOP and START	1300	-	ns
t_F	SDA fall time	-	300	ns
t_R	SDA rise time	-	300	ns
$t_{HD:DAT}$	Data hold time (accepted for Input Data)	0	-	ns
	Data Hold Time (guaranteed for Output Data)	300	900	ns
$t_{H:STA}$	Start condition hold time	600	-	ns
t_{HIGH}	High Period of SCL	600	-	ns
t_{LOW}	Low Period of SCL	1300	-	ns
$t_{SU:DAT}$	Data setup time	100	-	ns
$t_{SU:STA}$	Start condition setup time	600	-	ns
$t_{SU:STO}$	Stop condition setup time	600	-	ns
$t_{TIMEOUT}$	SMBus SCL Clock Low Timeout	25	35	ms
t_I	Noise Pulse Filtered at SCL and SDA Inputs	-	100	ns
t_{WR}	Write Cycle Time	-	5	ms
t_{PU}	Power-up Delay to Valid Temperature Recording	-	100	ms

Temperature Characteristics of Temperature Sensor

V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ T_A ≤ +95°C, active range	±1.0	°C
	+40°C ≤ T_A ≤ +125°C, monitor range	±2.0	°C
	-40°C ≤ T_A ≤ +125°C, sensing range	±3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Conversion Time		100	Ms
Thermal Resistance[1] θ_{JA}	Junction-to-Ambient (Still Air)	92	°C/W

[1] Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where TJ is the junction temperature and TA is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

Slave Address Bits of Temperature Sensor

Device	Device Type Identifier				Select Address Signals			R/W#
	b7[1]	b6	b5	b4	b3	b2	b1	b0
EEPROM	1	0	1	0	A_2	A_1	A_0	R/W#
Temp. Sensor	0	0	1	1	A_2	A_1	A_0	R/W#

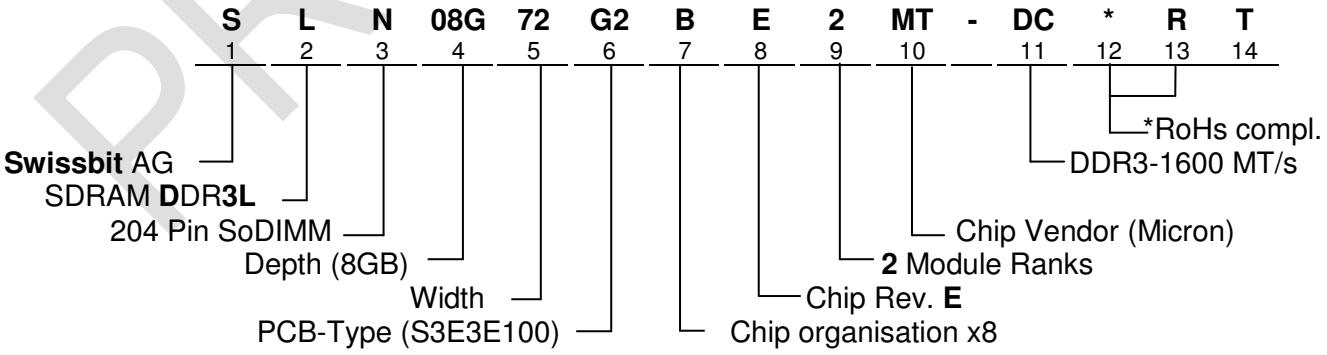
[1] The most significant bit, b7, is sent first.

SERIAL PRESENCE-DETECT MATRIX

Byte	Byte Description	12800 CL11	10600 CL9
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISON	0x11	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x08	
4	SDRAM DEVICE DENSITY & BANKS	0x04	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x21	
6	DDR3 MODULE NOMINAL VDD	0x02	
7	MODULE RANKS & DEVICE DQ COUNT	0x09	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x0B	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x11	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME ($t_{CK\ MIN}$)	0x0A	0x0C
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0xFE	0x7E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME ($t_{AA\ MIN}$)	0x69	
17	MIN WRITE RECOVERY TIME ($t_{WR\ MIN}$)	0x78	
18	MIN RAS# TO CAS# DELAY ($t_{RCD\ MIN}$)	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY ($t_{RRD\ MIN}$)	0x30	
20	MIN ROW PRECHARGE DELAY ($t_{RP\ MIN}$)	0x69	
21	UPPER NIBBLE FOR t_{RAS} & t_{RC}	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY ($t_{RAS\ MIN}$)	0x18	0x20
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY (tRCMIN)	0x81	0x8C
24	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) LSB	0x20	
25	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) MSB	0x08	
26	MIN INTERNAL WRITE TO READ CMD DELAY ($t_{WTR\ MIN}$)	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY ($t_{RTP\ MIN}$)	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) MSB	0x00	
29	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) LSB	0xF0	
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x83	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x05	

Byte	Byte Description	12800 CL11	10600 CL9
32	DDR3-MODULE THERMAL SENSOR	0x80	
33-59	BYTES 33-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x0F	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x03	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x00	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0x644D	0xC62B
128-145	MODULE PART NUMBER	"SLN08G72G2BE2MT-XX"	
146	MODULE DIE REV	X	
147	MODULE PCB REV	X	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0x2C	
150-175	MFR RESERVED BYTES 150-175	0x00	
176-255	CUSTOMER RESERVED BYTES 176-255	0xff	

Part Number Code



* optional / additional information
T= Thermal Sensor

Revision History		
Revision	Changes	Date
0.90	Preliminary version	14.12.2012

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CE Declaration of Conformity

We

Manufacturer: **Swissbit AG**
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Switzerland

declare under our sole responsibility that the product

Product Type: **8GB DDR3L SO-UDIMM**
Brand Name: **SWISSMEMORY™**
Product Series: **DDR3L SO-UDIMM**
Part Number: **SLN08G72G2BE2MT-xxxRT**

to which this declaration relates is in conformity with the following directives:

2002/96/EC Category 3 (WEEE)

following the provisions of Directive

Restriction of the use of certain hazardous substances

2011/65/EU

Swissbit AG, Dezember 2012

Manuela Kögel
Head of Quality Management