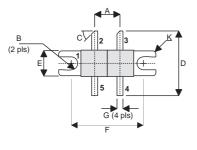
TetraFET

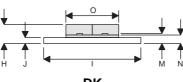
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ROHS COMPLIANT METAL GATE RF SILICON FET

MECHANICAL DATA





DK

 PIN 1
 SOURCE (COMMON)
 PIN 2
 DRAIN 1

 PIN 3
 DRAIN 2
 PIN 4
 GATE 2

 PIN 5
 GATE 1

DIM	mm	Tol.	Inches	Tol.
Α	6.45	0.13	0.254	0.005
В	1.65R	0.13	0.065R	0.005
С	45°	5°	45°	5°
D	16.51	0.76	0.650	0.03
Е	6.47	0.13	0.255	0.005
F	18.41	0.13	0.725	0.005
G	1.52	0.13	0.060	0.005
Н	5.08	max	0.200	max
1	24.76	0.13	0.975	0.005
J	1.52	0.13	0.060	0.005
К	0.81R	0.13	0.032R	0.005
М	0.10	0.02	0.004	0.001
Ν	2.16	0.13	0.085	0.005
0	12.80	max	0.504	max

GOLD METALLISED

MULTI-PURPOSE SILICON DMOS RF FET 100W – 28V – 500MHz PUSH–PULL

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN 10 dB MINIMUM

APPLICATIONS

• HF/VHF/UHF COMMUNICATIONS from 1 MHz to 500 MHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25℃ unless otherwise stated)

	(Case	,
P _D	Power Dissipation	292W
BV _{DSS}	Drain – Source Breakdown Voltage	70V
BV _{GSS}	Gate – Source Breakdown Voltage	±20V
I _{D(sat)}	Drain Current	15A
T _{stg}	Storage Temperature	–65 to 150℃
Тj	Maximum Operating Junction Temperature	200°C

* Per Side



ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

	Parameter	Test	Condition	าร	Min.	Тур.	Max.	Unit
	PER SIDE							
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$	I _D =	100mA	70			~
IDSS	Zero Gate Voltage Drain Current	V _{DS} = 28V	V _{GS}	= 0			3	mA
I _{GSS}	Gate Leakage Current	$V_{GS} = 20V$	V _{DS}	= 0			1	μA
V _{GS(th)}	Gate Threshold Voltage*	I _D = 10mA	V _{DS}	= V _{GS}	1		7	V
9 _{fs}	Forward Transconductance*	V _{DS} = 10V	I _D =	3A	2.4			mhos
V _{GS(th)m}	Gate Threshold Voltage atch Matching Between Sides	I _D = 10mA	V _{DS}	= V _{GS}			0.1	V
	TOTAL DEVICE							
G _{PS}	Common Source Power Gain	P _O = 100W	1		10			dB
η	Drain Efficiency	V _{DS} = 28V	I _{DQ} =	= 1.2A	50			%
VSWR	Load Mismatch Tolerance	f = 500MHz	2					_
PER SIDE								
C _{iss}	Input Capacitance	$V_{DS} = 28V$	$V_{GS} = -5V$	f = 1MHz			180	pF
C _{oss}	Output Capacitance	V _{DS} = 28V	$V_{GS} = 0$	f = 1MHz			90	pF
C _{rss}	Reverse Transfer Capacitance	V _{DS} = 28V	$V_{GS} = 0$	f = 1MHz			7.5	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle $\leq 2\%$

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

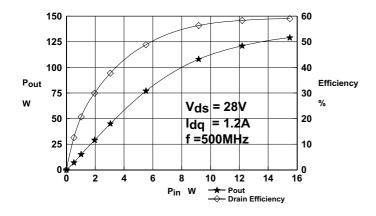
THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max. 0.6℃ / W]
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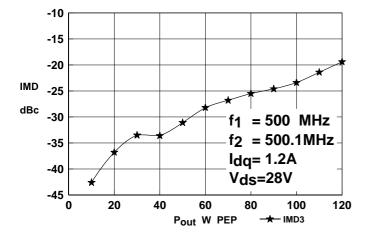
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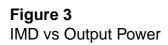


150 13 125 12 100 11 Pout Gain 75 10 w dB 9 50 Vds = 28V = 1.2A 25 ldq | 8 f =500MHz 0 0 2 4 6 10 14 16 8 12 Pin W Pout Gain

Figure 1 Power Output and Efficiency vs. Input







OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency	Z _S	ZL	
MHz	Ω	Ω	
500	2.0 - j2.2		

N.B. Impedances measured terminal to terminal



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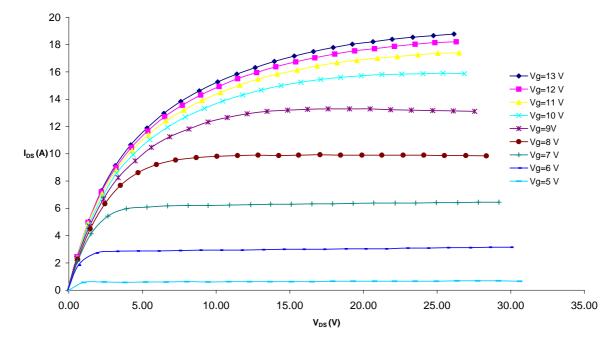
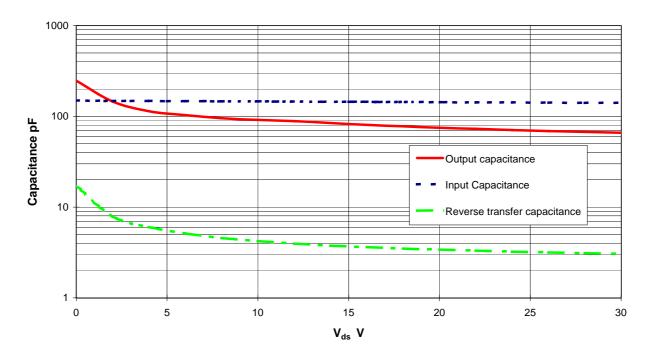


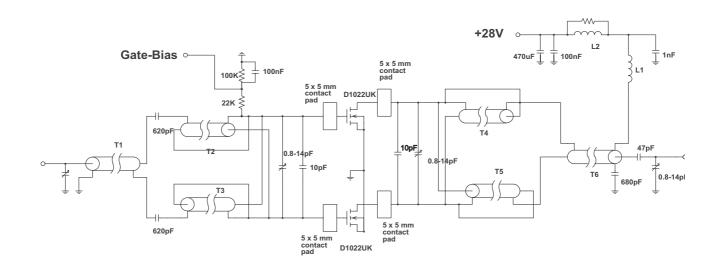
Figure 4 – Typical IV Characteristics.







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D1022UK 500MHz TEST FIXTURE

- T1, 6 7cm UT85 50 Ohm semi-rigid coax on Siemens B62152A1x1 2 hole ferrite core
- T2, 3,4, 5 7.7 cm UT85-15 15 ohm semi-rigid coax
- L1 6 turns 19swg enamelled copper wire, 3.5mm internal diameter
- L2 8.5 turns 19swg enamelled copper wire on Fair-rite FT82 ferrite core