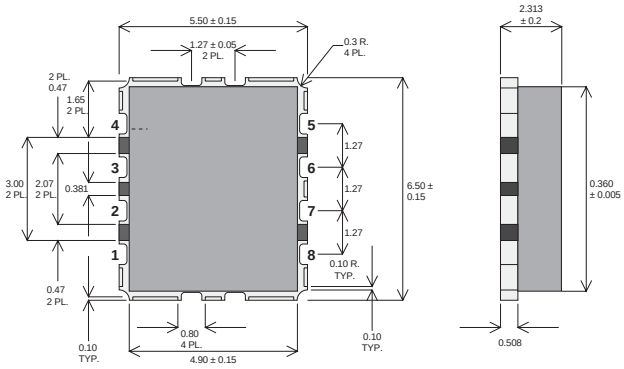
TetraFET

D1031UK

ROHS COMPLIANT METAL GATE RF SILICON FET

MECHANICAL DATA

Dimensions in mm.



F-0127 PACKAGE

PIN 1 – SOURCE	PIN 5 – SOURCE
PIN 2 – DRAIN	PIN 6 – GATE
PIN 3 – DRAIN	PIN 7 – GATE
PIN 4 – SOURCE	PIN 8 – SOURCE

Ceramic Material: Alumina.

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 10W – 28V – 500MHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **VERY LOW C_{rss}**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN – 13 dB MINIMUM**

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS from 1 MHz to 1 GHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25℃ unless otherwise stated)

P_D	Power Dissipation	30W
BV_{DSS}	Drain – Source Breakdown Voltage	70V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	5A
T_{stg}	Storage Temperature	–65 to 150℃
T_j	Maximum Operating Junction Temperature	200℃

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0	I_D = 100mA	70			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 28V	V_{GS} = 0			1	mA
I_{GSS}	Gate Leakage Current	V_{GS} = 20V	V_{DS} = 0			1	µA
$V_{GS(th)}$	Gate Threshold Voltage*	I_D = 10mA	V_{DS} = V_{GS}	1		7	V
g_{fs}	Forward Transconductance*	V_{DS} = 10V	I_D = 1A	0.8			S
G_{PS}	Common Source Power Gain	P_O = 10W		13			dB
η	Drain Efficiency	V_{DS} = 28V	I_{DQ} = 0.1A	50			%
VSWR	Load Mismatch Tolerance	f = 500MHz		20:1			—
C_{iss}	Input Capacitance	V_{DS} = 0V	V_{GS} = –5V f = 1MHz			60	pF
C_{oss}	Output Capacitance	V_{DS} = 28V	V_{GS} = 0 f = 1MHz			30	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 28V	V_{GS} = 0 f = 1MHz			2.5	pF

* Pulse Test: Pulse Duration = 300 µs , Duty Cycle ≤ 2%

THERMAL DATA

$R_{THj–case}$	Thermal Resistance Junction – Case	Max. 6°C / W

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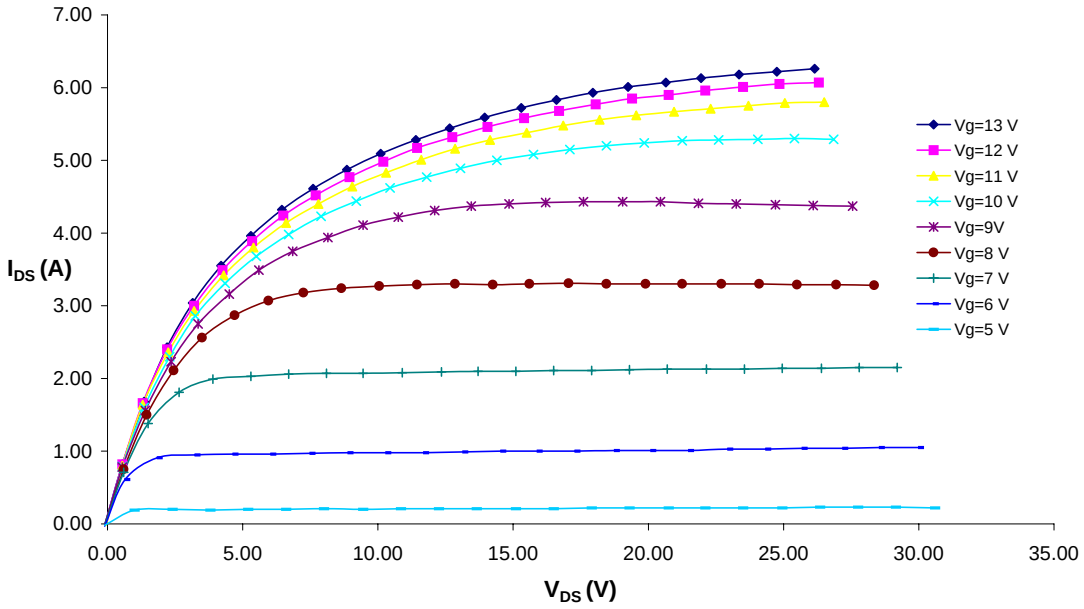

Figure 1 – Typical IV Characteristics.

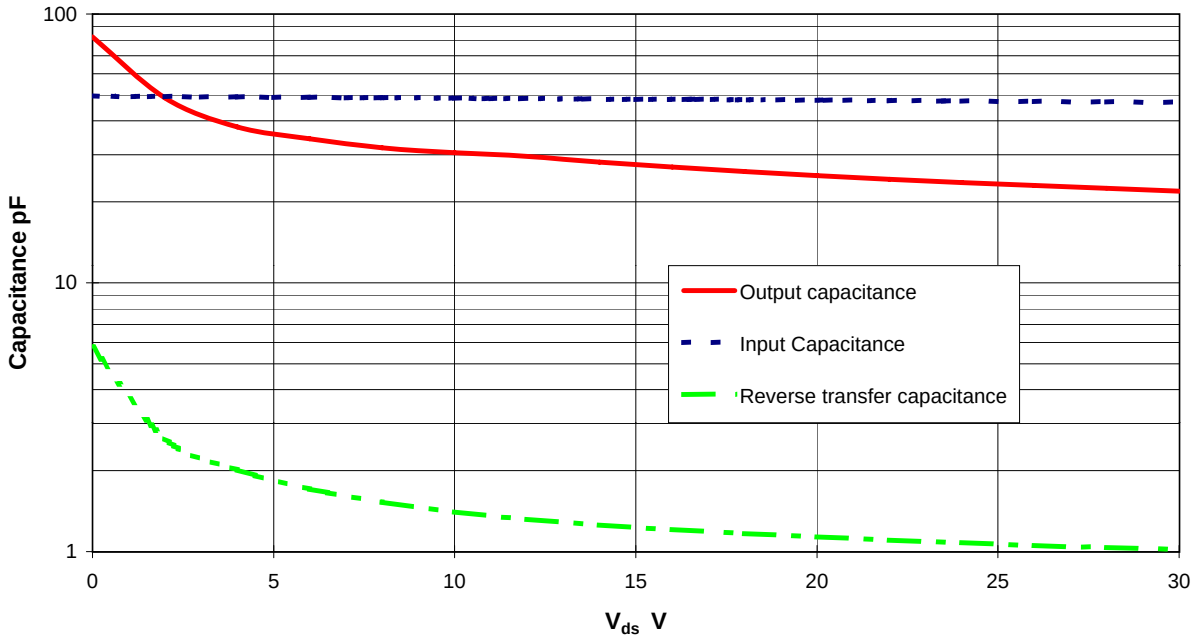

Figure 2 – Typical CV Characteristics.

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