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Solutions for Sustainability

ACT8865

Rev 1, 01-Aug-13

Advanced PMU for Atmel SAMA5D3 Series & SAM9 Series Processors

FEATURES

- **Three Step-Down DC/DC Converters**
- **Four Low-Dropout Linear Regulators**
- **I²C™ Serial Interface**
- **Advanced Enable/Disable Sequencing Controller**
- **Minimal External Components**
- **Tiny 4×4mm TQFN44-32 Package**
  - **0.75mm Package Height**
  - **Pb-Free and RoHS Compliant**

GENERAL DESCRIPTION

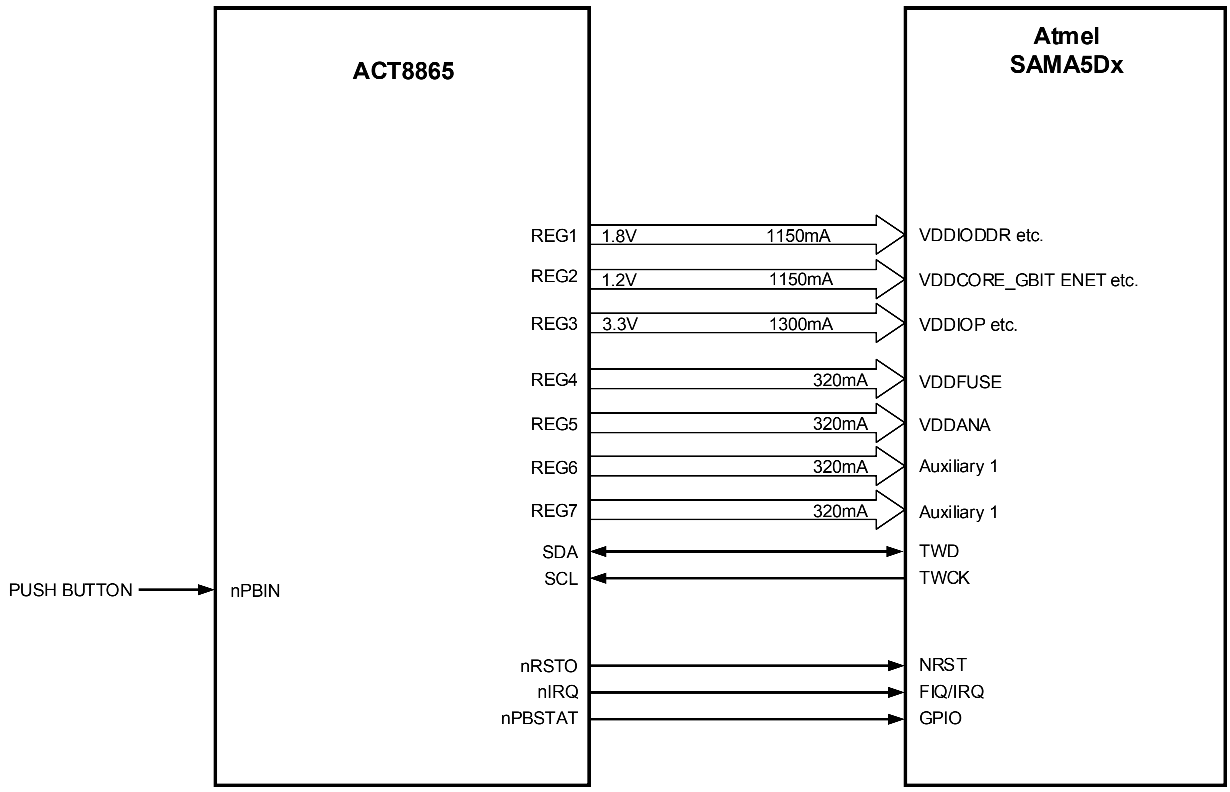
The ACT8865 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution, optimized for the unique power, voltage-sequencing, and control requirements of the Atmel SAMA5D3 series: SAMA5D[31/33/34/35/36] and SAM9 series:SAM9G[15/25/35/45/46];SAM9X[25/35], SAM9M[10/11], SAM9N[11/12] processors. It is ideal for a wide range of high performance portable handheld applications such as human-machine interfaces, control panels, smart grid infrastructures, network gateways, M2M systems, 2D barcode scanners, barcode printers, machine vision equipment, as well as home and commercial building automations, POS terminals, medical devices and white goods.

This device features three step-down DC/DC converters and four low-noise, low-dropout linear regulators.

The three DC/DC converters utilize a high-efficiency, fixed-frequency (2MHz), current-mode PWM control architecture that requires a minimum number of external components. Two DC/DCs are capable of supplying up to 1150mA of output current, while the third supports up to 1300mA. All four low-dropout linear regulators are high-performance, low-noise, regulators that supply up to 320mA.

The ACT8865 is available in a compact, Pb-Free and RoHS-compliant TQFN44-32 package.

TYPICAL APPLICATION DIAGRAM



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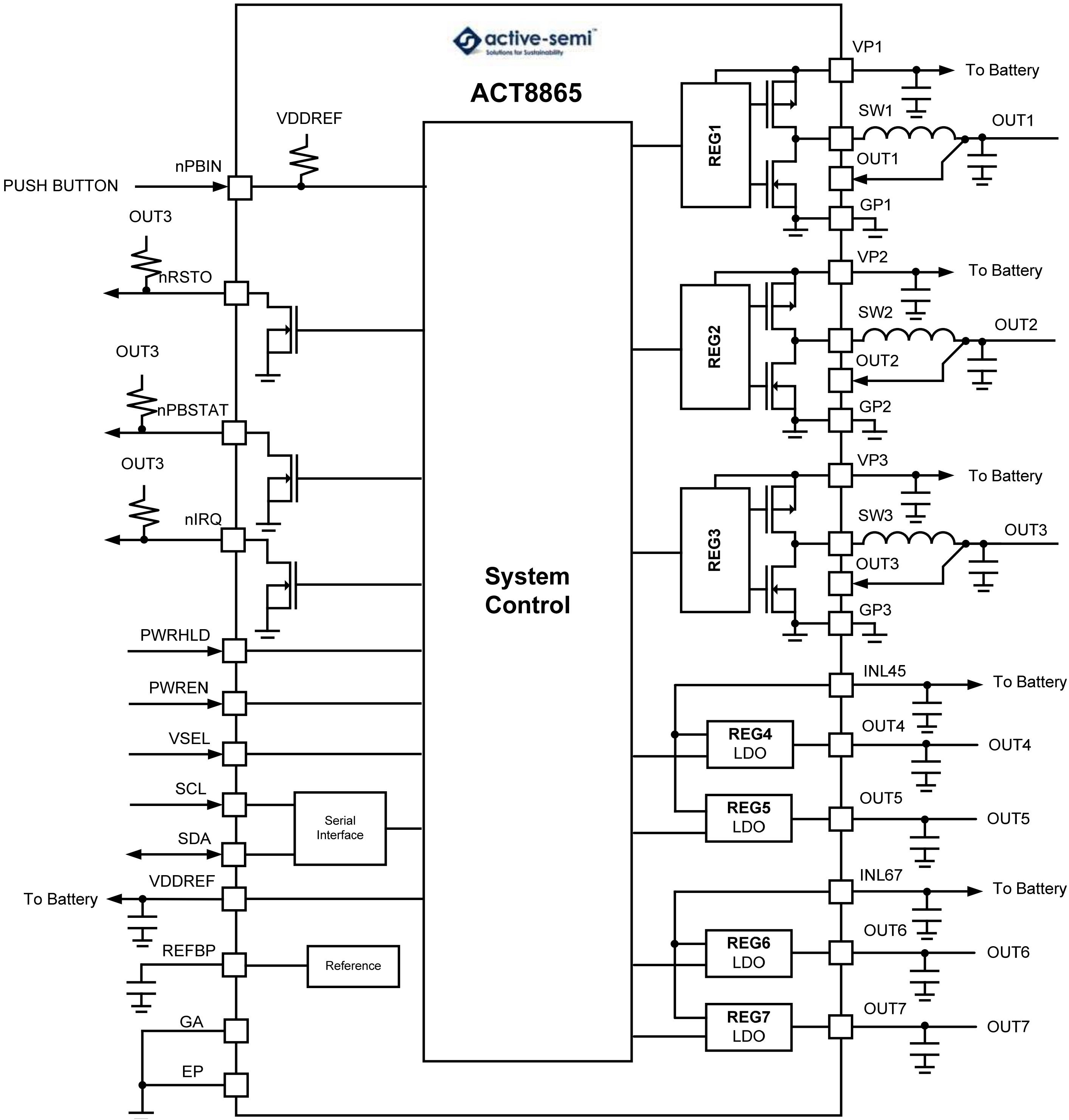
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①②③

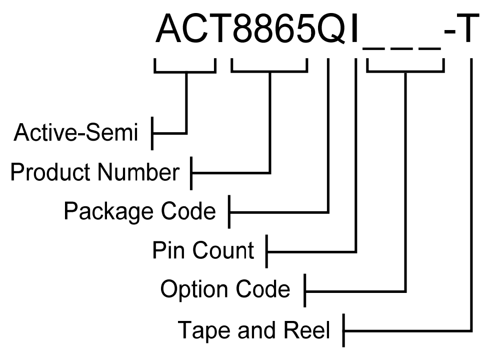
PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8865QI303-T	1.8V	1.2V④	3.3V	0.6V	0.6V	0.6V	0.6V	TQFN44-32	32	-40°C to +85°C

①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

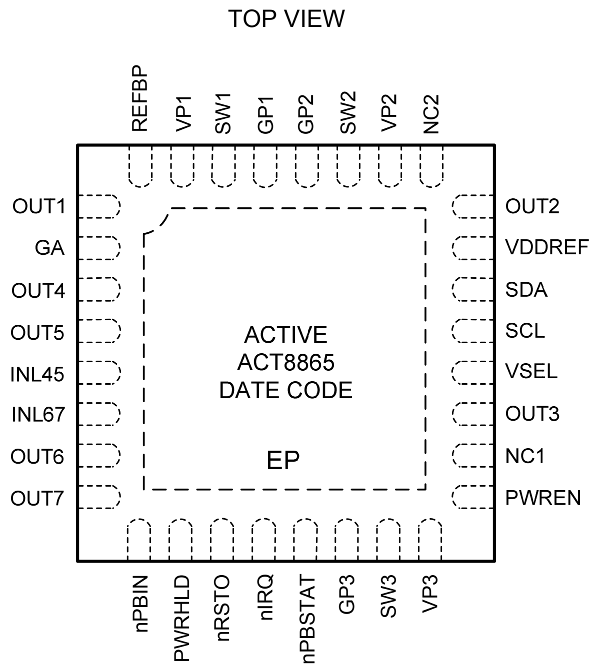
②: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity is 12,000 units.

③: To select V_{STBYx} as a output regulation voltage of REGx, drive VSEL to a logic high. The V_{STBYx} can be set by software via I^2C interface, refer to appropriate sections of this datasheet for V_{STBYx} setting.

④: V_{OUT2} = 1.2V @VSEL=0 and V_{OUT2} = 1.0V @VSEL=VIN



PIN CONFIGURATION



Thin - QFN (TQFN44-32)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	OUT1	Output Feedback Sense for REG1. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
2	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP1,GP2 and GP3 together at a single point as close to the IC as possible.
3	OUT4	Output Voltage for REG4. Capable of delivering up to 320mA of output current. Connect a 3.3µF ceramic capacitor from OUT4 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
4	OUT5	Output Voltage for REG5. Capable of delivering up to 320mA of output current. Connect a 3.3µF ceramic capacitor from OUT5 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
5	INL45	Power Input for REG4 and REG5. Bypass to GA with a high quality ceramic capacitor placed as close to the IC as possible.
6	INL67	Power Input for REG6 and REG7. Bypass to GA with a high quality ceramic capacitor placed as close to the IC as possible.
7	OUT6	Output Voltage for REG6. Capable of delivering up to 320mA of output current. Connect a 3.3µF ceramic capacitor from OUT6 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
8	OUT7	Output Voltage for REG7. Capable of delivering up to 320mA of output current. Connect a 3.3µF ceramic capacitor from OUT7 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
9	nPBIN	Master Enable Input. Drive nPBIN to GA through a 50kΩ resistor to enable the IC, drive nPBIN directly to GA to assert a manual reset condition. Refer to the *nPBIN Multi-Function Input* section for more information. nPBIN is internally pulled up to V_{VDDREF} through a 35kΩ resistor.
10	PWRHLD	Power Hold Input. Refer to the *Control Sequences* section for more information.
11	nRSTO	Active Low Reset Output. See the *nRSTO Output* section for more information.
12	nIRQ	Open-Drain Interrupt Output. nIRQ asserts any time an unmasked fault condition exists or an interrupt occurs. See the *nIRQ Output* section for more information.
13	nPBSTAT	Active-Low Open-Drain Push-Button Status Output. nPBSTAT is asserted low whenever the nPBIN is pushed, and is high-Z otherwise. See the *nPBSTAT Output* section for more information.
14	GP3	Power Ground for REG3. Connect GA, GP1, GP2, and GP3 together at a single point as close to the IC as possible.
15	SW3	Switching Node Output for REG3. Connect this pin to the switching end of the inductor.
16	VP3	Power Input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.
17	PWREN	Power Enable Input. Refer to the *Control Sequences* section for more information.
18	NC1	Not Connected. Not internally connected.
19	OUT3	Output Feedback Sense for REG3. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
20	VSEL	Step-Down DC/DCs Output Voltage Selection. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage. See the *Output Voltage Programming* section for more information.
21	SCL	Clock Input for I^2C Serial Interface.
22	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
23	VDDREF	Power supply for the internal reference. Connect this pin directly to the system power supply. Bypass VDDREF to GA with a 100nF capacitor placed as close to the IC as possible. Star connection with VP1, VP2 and VP3 preferred.
24	OUT2	Output Feedback Sense for REG2. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
25	NC2	Not Connected. Not internally connected.
26	VP2	Power Input for REG2 and System Control. Bypass to GP2 with a high quality ceramic capacitor placed as close to the IC as possible.
27	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
28	GP2	Power Ground for REG2. Connect GA, GP1,GP2 and GP3 together at a single point as close to the IC as possible.
29	GP1	Power Ground for REG1. Connect GA, GP1,GP2 and GP3 together at a single point as close to the IC as possible.
30	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
31	VP1	Power Input for REG1. Bypass to GP1 with a high quality ceramic capacitor placed as close to the IC as possible.
32	REFBP	Reference Bypass. Connect a 0.047µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1 to GP1, VP2 to GP2, VP3 to GP3	-0.3 to + 6	V
INL, VDDREF to GA	-0.3 to + 6	V
nPBIN, SCL, SDA, REFBP, PWRHLD, PWREN, VSEL to GA	-0.3 to (V_{VDDREF} + 0.3)	V
nRSTO, nIRQ, nPBSTAT to GA	-0.3 to + 6	V
SW1, OUT1 to GP1	-0.3 to (V_{VP1} + 0.3)	V
SW2, OUT2 to GP2	-0.3 to (V_{VP2} + 0.3)	V
SW3, OUT3 to GP3	-0.3 to (V_{VP3} + 0.3)	V
OUT4, OUT5, OUT6, OUT7 to GA	-0.3 to (V_{INL} + 0.3)	V
GP1, GP2, GP3 to GA	-0.3 to + 0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	27.5	°C/W
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

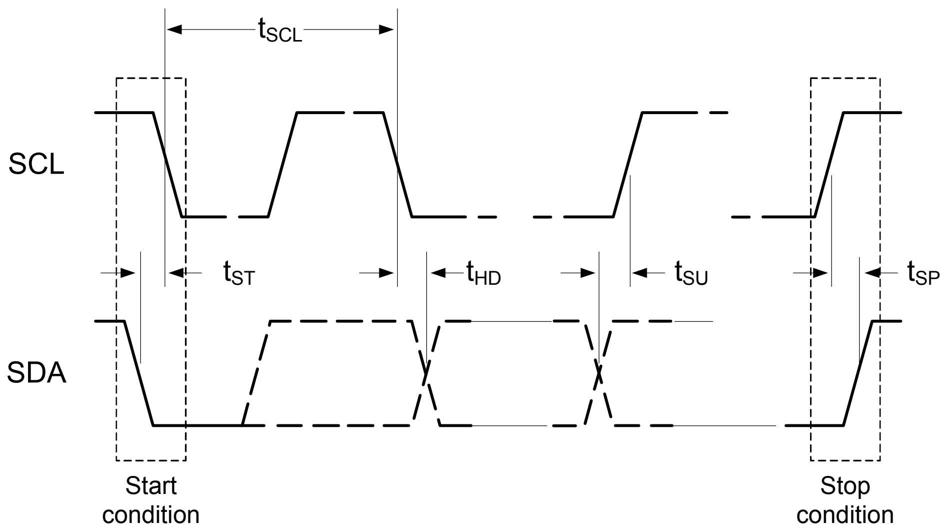
I^2C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{VDDREF} = 3.1V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA Input High	V_{VDDREF} = 3.1V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SDA Leakage Current				1	µA
SCL Leakage Current			1	2	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1:

I^2C Compatible Serial Bus Timing



GLOBAL REGISTER MAP

OUTPUT	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	NAME	TRST	nSYSMODE	nSYSLEVMSK	nSYSSTAT	SYSLEV[3]	SYSLEV[2]	SYSLEV[1]	SYSLEV[0]
		DEFAULT①	1	1	0	R	0	1	1	1
SYS	0x01	NAME	*Reserved*	*Reserved*	*MSTROFF*	*Reserved*	SCRATCH	SCRATCH	*Reserved*	SCRATCH
		DEFAULT①	0	0	0	0	0	0	0	0
REG1	0x20	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG1	0x21	NAME	*Reserved*	*Reserved*	VSET2[5]	VSET2[4]	VSET2[3]	VSET2[2]	VSET2[1]	VSET2[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG1	0x22	NAME	ON	PHASE	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	0	1	0	0	1	0	R
REG2	0x30	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG2	0x31	NAME	*Reserved*	*Reserved*	VSET2[5]	VSET2[4]	VSET2[3]	VSET2[2]	VSET2[1]	VSET2[0]
		DEFAULT①	0	0	0	1	0	0	0	0
REG2	0x32	NAME	ON	PHASE	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	0	1	0	1	0	0	R
REG3	0x40	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG3	0x41	NAME	*Reserved*	*Reserved*	VSET2[5]	VSET2[4]	VSET2[3]	VSET2[2]	VSET2[1]	VSET2[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG3	0x42	NAME	ON	PWRSTAT	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	0	1	0	0	0	0	R
REG4	0x50	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	0	0	0	0	0
REG4	0x51	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R
REG5	0x54	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	0	0	0	0	0
REG5	0x55	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R
REG6	0x60	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	0	0	0	0	0
REG6	0x61	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R
REG7	0x64	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	0	0	0	0	0
REG7	0x65	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R

①: Default values of ACT8865QI303-T.

②: All bits are automatically cleared to default values when the input power is removed or falls below the system UVLO.

REGISTER AND BIT DESCRIPTIONS

Table 1:

Global Register Map

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	TRST	R/W	Reset Timer Setting. Defines the reset timeout threshold. See *nRSTO Output* section for more information.
SYS	0x00	[6]	nSYSMODE	R/W	SYSLEV Mode Select. Defines the response to the SYSLEV voltage detector, 1: Generate an interrupt when V_{VDDREF} falls below the programmed SYSLEV threshold, 0: automatic shutdown when V_{VDDREF} falls below the programmed SYSLEV threshold.
SYS	0x00	[5]	nSYSLEVMSK	R/W	System Voltage Level Interrupt Mask. Disabled interrupt by default, set to 1 to enable this interrupt. See the *Programmable System Voltage Monitor* section for more information
SYS	0x00	[4]	nSYSSTAT	R	System Voltage Status. Value is 1 when V_{VDDREF} is lower than the SYSLEV voltage threshold, value is 0 when V_{VDDREF} is higher than the system voltage detection threshold.
SYS	0x00	[3:0]	SYSLEV	R/W	System Voltage Detect Threshold. Defines the SYSLEV voltage threshold. See the *Programmable System Voltage Monitor* section for more information.
SYS	0x01	[7:6]	-	R	Reserved.
SYS	0x01	[5]	MSTROFF	R/W	Master Off Control. Set bit to 1 to turn off all regulators. The bit will be automatically cleared to 0 when nPBIN is asserted.
SYS	0x01	[4]	-	R	Reserved.
SYS	0x01	[3:1]	SCRATCH	R/W	Scratchpad Bits. Non-functional bits, maybe be used by user to store system status information. Volatile bits, which are cleared upon system shutdown.
SYS	0x01	[0]	SCRATCH	R/W	Scratchpad Bits. Non-functional bits, maybe be used by user to store system status information. Volatile bits, which are cleared upon system shutdown.
REG1	0x20	[7:6]	-	R	Reserved.
REG1	0x20	[5:0]	VSET1	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information.
REG1	0x21	[7:6]	-	R	Reserved.
REG1	0x21	[5:0]	VSET2	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG1	0x22	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x22	[6]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for regulator to operate 180° out of phase with the oscillator, clear bit to 0 for regulator to operate in phase with the oscillator.
REG1	0x22	[5]	MODE	R/W	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.
REG1	0x22	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG1, REG2, REG3 Turn-on Delay* section for more information.
REG1	0x22	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable to fault-interrupts, clear bit to 0 to disable fault-interrupts.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG1	0x22	[0]	OK	R/W	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x30	[7:6]	-	R	Reserved.
REG2	0x30	[5:0]	VSET1	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information.
REG2	0x31	[7:6]	-	R	Reserved.
REG2	0x31	[5:0]	VSET2	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG2	0x32	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG2	0x32	[6]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for regulator to operate 180° out of phase with the oscillator, clear bit to 0 for regulator to operate in phase with the oscillator.
REG2	0x32	[5]	MODE	R/W	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.
REG2	0x32	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG1, REG2, REG3 Turn-on Delay* section for more information.
REG2	0x32	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable to fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG2	0x32	[0]	OK	R/W	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG3	0x40	[7:6]	-	R	Reserved.
REG3	0x40	[5:0]	VSET1	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information.
REG3	0x41	[7:6]	-	R	Reserved.
REG3	0x41	[5:0]	VSET2	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG3	0x42	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG3	0x42	[6]	PWRSTAT	R/W	Configures regulator behavior with respect to the nPBIN input. Set bit to 0 to enable regulator when nPBIN is asserted.
REG3	0x42	[5]	MODE	R/W	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transition to power-savings mode under light-load conditions.
REG3	0x42	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG1, REG2, REG3 Turn-on Delay* section for more information.
REG3	0x42	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable to fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG3	0x42	[0]	OK	R/W	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG4	0x50	[7:6]	-	R	Reserved.
REG4	0x50	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG4	0x51	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG4	0x51	[6]	DIS	R/W	Output Discharge Control. When activated, discharges LDO output to GA through 1.5kΩ when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG4	0x51	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG4	0x51	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG4	0x51	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable to fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG4	0x51	[0]	OK	R/W	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG5	0x54	[7:6]	-	R	Reserved.
REG5	0x54	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG5	0x55	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG5	0x55	[6]	DIS	R/W	Output Discharge Control. When activated, discharges LDO output to GA through 1.5kΩ when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG5	0x55	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG5	0x55	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG5	0x55	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable to fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG5	0x55	[0]	OK	R/W	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG6	0x60	[7:6]	-	R	Reserved.
REG6	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG6	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG6	0x61	[6]	DIS	R/W	Output Discharge Control. When activated, discharges LDO output to GA through 1.5kΩ when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG6	0x61	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG6	0x61	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG6	0x61	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable to fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x61	[0]	OK	R/W	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG7	0x64	[7:6]	-	R	Reserved.
REG7	0x64	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG7	0x65	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.

REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG7	0x65	[6]	DIS	R/W	Output Discharge Control. When activated, discharges LDO output to GA through 1.5kΩ when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG7	0x65	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG7	0x65	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG7	0x65	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable to fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG7	0x65	[0]	OK	R/W	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.7		5.5	V
UVLO Threshold Voltage	V_{VDDREF} Rising	2.2	2.45	2.65	V
UVLO Hysteresis	V_{VDDREF} Falling		200		mV
Supply Current	REG1, REG2, REG3 Enabled. REG4 REG5, REG6 and REG7 Disabled		13.85		mA
	REG1, REG2, REG3, REG4, REG5, REG6 and REG7 Enabled		14		
Shutdown Supply Current	All Regulators Disabled		1.5	3.0	µA
Oscillator Frequency		1.8	2	2.2	MHz
Logic High Input Voltage①		1.4			V
Logic Low Input Voltage				0.4	V
Leakage Current	V_{nIRQ} = V_{nRSTO} = 4.2V			1	µA
Low Level Output Voltage②	I_{SINK} = 5mA			0.35	V
nRSTO Delay			64③		ms
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

①: PWRHLD, PWREN, VSEL are logic inputs.

②: nPBSTAT, nIRQ, nRSTO are open drain outputs.

③: Typical value shown. Actual value may vary from 56.3ms to 72.8ms.

STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO Hysteresis	Input Voltage Falling		100		mV
Quiescent Supply Current	Regulator Enabled		4.5	7.0	mA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	1	µA
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, I_{OUT} = 10mA	-1%	V_{NOM}①	1%	V
	V_{OUT} < 1.2V, I_{OUT} = 10mA	-2%	V_{NOM}①	2%	
Line Regulation	V_{VP} = Max(V_{NOM}① +1, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT} = 10mA to IMAX②		0.0017		%/mA
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2		%V_{NOM}
Oscillator Frequency	V_{OUT} ≥ 20% of V_{NOM}	1.8	2	2.2	MHz
	V_{OUT} = 0V		500		kHz
Soft-Start Period			400		µs
Minimum On-Time			75		ns
REG1					
Maximum Output Current		1.15			A
Current Limit		1.5	1.8	2.1	A
PMOS On-Resistance	I_{SW1} = -100mA		0.16		Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.16		Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 0 or 5.5V			1	µA
REG2					
Maximum Output Current		1.15			A
Current Limit		1.5	1.8	2.1	A
PMOS On-Resistance	I_{SW2} = -100mA		0.16		Ω
NMOS On-Resistance	I_{SW2} = 100mA		0.16		Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 0 or 5.5V			1	µA
REG3					
Maximum Output Current		1.30			A
Current Limit		1.7	2.1	2.5	A
PMOS On-Resistance	I_{SW3} = -100mA		0.16		Ω
NMOS On-Resistance	I_{SW3} = 100mA		0.16		Ω
SW3 Leakage Current	V_{VP3} = 5.5V, V_{SW3} = 0 or 5.5V		0	1	µA

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, C_{OUT4} = C_{OUT5} = 1.5µF, C_{OUT6} = C_{OUT7} = 3.3µF, LOWIQ[ ] = [0], T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, T_A = 25°C, I_{OUT} = 10mA	-1%	V_{NOM} ①	2%	V
	V_{OUT} < 1.2V, T_A = 25°C, I_{OUT} = 10mA	-2%	V_{NOM} ①	4%	
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.05		mV/V
	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V LOWIQ[ ] = [1]		0.5		
Load Regulation	I_{OUT} = 1mA to IMAX②		0.08		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		75		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		65		
Supply Current per Output	Regulator Enabled, LOWIQ[ ] = [0]		37	60	µA
	Regulator Enabled, LOWIQ[ ] = [1]		31	52	
	Regulator Disabled		0	1	
Soft-Start Period	V_{OUT} = 2.9V		140		µs
Power Good Threshold	V_{OUT} Rising		89		%
Power Good Hysteresis	V_{OUT} Falling		3		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		50		$µV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
REG4					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		90	180	mV
Maximum Output Current		320			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	400			mA
Stable C_{OUT4} Range		3.3		20	µF
REG5					
Dropout Voltage	I_{OUT} = 160mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		320			mA
Current Limit	V_{OUT} = 95% of regulation voltage	400			mA
Stable C_{OUT5} Range		3.3		20	µF
REG6					
Dropout Voltage	I_{OUT} = 160mA, V_{OUT} > 3.1V		90	180	mV
Maximum Output Current		320			mA
Current Limit	V_{OUT} = 95% of regulation voltage	400			mA
Stable C_{OUT6} Range		3.3		20	µF
REG7					
Dropout Voltage	I_{OUT} = 160mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		320			mA
Current Limit	V_{OUT} = 95% of regulation voltage	400			mA
Stable C_{OUT7} Range		3.3		20	µF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

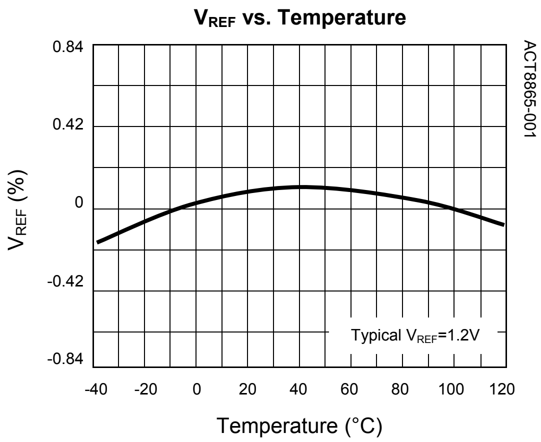
②: IMAX Maximum Output Current.

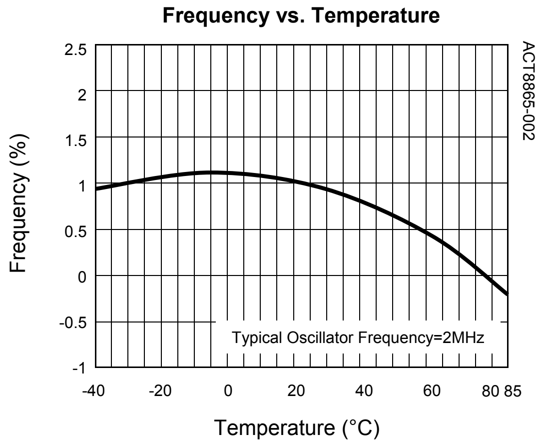
③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher)

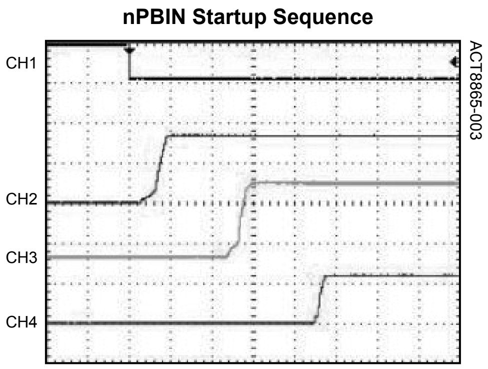
④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

TYPICAL PERFORMANCE CHARACTERISTICS

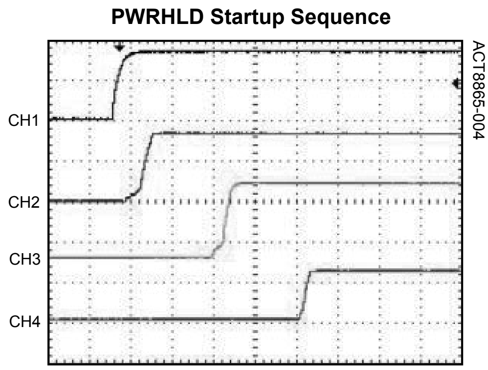
(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)



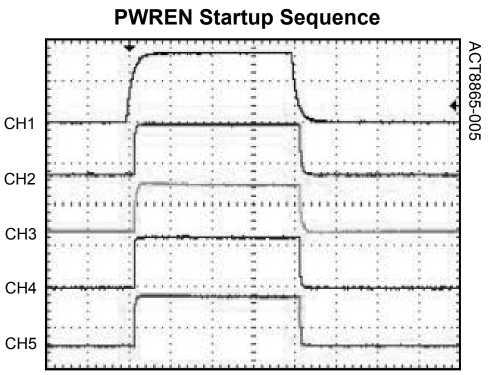




CH1: V_{nPBIN}, 2V/div
CH2: V_{OUT3}, 2V/div
CH3: V_{OUT1}, 1V/div
CH4: V_{OUT2}, 1V/div
TIME: 1ms/div



CH1: V_{PWRHLD}, 2V/div
CH2: V_{OUT3}, 2V/div
CH3: V_{OUT1}, 1V/div
CH4: V_{OUT2}, 1V/div
TIME: 1ms/div

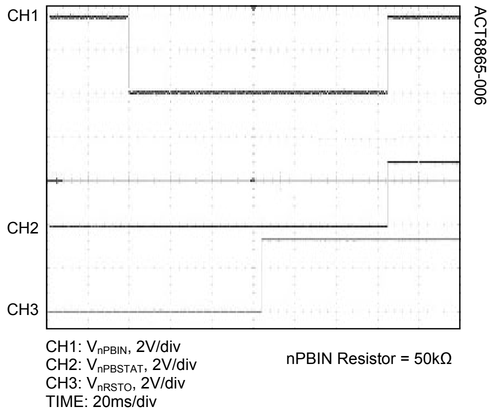


CH1: V_{PWREN}, 2V/div
CH2: V_{OUT4}, 500mV/div
CH3: V_{OUT5}, 500mV/div
CH4: V_{OUT6}, 500mV/div
CH5: V_{OUT7}, 500mV/div
TIME: 1ms/div

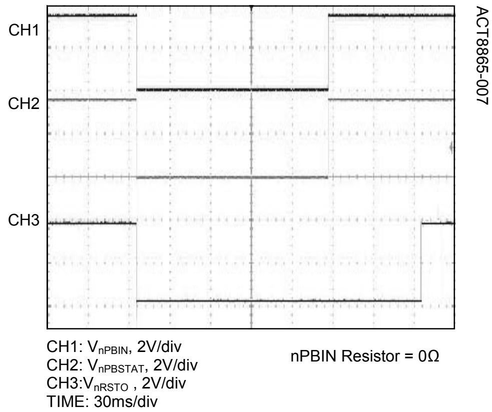
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

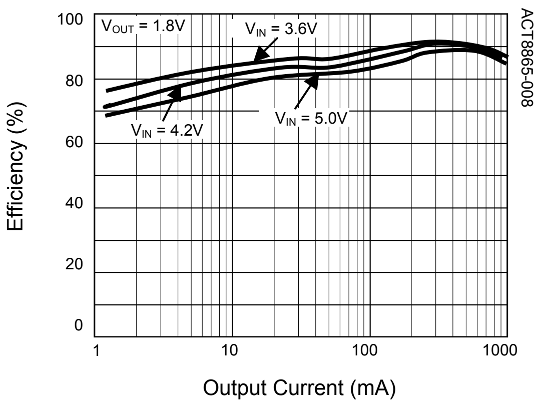
Push-Button Response (First Power-Up)



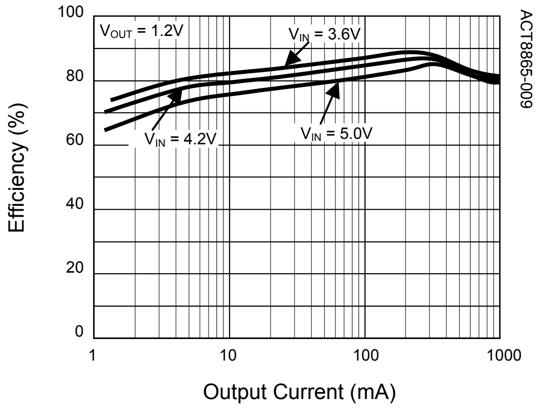
Manual Reset Response



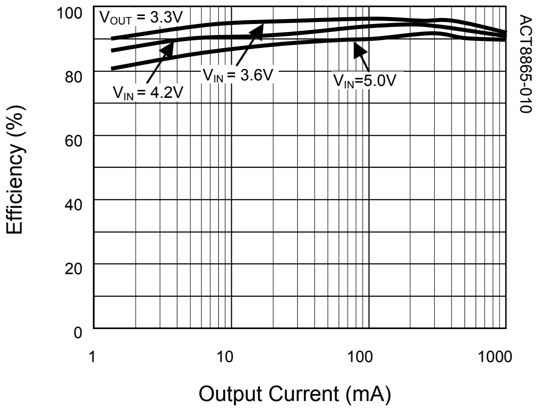
REG1 Efficiency vs. Output Current



REG2 Efficiency vs. Output Current

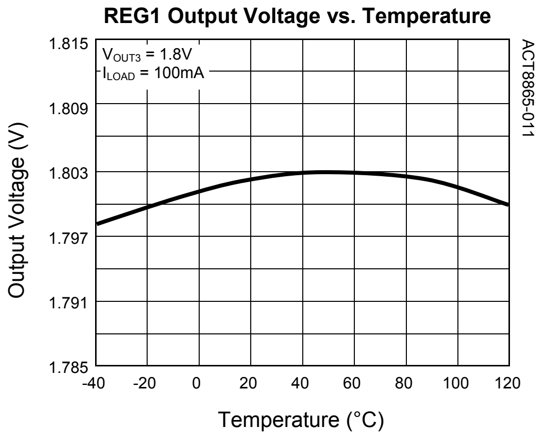


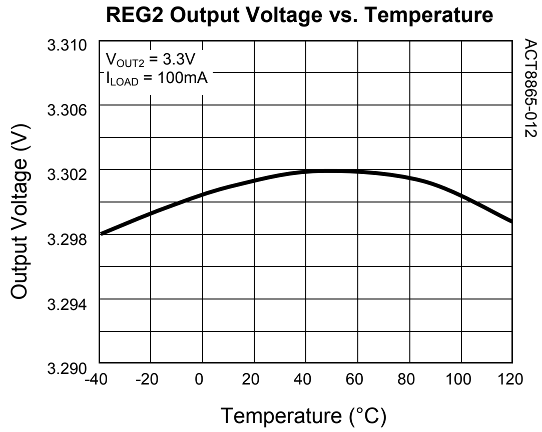
REG3 Efficiency vs. Output Current

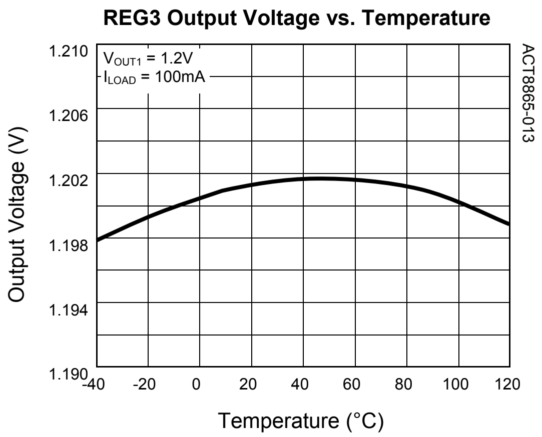


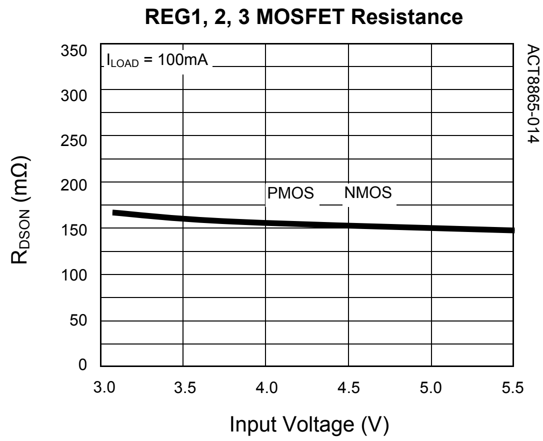
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)



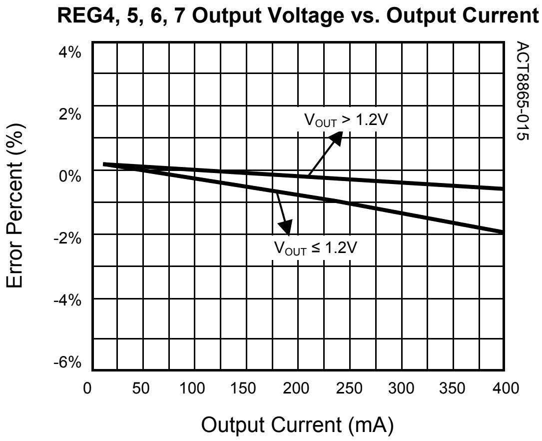


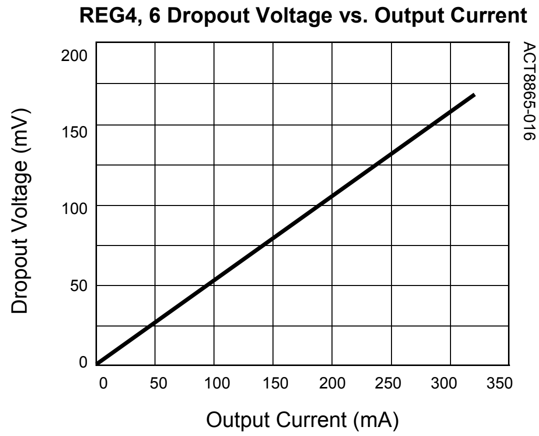


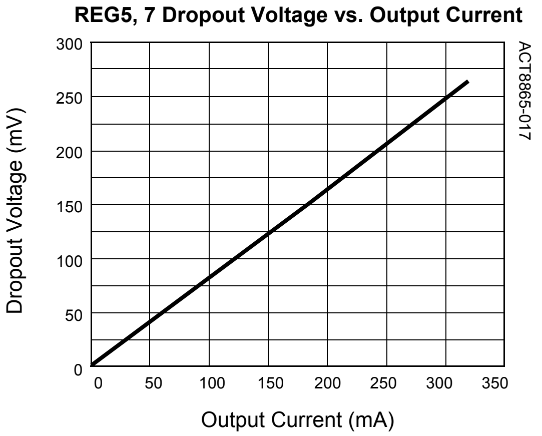


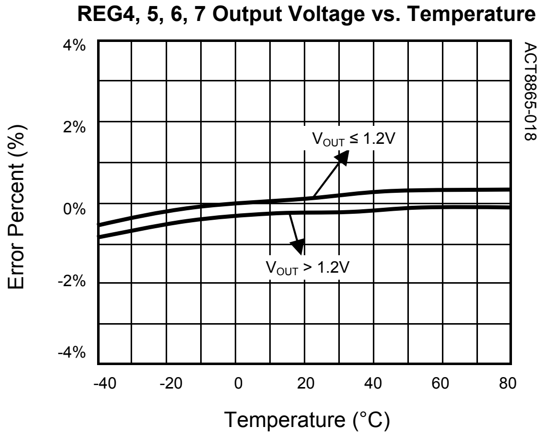
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

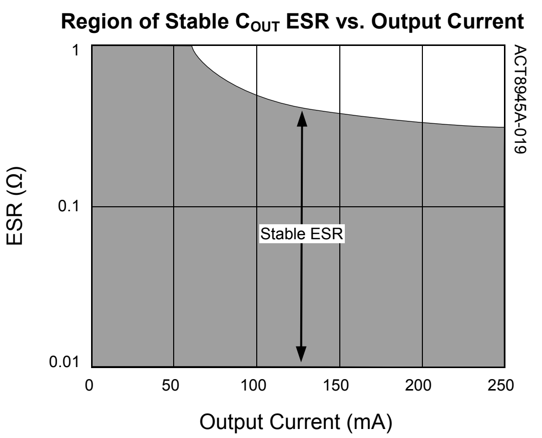
(T_A = 25°C, unless otherwise specified.)

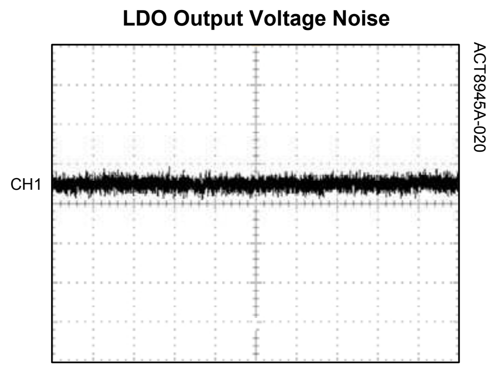












CH1: V_{OUTx}, 200µV/div (AC COUPLED)
TIME: 200ms/div

SYSTEM CONTROL INFORMATION

Interfacing with the Atmel SAMA5D3 Series & SAM9 Series Processors

The ACT8865 is optimized for use in applications using the following Atmel platforms: SAMA5D3 series and SAM9 series processors, supporting the power domains as shown in the following table:

Table 2:

ACT8865 and Atmel SAMA5D3 Series & SAM9 Series Power Domains

POWER DOMAIN	ACT8865 CHANNEL	TYPE	DEFAULT VOLTAGE	CURRENT CAPABILITY
VDDIODDR/VDDCORE_LPDDR	REG1	DC/DC	1.8V	1100mA
VDDCORE_GBIT ENET, VDDIO_LPDDR	REG2	DC/DC	1.2V①	1100mA
VDDIOP, VDDOSC, VDDUTMII, VDDIOM,10/100 ENET	REG3	DC/DC	3.3V	1200mA
VDDFUSE	REG4	LDO	0.6V	320mA
VDDANA	REG5	LDO	0.6V	320mA
Auxiliary 1	REG6	LDO	0.6V	320mA
Auxiliary 2	REG7	LDO	0.6V	320mA

①: V_{OUT2} = 1.2V @ VSEL=0 (SAMA5 series) and V_{OUT2} = 1.0V @ VSEL=VIN (SAM9 series)

SYSTEM CONTROL INFORMATION

Control Signals

Enable Inputs

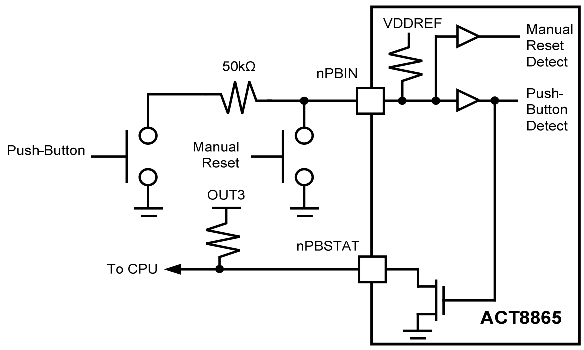
The ACT8865 features a variety of control inputs, which are used to enable and disable outputs depending upon the desired mode of operation. PWREN, PWRHLD are logic inputs, while nPBIN is a unique, multi-function input. Refer to the Processor Specification for a description of which channels are controlled by each input.

nPBIN Multi-Function Input

ACT8865 features the nPBIN multi-function pin, which combines system enable/disable control with a hardware reset function. Select either of the two pin functions by asserting this pin, either through a direct connection to GA, or through a 50kΩ resistor to GA, as shown in Figure 2.

Figure 2:

nPBIN Input



Manual Reset Function

The second major function of the nPBIN input is to provide a manual-reset input for the processor. To manually-reset the processor, drive nPBIN directly to GA through a low impedance (less than 2.5kΩ). When this occurs, nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires.

nPBSTAT Output

nPBSTAT is an open-drain output that reflects the state of the nPBIN input; nPBSTAT is asserted low whenever nPBIN is asserted, and is high-Z otherwise. This output is typically used as an interrupt signal to the processor, to initiate a software-programmable routine such as operating mode selection or to open a menu. Connect nPBSTAT to an appropriate supply voltage (typically OUT3) through a 10kΩ or greater resistor.

nRSTO Output

nRSTO is an open-drain output which asserts low upon startup or when manual reset is asserted via the nPBIN input. When asserted on startup, nRSTO remains low until reset time-out period expires after OUT3 reaches its power-OK threshold. When asserted due to manual-reset, nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires.

Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply (typically OUT3).

nIRQ Output

nIRQ is an open-drain output that asserts low any time an interrupt is generated. Connect a 10kΩ or greater pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor.

Many of the ACT8865's functions support interrupt-generation as a result of various conditions. These are typically masked by default, but may be unmasked via the I^2C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet.

Note that under some conditions a false interrupt may be generated upon initial startup. For this reason, it is recommended that the interrupt service routine check and validate nSYSLEVMSK[ ] and nFLTMSK[ ] bits before processing an interrupt generated by these bits. These interrupts may be validated by nSYSSTAT[ ], OK[ ] bits.

Push-Button Control

The ACT8865 is designed to initiate a system enable sequence when the nPBIN multi-function input is asserted. Once this occurs, a power-on sequence commences, as described below. The power-on sequence must complete and the microprocessor must take control (by asserting PWREN or PWRHLD) before nPBIN is de-asserted. If the microprocessor is unable to complete its power-up routine successfully before the user releases the push-button, the ACT8865 automatically shuts the system down. This provides protection against accidental or momentary assertions of the push-button. If desired, longer "push-and-hold" times can be implemented by simply adding an additional time delay before asserting PWREN or PWRHLD.

Control Sequences

The ACT8865 features a variety of control sequences that are optimized for supporting system enable and disable sequences of Atmel SAMA5D3 Series: SAMA5D[31/33/34/35/36] and SAM9 series: SAM9G[15/25/35/45/46], SAM9X[25/35], SAM9M[10/11], SAM9N[11/12] application processor.

Enabling/Disabling Sequence

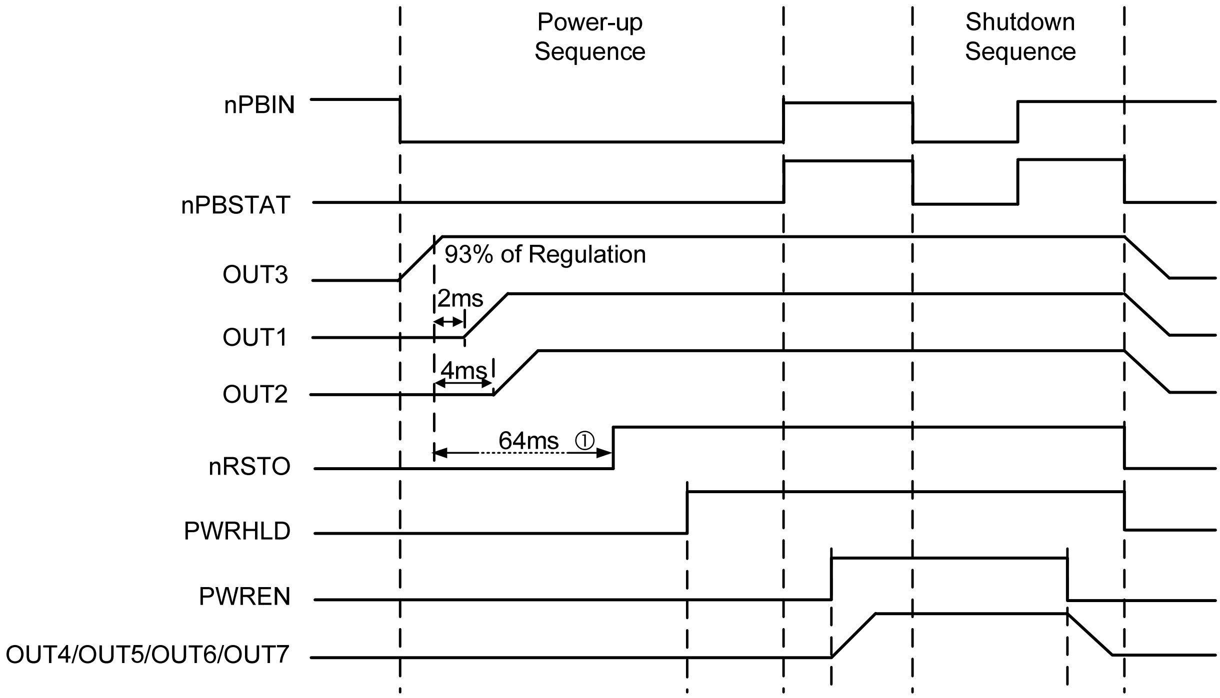
A typical enable sequence is initiated whenever nPBIN is asserted low via 50KΩ resistance. The enable sequence begins by enabling REG3. When REG3 reaches its power-OK threshold, nRSTO is asserted low, resetting the microprocessor. When REG3 reaches its power-OK threshold for 2ms①, REG1 is enabled. When REG3 reaches its power-OK threshold for 4ms①, REG2 is enabled. When REG3 is above its power-OK threshold when the reset timer expires, nRSTO is de-asserted, allowing the microprocessor to begin its boot sequence. REG4, REG5, REG6 and REG7 can be enabled or disabled by PWREN after system powers up.

During the boot sequence, the microprocessor must assert PWRHLD, holding the regulators to ensure that the system remains powered after nPBIN is released.

As with the enable sequence, a typical disable sequence is initiated when the user presses the push-button, which interrupts the processor via the nPBSTAT output. The actual disable sequence is completely software-controlled, but typically involved initiating various "clean-up" processes before finally set MSTROFF[] bit to 1 to shut the system down.

Figure 3:

ACT8865QI303-T Enable/Disable Sequence



①: Typical value shown, actual delay time may vary from (T-1ms) x 88% to T x 112%, where T is the typical delay time setting.

FUNCTIONAL DESCRIPTION

I^2C Interface

The ACT8865 features an I^2C interface that allows advanced programming capability to enhance overall system performance. To ensure compatibility with a wide range of system processors, the I^2C interface supports clock speeds of up to 400kHz ("Fast-Mode" operation) and uses standard I^2C commands. I^2C write-byte commands are used to program the ACT8865, and I^2C read-byte commands are used to read the ACT8865's internal registers. The ACT8865 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011011x].

SDA is a bi-directional data line and SCL is a clock input. The master device initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I^2C 2-wire serial interface, go to the NXP website: http://www.nxp.com.

Voltage Monitor and Interrupt

Programmable System Voltage Monitor

The ACT8865 features a programmable system-voltage monitor, which monitors the voltage at VDDREF and compares it to a programmable threshold voltage. The programmable voltage threshold is programmed by SYSLEV[3:0], as shown in Table 3.

SYSLEV[ ] is set to 3.0V by default. There is a 200mV rising hysteresis on SYSLEV[ ] threshold such that V_{VDDREF} needs to be 3.2V(typ) or higher in order to power up the IC.

The nSYSSTAT[ ] bit reflects the output of an internal voltage comparator that monitors VDDREF relative to the SYSLEV[ ] voltage threshold, the value of nSYSTAT[ ] = 1 when V_{VDDREF} is lower than the SYSLEV[ ] voltage threshold, and nSYSTAT[ ] = 0 when V_{VDDREF} is higher than the SYSLEV[ ] voltage threshold. Note that the SYSLEV[ ] voltage threshold is defined for falling voltages, and that the comparator produces about 200mV of hysteresis at VDDREF. As a result, once V_{VDDREF} falls below the SYSLEV threshold, its voltage must increase by more than about 200mV to clear that condition.

After the IC is powered up, the ACT8865 responds in one of two ways when the voltage at VDDREF falls below the SYSLEV[ ] voltage threshold:

1) If nSYSMODE[ ] = 1 (default case), when system voltage level interrupt is unmasked (nSYSLEVMSK[ ]=1) and V_{VDDREF} falls below the programmable threshold, the ACT8865 asserts nIRQ, providing a software "under-voltage alarm". The response to this interrupt is controlled by the CPU, but will typically initiate a controlled shutdown sequence either or alert the user that the battery is low. In this case the interrupt is cleared when V_{VDDREF} rises up again above the SYSLEV rising threshold and nSYSSTAT[ ] is read via I^2C.

2) If nSYSMODE[ ] = 0, when V_{VDDREF} falls below the programmable threshold the ACT8865 shuts down, immediately disabling all regulators. This option is useful for implementing a programmable "under-voltage lockout" function that forces the system off when the battery voltage falls below the SYSLEV threshold voltage. Since this option does not support a controlled shutdown sequence, it is generally used as a "fail-safe" to shut the system down when the battery voltage is too low.

Table 3:

SYSLEV Falling Threshold

SYSLEV[3:0]	SYSLEV Falling Threshold (Hysteresis = 200mV)
0000	2.3
0001	2.4
0010	2.5
0011	2.6
0100	2.7
0101	2.8
0110	2.9
0111	3.0
1000	3.1
1001	3.2
1010	3.3
1011	3.4
1100	3.5
1101	3.6
1110	3.7
1111	3.8

Thermal Shutdown

The ACT8865 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8865 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

STEP-DOWN DC/DC REGULATORS

General Description

The ACT8865 features three synchronous, fixed-frequency, current-mode PWM step down converters that achieve peak efficiencies of up to 97%. REG1 and REG2 are capable of supplying up to 1150mA of output current, while REG3 supports up to 1300mA. These regulators operate with a fixed frequency of 2MHz, minimizing noise in sensitive applications and allowing the use of small external components.

100% Duty Cycle Operation

Each regulator is capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Synchronous Rectification

REG1, REG2, and REG3 each feature integrated n-channel synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

When enabled, each output voltages tracks an internal 400μs soft-start ramp, minimizing input current during startup and allowing each regulator to power up in a smooth, monotonic manner that is independent of output load conditions.

Compensation

Each buck regulator utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 4.7μF ceramic capacitor is recommended for each regulator in most applications.

Output Capacitor Selection

For most applications, 22μF ceramic output capacitors are recommended for REG1/REG2/ REG3.

Despite the advantages of ceramic capacitors, care must be taken during the design process to ensure stable operation over the full operating voltage and temperature range. Ceramic capacitors are available in a variety of dielectrics, each of which exhibits different characteristics that can greatly affect performance over their temperature and voltage ranges.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications, as their characteristics are more stable over their operating ranges, and are highly recommended.

Inductor Selection

REG1, REG2, and REG3 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 2.2μH inductors, although inductors in the 1.5μH to 3.3μH range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%.

Enable / Disable Control

During normal operation, each buck may be enabled or disabled via the I^2C interface by writing to that regulator's ON[ ] bit. To enable the regulator set ON[ ] to 1, to disable the regulator clear ON[ ] to 0.

REG1, REG2, REG3 Turn-On Delay

Each of REG1/REG2/REG3 features a programmable Turn-On Delay which help ensure a reliable qualification. This delay is programmed by DELAY[2:0], as shown in Table 5.

Operating Mode

REG1, REG2, and REG3 each operate in fixed-frequency PWM mode at medium to heavy loads when MODE[ ] bit is set to 0, and transition to a proprietary power-saving mode at light loads in order to maximize standby battery life. In applications where low noise is critical, force fixed-frequency PWM operation across the entire load current range, at the expense of light-load efficiency, by setting the MODE[ ] bit to 1.

OK[ ] and Output Fault Interrupt

Each DC/DC features a power-OK status bit that can be read by the system microprocessor via the I^2C interface. If an output voltage is lower than the power-OK threshold, typically 7% below the programmed regulation voltage, that regulator's OK[ ] bit will be 0.

If a DC/DC's nFLTMSK[ ] bit is set to 1, the ACT8865 will interrupt the processor if that DC/DC's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until the OK[ ] bit has been read via I^2C.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design.

Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of via if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple via. The output node for each regulator should be connected to its corresponding OUTx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

Table 4:

REGx/VSET[ ] Output Voltage Setting

REGx/VSET[2:0]	REGx/VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.600	0.800	1.000	1.200	1.600	2.000	2.400	3.200
001	0.625	0.825	1.025	1.250	1.650	2.050	2.500	3.300
010	0.650	0.850	1.050	1.300	1.700	2.100	2.600	3.400
011	0.675	0.875	1.075	1.350	1.750	2.150	2.700	3.500
100	0.700	0.900	1.100	1.400	1.800	2.200	2.800	3.600
101	0.725	0.925	1.125	1.450	1.850	2.250	2.900	3.700
110	0.750	0.950	1.150	1.500	1.900	2.300	3.000	3.800
111	0.775	0.975	1.175	1.550	1.950	2.350	3.100	3.900

LOW-NOISE, LOW-DROPOUT LINEAR REGULATORS

General Description

REG4, REG5, REG6 and REG7 are low-noise, low-dropout linear regulators (LDOs) that supply up to 320mA. Each LDO has been optimized to achieve low noise and high-PSRR, achieving more than 65dB PSRR at frequencies up to 10kHz.

Output Current Limit

Each LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal and moderate overload conditions, the regulators can support more than their rated output currents. During extreme overload conditions, however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC.

Compensation

The LDOs are internally compensated and require very little design effort, simply select input and output capacitors according to the guidelines below.

Input Capacitor Selection

Each LDO requires a small 1µF ceramic output capacitor for stability. For best performance, each output capacitor should be connected directly between the output and GA pins, as close to the output as possible, and with a short, direct connection. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Output Capacitor Selection

Each LDO requires a small 3.3µF ceramic output capacitor for stability. For best performance, each output capacitor should be connected directly between the output and GA pins, as close to the output as possible, and with a short, direct connection. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Configuration Options

Output Voltage Programming

By default, each LDO powers up and regulates to its default output voltage. Once the system is enabled, each output voltage may be independently programmed to a different value by writing to the regulator's VSET[ ] register via the I^2C serial interface as shown in Table 4.

Enable / Disable Control

During normal operation, each LDO may be enabled or disabled via the I^2C interface by writing to that LDO's ON[ ] bit. To enable the LDO set ON[ ] to 1, to disable the LDO clear ON[ ] to 0.

REG4, REG5, REG6, REG7 Turn-on Delay

Each of REG4, REG5, REG6 and REG7 features a programmable Turn-on Delay which help ensure a reliable qualification. This delay is programmed by DELAY[2:0], as shown in Table 5.

Table 5:

REGx/DELAY[ ] Turn-On Delay

DELAY[2]	DELAY[1]	DELAY[0]	TURN-ON DELAY
0	0	0	0 ms
0	0	1	2 ms
0	1	0	4 ms
0	1	1	8 ms
1	0	0	16 ms
1	0	1	32 ms
1	1	0	64 ms
1	1	1	128 ms

Output Discharge

Each of the ACT8865's LDOs features an optional output discharge function, which discharges the output to ground through a 1.5kΩ resistance when the LDO is disabled. This feature may be enabled or disabled by setting DIS[ ] via; set DIS[ ] to 1 to enable this function, clear DIS[ ] to 0 to disable it.

Low-Power Mode

Each of ACT8865's LDOs features a LOWIQ[ ] bit which, when set to 1, reduces the LDO's quiescent current by about 16%, saving power and extending battery lifetime.

OK[ ] and Output Fault Interrupt

Each LDO features a power-OK status bit that can be read by the system microprocessor via the interface. If an output voltage is lower than the power-OK threshold, typically 11% below the programmed regulation voltage, the value of that regulator's OK[ ] bit will be 0.

If a LDO's nFLTMSK[ ] bit is set to 1, the ACT8865 will interrupt the processor if that LDO's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until the OK[ ] bit has been read via I^2C.

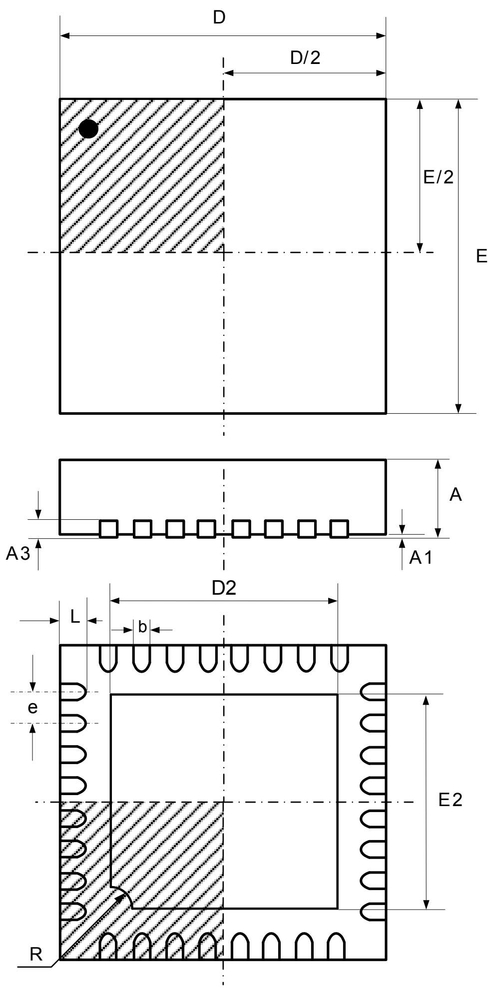
PCB Layout Considerations

PCB Layout Considerations The ACT8865's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs.

REFBP is a filtered reference noise, and internally has a direct connection to the linear regulator controller. Any noise injected onto REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of via whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

TQFN44-32 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.200		0.008	
b	0.150	0.250	0.006	0.010
D	4.000 TYP		0.158 TYP	
E	4.000 TYP		0.158 TYP	
D2	2.550	2.800	0.100	0.110
E2	2.550	2.800	0.100	0.110
e	0.400 TYP		0.016 TYP	
L	0.250	0.450	0.010	0.018
R	0.250		0.010	

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev PrB	20 Jun 2013	Initial Release.
Rev 0	18 Jul 2013	Updated Table 2.
Rev 1	01 Aug 2013	Updated general description and typical application diagram.