Wide Dynamic Range Microphone with PDM Digital Output

GENERAL DESCRIPTION

The ADMP621*is a high sound pressure level (SPL), ultralow noise, low power, digital output, bottom ported omnidirectional MEMS microphone. This microphone clips at 133 dB SPL, which is useful for clearly capturing audio in loud environments. The ADMP621 consists of a MEMS microphone element and an impedance converter amplifier followed by a fourth-order Σ-Δ modulator. The digital interface allows the pulse density modulated (PDM) output of two microphones to be time multiplexed on a single data line using a single clock. The ADMP621 is pin compatible with the ADMP421 and ADMP521 microphones, providing an easy upgrade path.

The ADMP621 has a high SNR of 65 dBA and sensitivity of −46 dBFS. The ADMP621 has an extended wideband frequency response, resulting in natural sound with high intelligibility. Low current consumption and a sleep mode at less than 5.5 µA enables long battery life for portable applications.

The ADMP621 is available in a thin 4 × 3 × 1 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation.

**Protected by U.S. Patents 7,449,356; 7,825,484; 7,885,423; and 7,961,897. Other patents are pending.*

APPLICATIONS

- Tablet Computers
- Notebook PCs
- Smartphones
- Microphone Arrays
- Teleconferencing Systems
- Digital Still and Video Cameras
- Bluetooth Headsets
- Security and Surveillance

FEATURES

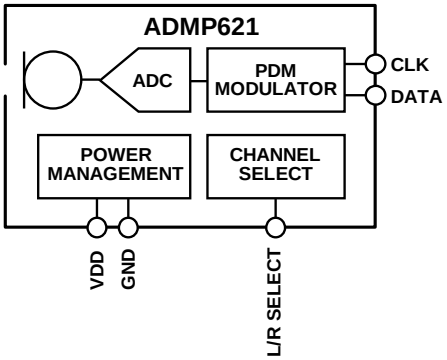
- High Acoustic Overload Point of 133 dB SPL
- Small, Thin 4 × 3 × 1 mm Surface-Mount Package
- Omnidirectional Response
- Very High Signal-to-Noise Ratio (SNR): 65 dBA
- Sensitivity of −46 dBFS
- Extended Frequency Response from 45 Hz to >20 kHz
- Low Current Consumption: 1.2 mA
- Sleep Mode for Extended Battery Life: 5.5 µA
- High Power Supply Rejection (PSR): −100 dBFS
- Fourth-Order Σ-Δ Modulator
- Digital Pulse Density Modulation (PDM) Output
- Compatible with Sn/Pb and Pb-Free Solder Processes
- RoHS/WEEE Compliant

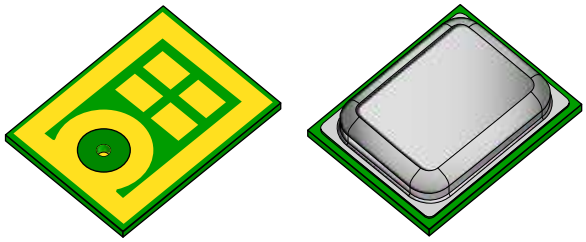
ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ADMP621ACEZ-RL	−40°C to +85°C*	CE-5-1
ADMP621ACEZ-RL7	−40°C to +85°C†	CE-5-1
EVAL-ADMP621Z-FLEX	—	—

* – 13” Tape and Reel † – 7” Tape and Reel

FUNCTIONAL BLOCK DIAGRAM





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SPECIFICATIONS

TABLE 1. ELECTRICAL CHARACTERISTICS

(T_A = −40 to 85°C, VDD = 1.8 to 3.3 V, CLK = 3.072 MHz, C_{LOAD} = 30 pF, unless otherwise noted. All minimum and maximum specifications are guaranteed across temperature, voltage, and clock frequency specified in Table 1 and Table 2, unless otherwise noted. Typical specifications are not guaranteed.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PERFORMANCE							
Directionality				Omni			
Output Polarity		Input acoustic pressure vs. output data		Inverted			
Sensitivity		1kHz, 94 dB SPL	−48	−46	−44	dBFS	1, 2
Signal-to-Noise Ratio (SNR)		20 Hz to 20 kHz, A-weighted		65		dBA	
Equivalent Input Noise (EIN)		20 Hz to 20 kHz, A-weighted		29		dBA SPL	
Acoustic Dynamic Range Digital Dynamic Range		Derived from EIN and acoustic overload point		104		dB	2
		Derived from EIN and full-scale acoustic level		111		dB	
Frequency Response		Low frequency −3 dB point		45		Hz	3
		High frequency −3 dB point		>20		kHz	
Total Harmonic Distortion (THD)		105 dB SPL		0.35	1	%	
Power Supply Rejection (PSR)		217 Hz, 100 mV p-p square wave superimposed on VDD = 1.8 V, A-weighted		−100		dBFS	
Power Supply Rejection—Swept Sine		1 kHz sine wave		−113		dBFS	
Acoustic Overload Point		10% THD		133		dB SPL	
Full-Scale Acoustic Level		0 dBFS output		140		dB SPL	
POWER SUPPLY							
Supply Voltage (V_{DD})			1.62		3.63	V	
Supply Current (I_S)							
V_{DD} = 1.8 V	Normal Mode			1.2	1.5	mA	
	Sleep Mode				5.5	µA	4
V_{DD} = 3.3 V	Normal Mode			1.3	1.6	mA	
	Sleep Mode				8	µA	4
DIGITAL INPUT/OUTPUT CHARACTERISTICS							
Input Voltage High (V_{IH})			0.65 x V_{DD}			V	
Input Voltage Low (V_{IL})					0.35 x V_{DD}	V	
Output Voltage High (V_{OH})		I_{LOAD} = 0.5 mA	0.7 x V_{DD}	V_{DD}		V	
Output Voltage Low (V_{OL})		I_{LOAD} = 0.5 mA		0	0.3 x V_{DD}	V	
Output DC Offset		Percent of full scale		3		%	
Latency				<30		µs	
Noise Floor		20 Hz to 20 kHz, A-weighted		−111		dBFS	

Note 1: Sensitivity is relative to the RMS level of a sine wave with positive amplitude equal to 100% logical 1s density and negative amplitude equal to 0% logical 1s density.

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Note 2: The ±2 dB sensitivity specification is valid for CLK = 3.072 MHz. At lower clock frequencies, the minimum and maximum specifications are −49 dBFS and −43 dBFS, respectively.
Note 3: See Figure 4 and Figure 5.
Note 4: The microphone enters sleep mode when the clock frequency is less than 1 kHz.

TABLE 2. TIMING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SLEEP MODE						
Sleep Time	Time from CLK falling < 1 kHz		30		µs	1
Wake-Up Time	Time from CLK rising > 1 kHz to output within 3 dB of final sensitivity, power on		10		ms	1
INPUT						
t_{CLKIN}	Input clock period	270		1000	ns	
Clock Frequency (CLK)		1.0	3.072	3.6	MHz	1
Clock Duty Cycle		40		60	%	
OUTPUT						
T_{1OUTEN}	DATA1 (right) driven after falling clock edge	31			ns	
$T_{1OUTDIS}$	DATA1 (right) disabled after rising clock edge	5		23	ns	
T_{2OUTEN}	DATA2 (left) driven after rising clock edge	31			ns	
$T_{2OUTDIS}$	DATA2 (left) disabled after falling clock edge	5		26	ns	

Note 1: The microphone operates at any clock frequency between 1.0 MHz and 3.6 MHz. Some specifications may not be guaranteed at frequencies other than 3.072 MHz.

TIMING DIAGRAM

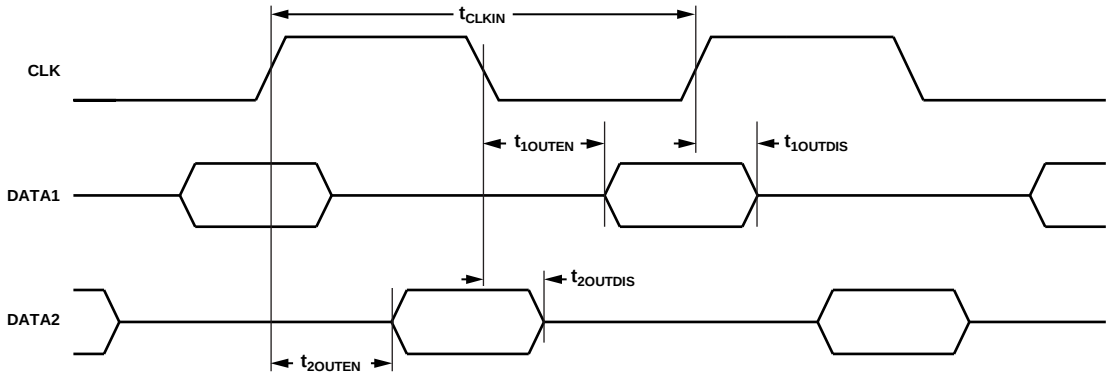

Figure 1. Pulse Density Modulated Output Timing

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ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 3. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage (VDD)	−0.3 V to +3.63 V
Digital Pin Input Voltage	−0.3 V to (VDD) + 0.3 V or 3.63 V, whichever is less
Sound Pressure Level	160 dB
Mechanical Shock	10,000 *g*
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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SOLDERING PROFILE

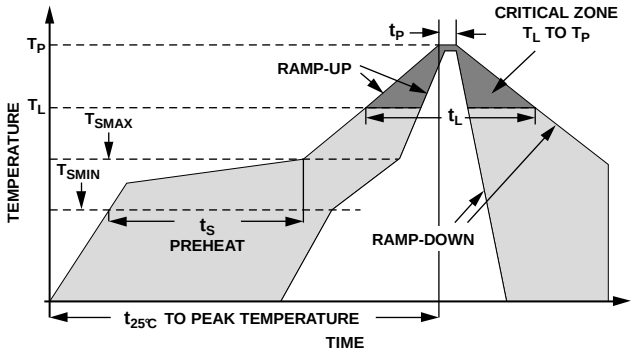

Figure 2. Recommended Soldering Profile Limits

TABLE 4. RECOMMENDED SOLDERING PROFILE

PROFILE FEATURE		Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)		1.25°C/sec max	1.25°C/sec max
Preheat	Minimum Temperature (T_{SMIN})	100°C	100°C
	Minimum Temperature (T_{SMIN})	150°C	200°C
	Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)		1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)		45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)		183°C	217°C
Peak Temperature (T_P)		215°C +3°C/−3°C	260°C +0°C/−5°C
Time Within +5°C of Actual Peak Temperature (t_P)		20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		3°C/sec max	3°C/sec max
Time +25°C ($t_{25°C}$) to Peak Temperature		5 min max	5 min max

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

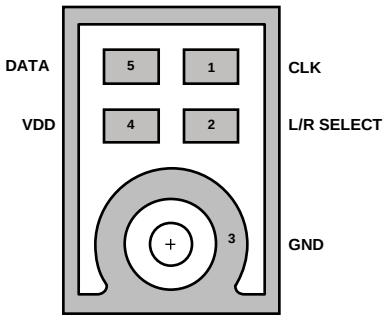

Figure 3. Pin Configuration

TABLE 5. PIN FUNCTION DESCRIPTIONS

PIN	NAME	FUNCTION
1	CLK	Clock Input to Microphone
2	L/R SELECT	Left Channel or Right Channel Select: DATA 1 (right): L/R SELECT tied to GND DATA 2 (left): L/R SELECT tied to VDD
3	GND	Ground
4	VDD	Power Supply. For best performance and to avoid potential parasitic artifacts, place a 0.1 µF (100 nF) ceramic type X7R capacitor between Pin 4 (VDD) and ground. Place the capacitor as close to Pin 4 as possible.
5	DATA	Digital Output Signal (DATA1 or DATA2)

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TYPICAL PERFORMANCE CHARACTERISTICS

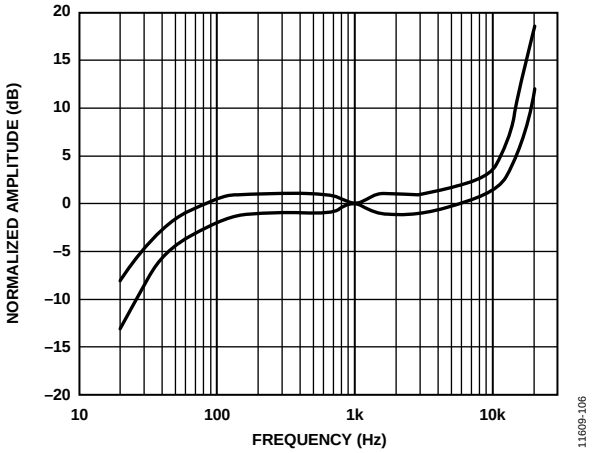

Figure 4. Frequency Response Mask

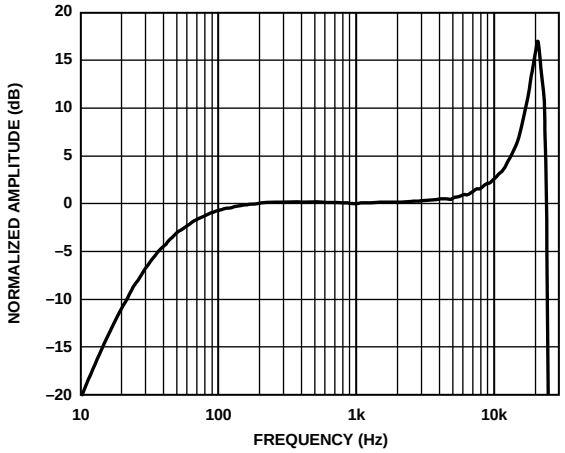

Figure 5. Typical Frequency Response (Measured)

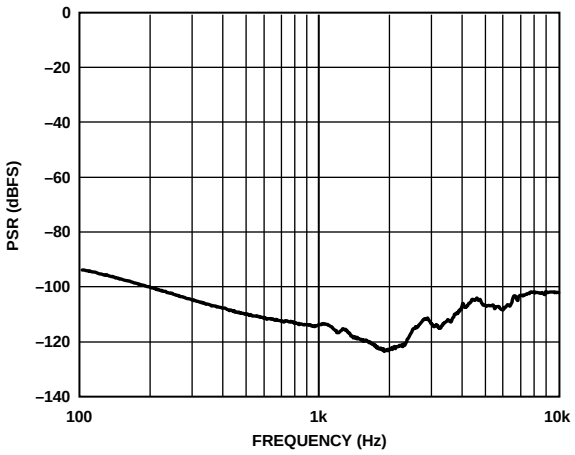

Figure 6. PSR vs. Frequency, 100 mV p-p Swept Sine Wave

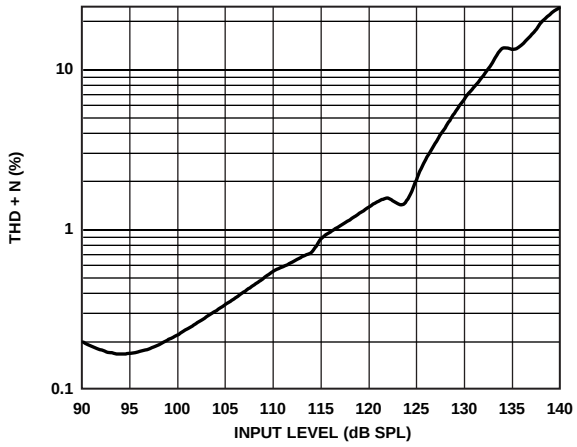

Figure 7. Total Harmonic Distortion + Noise (THD+N) vs. Input SPL

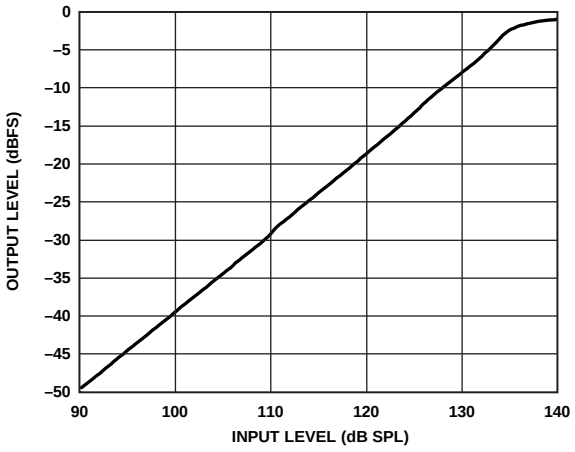

Figure 8. Linearity

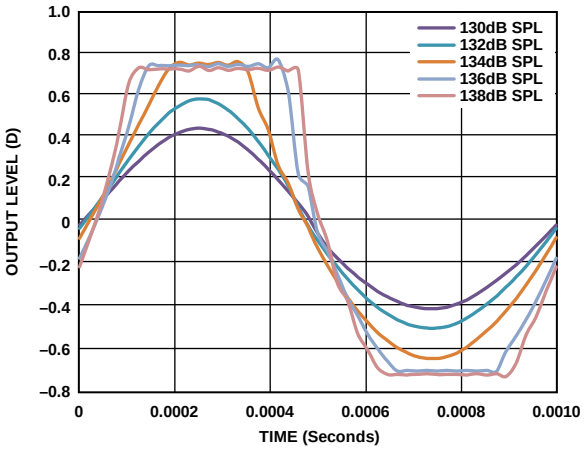

Figure 9. Clipping Characteristics

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THEORY OF OPERATION

PDM DATA FORMAT

The output from the DATA pin of the ADMP621 is in pulse density modulated (PDM) format. This data is the 1-bit output of a fourth-order Σ-Δ modulator. The data is encoded so that the left channel is clocked on the falling edge of CLK, and the right channel is clocked on the rising edge of CLK. After driving the DATA signal high or low in the appropriate half frame of the CLK signal, the DATA driver of the microphone tristates. In this way, two microphones, one set to the left channel and the other to the right, can drive a single DATA line. See Figure 1 for a timing diagram of the PDM data format; the DATA1 and DATA2 lines shown in this figure are two halves of the single physical DATA signal. Figure 10 shows a diagram of the two stereo channels sharing a common DATA line.

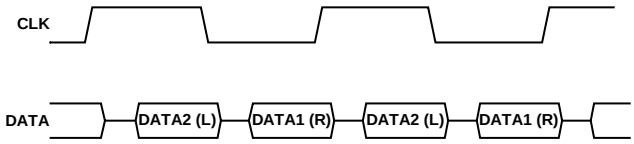

Figure 10. Stereo PDM Format

If only one microphone is connected to the DATA signal, the output is only clocked on a single edge (Figure 11). For example, a left channel microphone is never clocked on the rising edge of CLK. In a single microphone application, each bit of the DATA signal is typically held for the full CLK period until the next transition because the leakage of the DATA line is not enough to discharge the line while the driver is tristated.

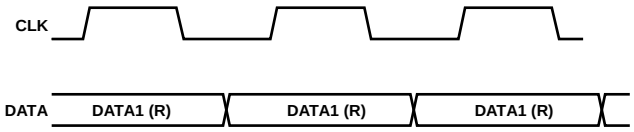

Figure 11. Mono PDM Format

See Table 6 for the channel assignments according to the logic level on the L/R SELECT pin.

TABLE 6. ADMP621 CHANNEL SETTING

L/R SELECT Pin Setting	Channel
Low (tie to GND)	Right (DATA1)
High (tie to VDD)	Left (DATA2)

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For PDM data, the density of the pulses indicates the signal amplitude. A high density of high pulses indicates a signal near positive full scale, and a high density of low pulses indicates a signal near negative full scale. A perfect zero (DC) audio signal shows an alternating pattern of high and low pulses.

The output PDM data signal has a small DC offset of about 3% of full scale. A high-pass filter in the codec that is connected to the digital microphone and does not affect the performance of the microphone typically removes this DC signal.

PDM MICROPHONE SENSITIVITY

The sensitivity of a PDM output microphone is specified with the unit dBFS (decibels relative to digital full scale). A 0 dBFS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure 12). This measurement convention also means that signals with a different crest factor may have an RMS level higher than 0 dBFS. For example, a full-scale square wave has an RMS level of 3 dBFS.

This definition of a 0 dBFS signal must be understood when measuring the sensitivity of the ADMP621. A 1 kHz sine wave at a 94 dB SPL acoustic input to the ADMP621 results in an output signal with a −46 dBFS level. The output digital word peaks at −46 dB below the digital full-scale level. A common misunderstanding is that the output has an RMS level of −49 dBFS; however, this is not true because of the definition of the 0 dBFS sine wave.

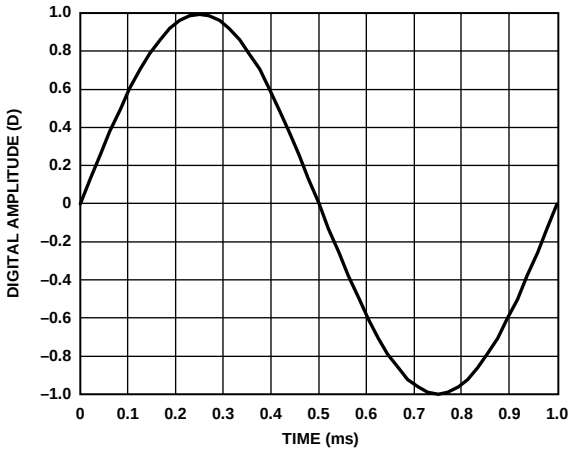

Figure 12. 1 kHz, 0 dBFS Sine Wave

There is not a commonly accepted unit of measurement to express the instantaneous level, as opposed to the RMS level of the signal, of a digital signal output from the microphone. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale. In this case, a −46 dBFS sine wave has peaks at 0.005 D.

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DYNAMIC RANGE CONSIDERATIONS

The full-scale digital output (0 dBFS) of the ADMP621 is mapped to an acoustic input of 140 dB SPL. The microphone clips (THD = 10%) at 133 dB SPL (see Figure 7); however, it continues to output an increasingly distorted signal above that point. The peak output level, which is controlled by the modulator, limits at about −3 dBFS (see Figure 8).

To fully use the 111 dB digital dynamic range of the output data of the ADMP621 in a design, the digital signal processor (DSP), analog-to-digital converter (ADC), or codec circuit following it must be chosen carefully. The decimation filter that inputs the PDM signal from the ADMP621 must have a dynamic range sufficiently better than the dynamic range of the microphone so that the overall noise performance of the system is not degraded. If the decimation filter has a dynamic range of 10 dB better than the microphone (121 dB), the overall system noise only degrades by 0.4 dB.

CONNECTING PDM MICROPHONES

A PDM output microphone is typically connected to a codec with a dedicated PDM input. This codec separately decodes the left and right channels and filters the high sample rate modulated data back to the audio frequency band. This codec also generates the clock for the PDM microphones or is synchronous with the source that is generating the clock. Figure 13 and Figure 14 show mono and stereo connections of the ADMP621 to a codec. The mono connection shows an ADMP621 set to output data on the right channel. To output on the left channel, tie the L/R SELECT pin to VDD instead of tying it to GND.

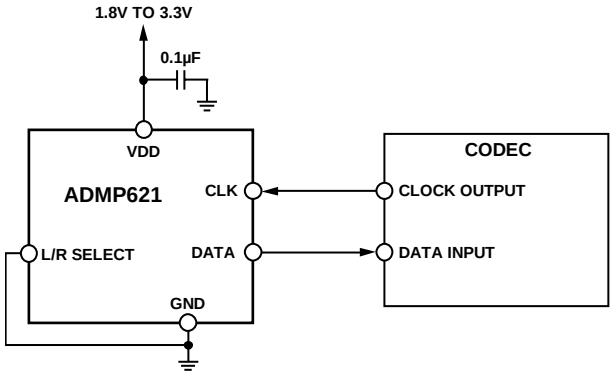

Figure 13. Mono PDM Microphone (Right Channel) Connection to Codec

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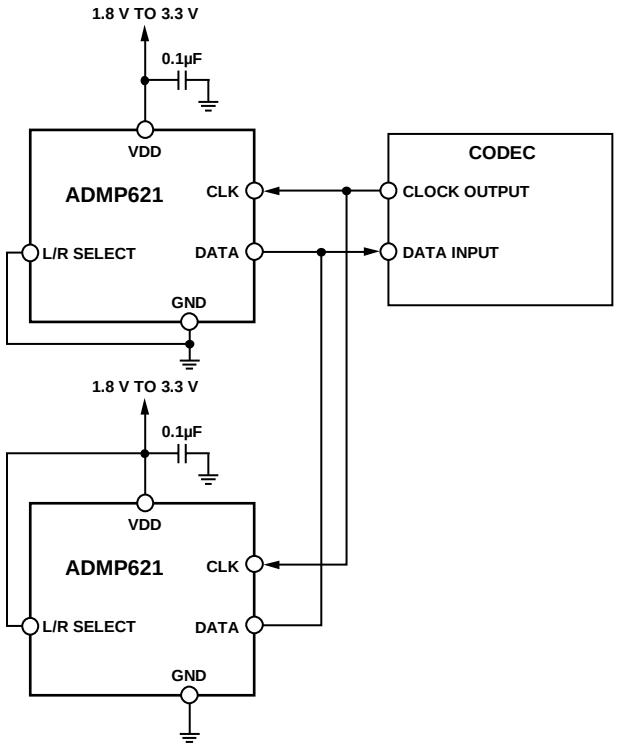

Figure 14. Stereo PDM Microphone Connection to Codec

Decouple the VDD pin of the ADMP621 to GND with a 0.1 µF capacitor. Place this capacitor as close to VDD as the printed circuit board (PCB) layout allows.

Do not use a pull-up or pull-down resistor on the PDM data signal line because it can pull the signal to an incorrect state during the period that the signal line is tristated.

The DATA signal does not need to be buffered in normal use when the ADMP621 microphone(s) is placed close to the codec on the PCB. If the DATA signal must be driven over a long cable (>15 cm) or other large capacitive load, a digital buffer may be required. Only use a signal buffer on the DATA line when one microphone is in use or after the point where two microphones are connected (see Figure 15). The DATA output of each microphone in a stereo configuration cannot be individually buffered because the two buffer outputs cannot drive a single signal line. If a buffer is used, take care to select one with low propagation delay so that the timing of the data connected to the codec is not corrupted.

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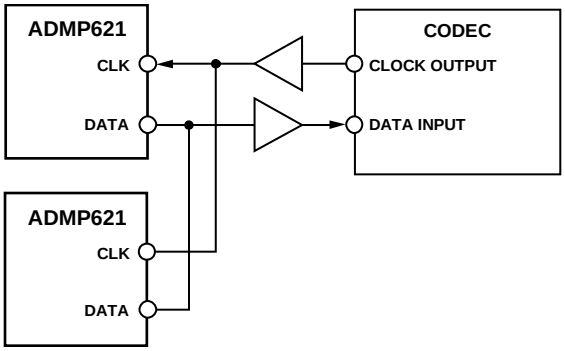

Figure 15. Buffered Connections Between Stereo ADMP621s and a Codec

When long wires are used to connect the codec to the ADMP621, a source termination resistor can be used on the clock output of the codec instead of a buffer to minimize signal overshoot or ringing. Match the value of this resistor to the characteristic impedance of the CLK trace on the PCB. Depending on the drive capability of the codec clock output, a buffer may still be needed, as shown in Figure 15.

SLEEP MODE

The microphone enters sleep mode when the clock frequency falls below 1 kHz. In this mode, the microphone data output is in a high impedance state. The current consumption in sleep mode is less than 5.5 µA.

The ADMP621 enters sleep mode within 1ms of the clock frequency falling below 1 kHz. The microphone wakes up from sleep mode and begins to output data 32,768 cycles after the clock becomes active. For a 3.072 MHz clock, the microphone starts to output data in 10.7 ms. For a 2.4 MHz clock, the microphone starts to output data in 13.7 ms. The wake-up time, as specified in Table 2, indicates the time from when the clock is enabled to when the ADMP621 outputs data within 3 dB of its settled sensitivity.

START-UP TIME

The start-up time of the ADMP621 from when the clock is active is the same as the wake-up time. The microphone starts up 32,768 cycles after the clock is active.

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SUPPORTING DOCUMENTS

For additional information, see the following documents.

EVALUATION BOARD USER GUIDE

UG-326 PDM Digital Output MEMS Microphone Evaluation Board

CIRCUIT NOTE

CN-0078 High Performance Digital MEMS Microphone Simple Interface to a SigmaDSP Audio Codec

APPLICATION NOTES

AN-1003 Recommendations for Mounting and Connecting the Invensense, Bottom-Ported MEMS Microphones
AN-1068 Reflow Soldering of the MEMS Microphone
AN-1112 Microphone Specifications Explained
AN-1124 Recommendations for Sealing Invensense, Bottom-Port MEMS Microphones from Dust and Liquid Ingress
AN-1140 Microphone Array Beamforming

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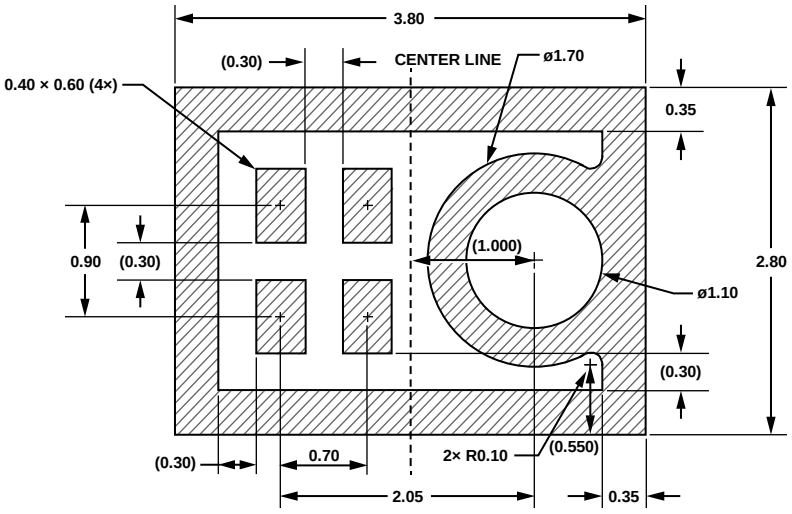
PCB DESIGN AND LAND PATTERN LAYOUT

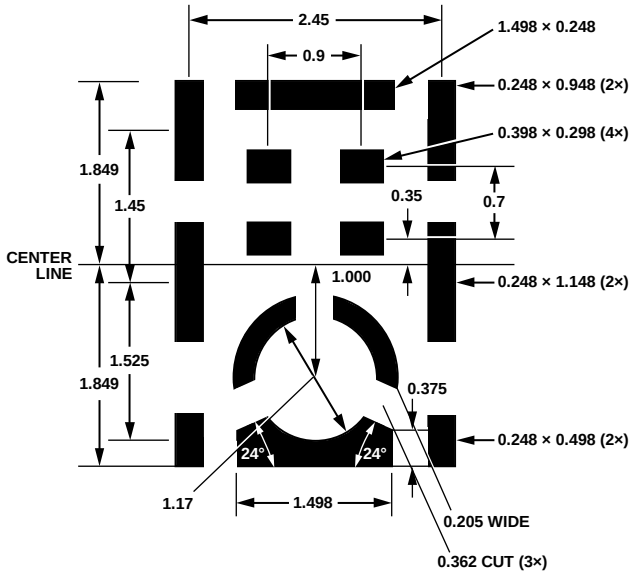
The recommended PCB land pattern for the ADMP621 must be laid out to a 1:1 ratio to the solder pads on the microphone package, as shown in Figure 16. Avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 17.

The response of the ADMP621 is not affected by the PCB hole size as long as the hole is not smaller than the sound port of the microphone (0.25 mm, or 0.010 inch, in diameter). A 0.5 mm to 1 mm (0.020 inch to 0.040 inch) diameter for the hole is recommended. Take care to align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the microphone performance as long as the holes are not partially or completely blocked.



Dimensions shown in millimeters

Figure 16. Recommended PCB Land Pattern Layout



Dimensions shown in millimeters

Figure 17. Suggested Solder Paste Stencil Pattern Layout

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ALTERNATIVE PCB LAND PATTERNS

The standard PCB land pattern of the ADMP621 has a solid rectangle around the edge of the footprint that can make routing the microphone signals more difficult in some board designs. This rectangle is used to improve the radio frequency (RF) immunity performance of the ADMP621; however, it is not necessary to have this full rectangle connected for electrical functionality. If a design can tolerate reduced RF immunity, this rectangle can either be broken or removed completely from the PCB footprint. Figure 18 shows an example PCB land pattern with no enclosing rectangle around the edge of the part, and Figure 19 shows an example PCB land pattern with the rectangle broken on two sides so that the inner pads can be more easily routed on the PCB.

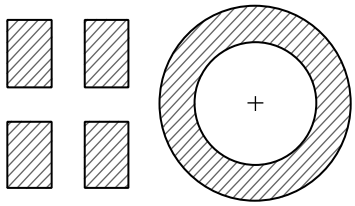

Figure 18. Example PCB Land Pattern with No Enclosing Rectangle

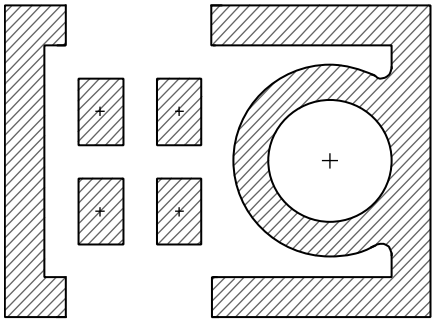

Figure 19. Example PCB Land Pattern with Broken Enclosing Rectangle

Note that in both of these patterns, the solid ring around the sound port is still present; this ring is needed to ground the microphone and for acoustic performance. The pad on the package connected to this ring is ground and still needs a solid electrical connection to the PCB ground. If a pattern like one of these two examples is used on a PCB, take care that the unconnected rectangle on the bottom of the ADMP621 is not placed directly over any exposed copper. This ring on the microphone is still at ground, and any PCB traces routed underneath it must be properly masked to avoid short circuits.

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PCB MATERIAL AND THICKNESS

The performance of the ADMP621 is not affected by PCB thickness and can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port, while providing the shortest acoustic path for good sound quality.

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HANDLING INSTRUCTIONS

PICK AND PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 2 and Table 4.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

Document Number: DS-ADMP621-00
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OUTLINE DIMENSIONS

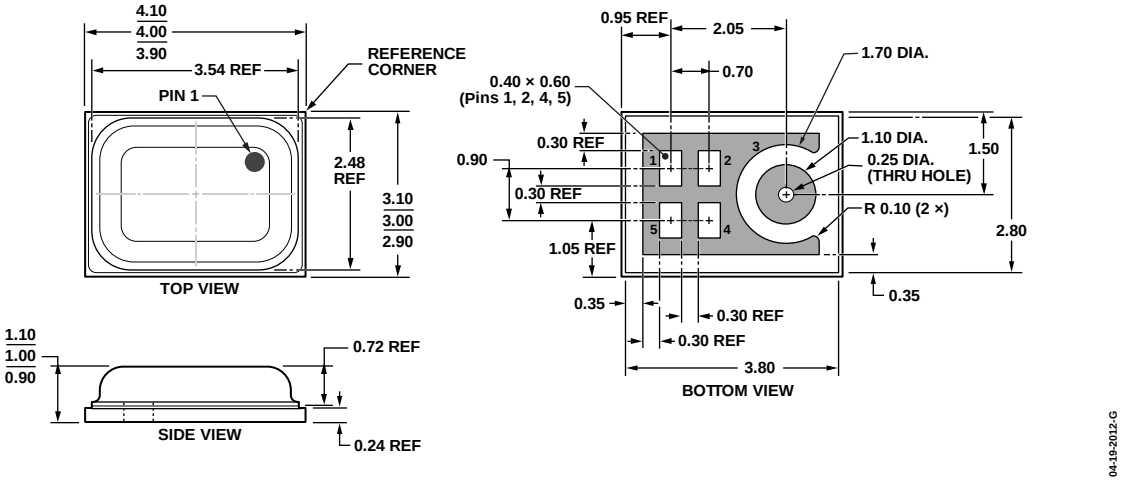

Figure 20. 5-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
4 mm × 3 mm Body
(CE-5-1)
Dimensions shown in millimeters

ORDERING GUIDE

PART[1]	TEMP RANGE	PACKAGE	PACKAGE OPTION[2]	QUANTITY
ADMP621ACEZ-RL	−40°C to +85°C	5-Terminal LGA_CAV*	CE-5-1	5,000
ADMP621ACEZ-RL7	−40°C to +85°C	5-Terminal LGA_CAV†	CE-5-1	1,000
EVAL-ADMP621Z-FLEX	—	Flexible Evaluation Board	—	—

* – 13” Tape and Reel [1]Z = RoHS Compliant Part
† – 7” Tape and Reel [2]This package option is halide free

REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
11/21/2013	1.0	Initial Release

Compliance Declaration Disclaimer:

InvenSense believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

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