# Enpirion® Power Datasheet

## EN5367QI 6A PowerSoC
## Highly Integrated Synchronous Buck With Integrated Inductor

## Description

The EN5367QI is a Power System on a Chip (PowerSoC) DC to DC converter with an integrated inductor, PWM controller, MOSFETs and compensation to provide the smallest solution size in a 5.5x10x3mm 54-pin QFN module. It offers high efficiency, excellent line and load regulation over temperature and up to the full 6A load range. The EN5367QI is specifically designed to meet the precise voltage and fast transient requirements of high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architecture. The EN5367QI also features switching frequency synchronization with an external clock, programmable soft-start as well as thermal shutdown, over-current and short circuit protection. The device's advanced circuit techniques, ultra high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

The Altera Enpirion integrated inductor solution significantly helps to reduce noise. The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements. All Altera Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

## Features

- High Efficiency (Up to 93%)
- Excellent Ripple and EMI Performance
- Up to 6A Continuous Operating Current
- Input Voltage Range (2.5V to 5.5V)
- Frequency Synchronization (External Clock)
- 3% $V_{OUT}$ Accuracy (Over Line/Load/Temperature)
- Optimized Total Solution Size (160mm$^2$)
- Programmable Soft-Start
- Output Enable Pin and Power OK
- Thermal Shutdown, Over-Current, Short Circuit, and Under-Voltage Lockout Protection (UVLO)
- RoHS Compliant, MSL Level 3, 260°C Reflow

## Applications

- Point of Load Regulation for Low-Power, ASICs Multi-Core and Communication Processors, DSPs, FPGAs and Distributed Power Architectures
- Blade Servers, RAID Storage and LAN/SAN Adapter Cards, Wireless Base Stations, Industrial Automation, Test and Measurement, Embedded Computing, and Printers
- Beat Frequency/Noise Sensitive Applications

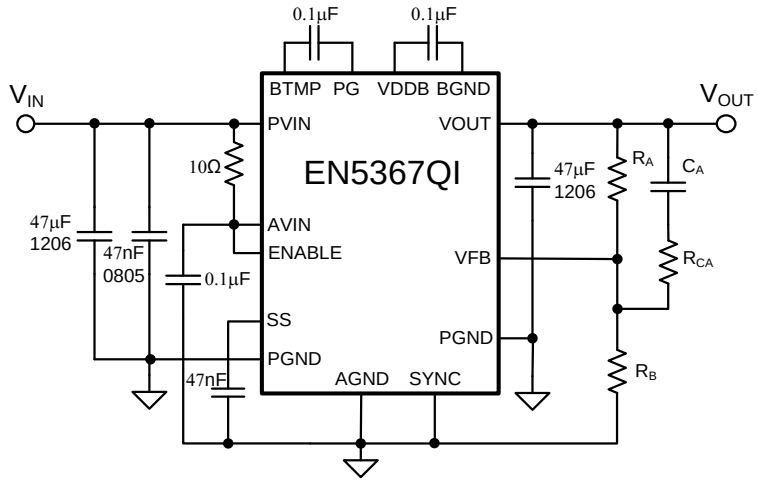



**Figure 1.** Simplified Applications Circuit

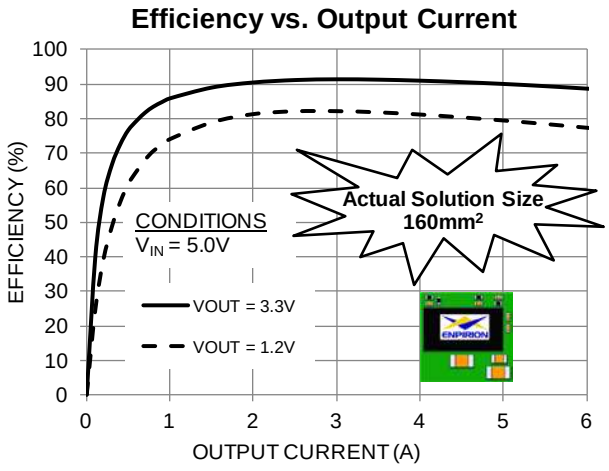



**Figure 2.** Highest Efficiency in Smallest Solution Size

## Ordering Information

| Part Number | Package Markings | Temp Rating (°C) | Package Description |
|---|---|---|---|
| EN5367QI | EN5367QI | -40 to +85 | 54-pin (5.5mm x 10mm x 3mm) QFN T&R |
| EVB-EN5367QI | EN5367QI | QFN Evaluation Board | |

**Packing and Marking Information**: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

## Pin Assignments (Top View)

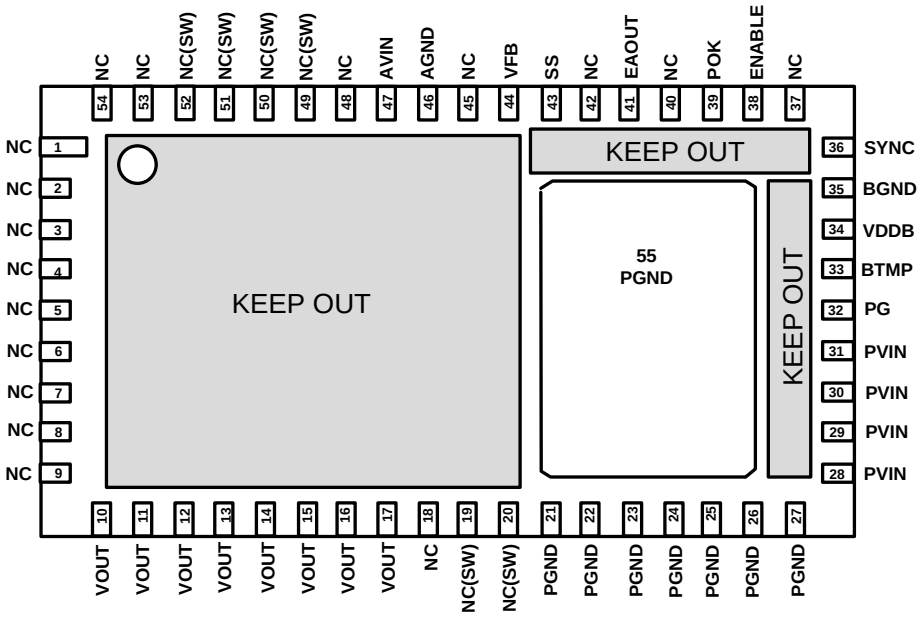



**Figure 3:** Pin Out Diagram (Top View)

**NOTE A**: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

**NOTE B**: Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 9 for details.

**NOTE C**: White 'dot' on top left is pin 1 indicator on top of the device package.

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1-9, 18, 37, 40, 42, 45, 48, 53-54 | NC | NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage. |
| 10-17 | VOUT | Regulated converter output. Connect these pins to the load and place output capacitor between these pins and PGND pins 21-24. |
| 19-20, 49-52 | NC(SW) | NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device. |
| 21-27 | PGND | Input/Output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details. |
| 28-31 | PVIN | Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 25-27. |
| 32 | PG | High-side FET gate. This pin needs to be connected to BTMP using a 0.1µF capacitor. |

| PIN | NAME | FUNCTION |
|---|---|---|
| 33 | BTMP | Low side of the flying capacitor that drives the high-side FET gate. Connect to PG using a 0.1µF capacitor. |
| 34 | VDDB | Regulated voltage used for internal control circuitry. Decouple with a 0.1µF capacitor to BGND. |
| 35 | BGND | Internal GND for VDDB. Connect to VDDB using a 0.1µF capacitor. Do not tie to any grounds on the PCB. |
| 36 | SYNC | A clocked input to this pin will synchronize the internal switching frequency to the external signal. If the SYNC function is not to be used, this pin has to be grounded. Do not float this pin or tie it to a static high voltage. |
| 38 | ENABLE | Input Enable. Applying a logic high enables the output and initiates a soft-start. Applying a logic low disables the output. |
| 39 | POK | Power OK is an open drain transistor used for power system state indication. POK is logic high when VOUT is within -10% of VOUT nominal. |
| 41 | EAOUT | Optional Error Amplifier output. Allows for customization of the control loop. |
| 43 | SS | Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time. |
| 44 | VFB | External Feedback Input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The midpoint of the divider is connected to VFB. A phase lead capacitor from this pin to VOUT is also required to stabilize the loop. |
| 46 | AGND | Analog Ground. This is the Ground return for the controller. Needs to be connected to the GND plane using a via right next to the pin. |
| 47 | AVIN | Input power supply for the controller. Needs to be decoupled to AGND with a 0.1µF capacitor and connected to the input voltage at a quiet point through a 10Ω resistor. |
| 55 | PGND | Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat sinking purposes through a matrix of vias. |

## Absolute Maximum Ratings

**CAUTION**: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Voltages on : PVIN, AVIN, VOUT | | -0.3 | 6.5 | V |
| Voltages on: ENABLE, POK, SYNC | | -0.3 | $V_{IN}$+0.3 | V |
| Voltages on: VFB, SS | | -0.3 | 2.75 | V |
| Storage Temperature Range | $T_{STG}$ | -65 | 150 | ℃ |
| Maximum Operating Junction Temperature | $T_{J\text{-}ABS\ Max}$ | | 150 | ℃ |
| Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A | | | 260 | ℃ |
| ESD Rating (based on Human Body Model) | | | 2000 | V |
| ESD Rating (based on CDM) | | | 500 | V |

## Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | 2.5 | 5.5 | V |
| Output Voltage Range (Note 1) | $V_{OUT}$ | 0.60 | $V_{IN} - V_{DO}$ | V |
| Output Current | $I_{OUT}$ | | 6 | A |
| Operating Ambient Temperature | $T_A$ | -40 | +85 | ℃ |
| Operating Junction Temperature | $T_J$ | -40 | +125 | ℃ |

## Thermal Characteristics

| PARAMETER | SYMBOL | TYP | UNITS |
|---|---|---|---|
| Thermal Resistance: Junction to Ambient (0 LFM) (Note 2) | $\theta_{JA}$ | 22 | ℃/W |
| Thermal Resistance: Junction to Case (0 LFM) | $\theta_{JC}$ | 2 | ℃/W |
| Thermal Shutdown | $T_{SD}$ | 150 | ℃ |
| Thermal Shutdown Hysteresis | $T_{SDH}$ | 20 | ℃ |

**Note 1**: $V_{DO}$ (Dropout Voltage) is defined as ($I_{LOAD}$ x Dropout Resistance). Please refer to Electrical Characteristics Table.

**Note 2**: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

## Electrical Characteristics

NOTE: $V_{IN}$=5.5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at $T_A$ = 25°C.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Input Voltage | $V_{IN}$ | | 2.5 | | 5.5 | V |
| Under Voltage Lock-out – $V_{IN}$ Rising | $V_{UVLOR}$ | Voltage above which UVLO is not asserted | | 2.25 | | V |
| Under Voltage Lock-out – $V_{IN}$ Falling | $V_{UVLOF}$ | Voltage below which UVLO is asserted | | 2.05 | | V |
| Shut-Down Supply Current | $I_S$ | ENABLE=0V | | 100 | | µA |
| Feedback Pin Voltage | $V_{FB}$ | Feedback node voltage at: $V_{IN}$ = 5V, ILOAD = 0, $T_A$ = 25°C | 0.735 | 0.75 | 0.765 | V |
| Feedback Pin Voltage | $V_{FB}$ | Feedback node voltage at: 2.5V ≤ $V_{IN}$ ≤ 5.5V 0A ≤ ILOAD ≤ 6A | 0.7275 | 0.75 | 0.7725 | V |
| Feedback pin Input Leakage Current (Note 3) | $I_{FB}$ | VFB pin input leakage current | -5 | | 5 | nA |
| $V_{OUT}$ Rise Time (Note 3) | $t_{RISE}$ | Measured from when $V_{IN}$ > $V_{UVLOR}$ & ENABLE pin voltage crosses its logic high threshold to when $V_{OUT}$ reaches its final value. $C_{SS}$ = 47 nF | 2.82 | 3.76 | 4.70 | ms |
| Soft Start Capacitor Range | $C_{SS\_RANGE}$ | | 10 | | 68 | nF |
| Output Drop Out Voltage Resistance (Note 3) | $V_{DO}$ $R_{DO}$ | $V_{INMIN}$ - $V_{OUT}$ at Full load Input to Output Resistance | | 300 50 | 600 100 | mV mΩ |
| Continuous Output Current | $I_{OUT\_Max\_Cont}$ | | 0 | | 6 | A |
| Over Current Trip Level | $I_{OCP}$ | $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V | | 9 | | A |
| Disable Threshold | $V_{DISABLE}$ | ENABLE pin logic low. | 0.0 | | 0.6 | V |
| ENABLE Threshold | $V_{ENABLE}$ | ENABLE pin logic high 2.5V ≤ $V_{IN}$ ≤ 5.5V | 1.8 | | $V_{IN}$ | V |
| ENABLE Lockout Time | $T_{ENLOCKOUT}$ | | | 2.4 | | ms |
| ENABLE pin Input Current | $I_{ENABLE}$ | ENABLE pin has ~180kΩ pull down | | 30 | | µA |
| Switching Frequency (Free Running) | $F_{SW}$ | Free Running frequency of oscillator | | 4 | | MHz |
| External SYNC Clock Frequency Lock Range | $F_{PLL\_LOCK}$ | Range of SYNC clock frequency | 3.2 | | 4.2 | MHz |
| SYNC Pin Threshold – Lo | $V_{SYNC\_LO}$ | SYNC Clock Logic Level | | | 0.8 | V |
| SYNC Pin Threshold – Hi | $V_{SYNC\_HI}$ | SYNC Clock Logic Level (Note 4) | 1.8 | | 2.5 | V |

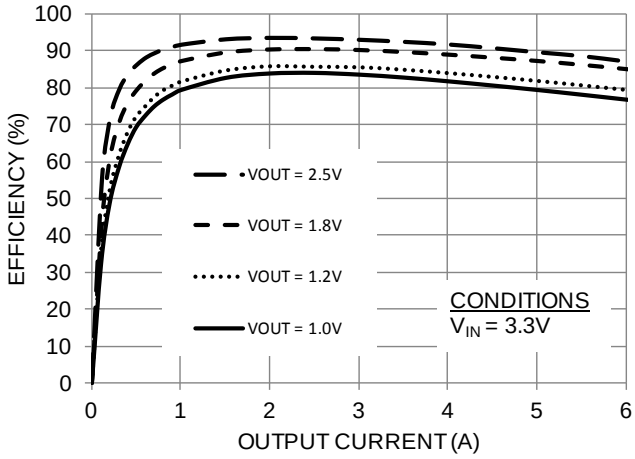
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| POK Threshold | $POK_T$ | Output voltage as a fraction of expected output voltage | | 90 | | % |
| POK Output low Voltage | $V_{POKL}$ | With 1mA current sink into POK | | | 0.4 | V |
| POK Output Hi Voltage | $V_{POKH}$ | $2.5V \le V_{IN} \le 5.5V$ | | | $V_{IN}$ | V |
| POK pin $V_{OH}$ leakage current (Note 3) | $I_{POK}$ | POK high | | | 1 | µA |
| SYNC Pin Current | | SYNC Pin is <2.5V | | <100 | | nA |

**Note 3**: Parameter not production tested but is guaranteed by design.

**Note 4**: For proper operation of the SYNC circuit, the high-level amplitude of the SYNC signal should not be above 2.5V.

## Typical Performance Curves

### Efficiency vs. Output Current

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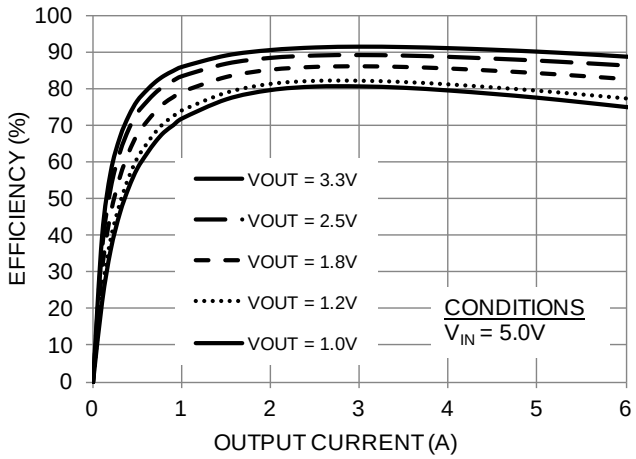
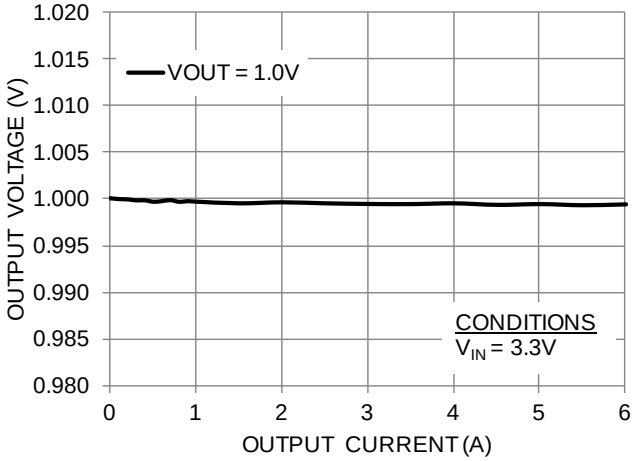



### Output Voltage vs. Output Current

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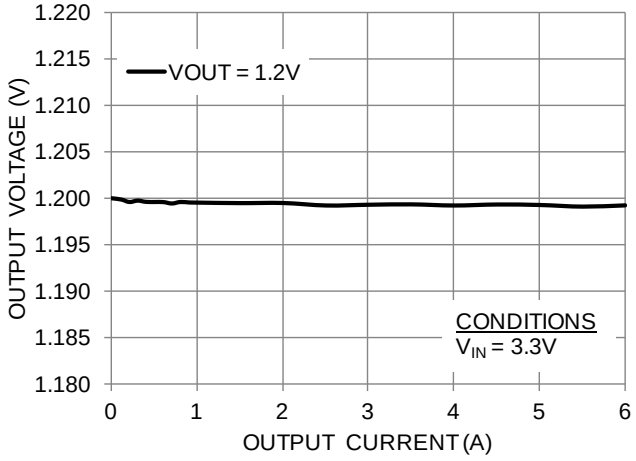


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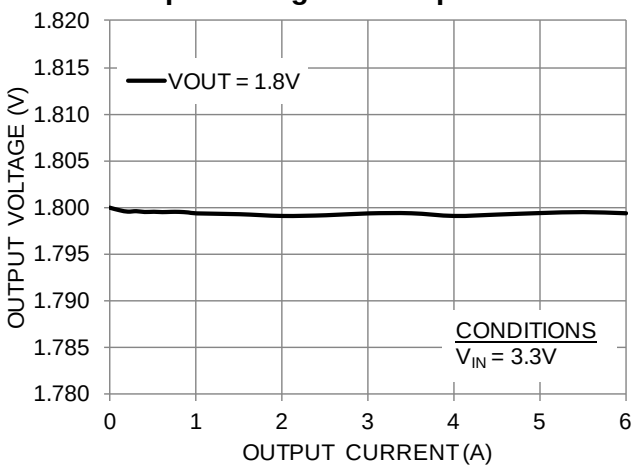
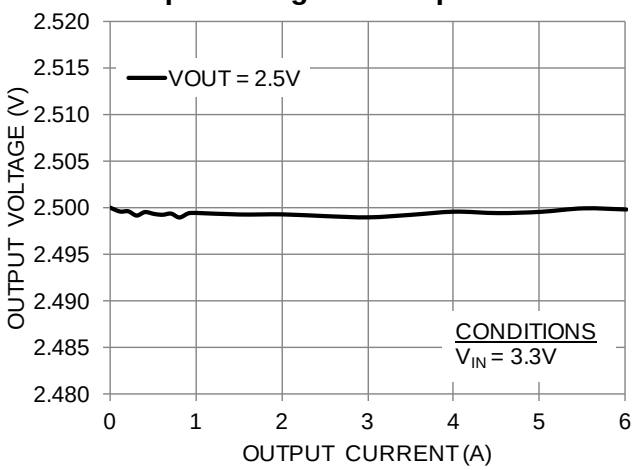
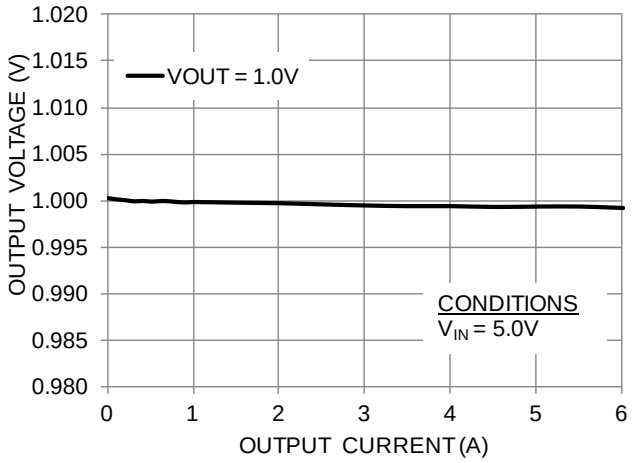



### Output Voltage vs. Output Current

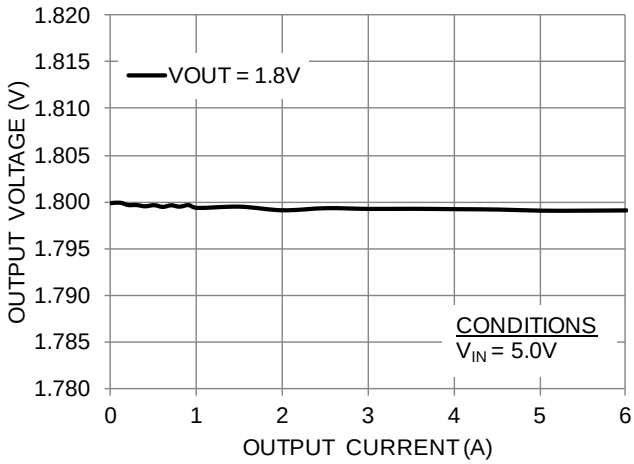


## Typical Performance Curves (Continued)

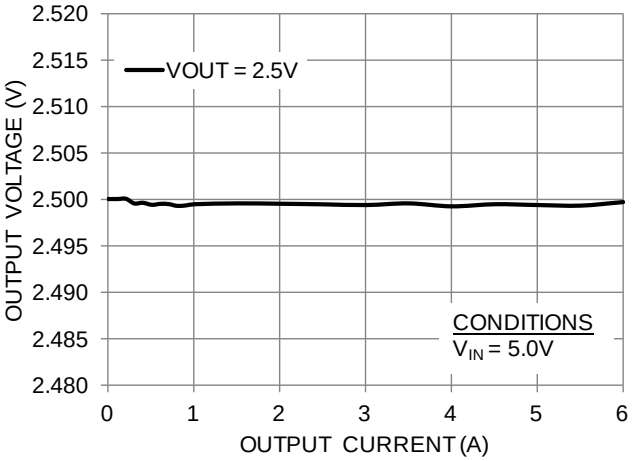
### Output Voltage vs. Output Current




### Output Voltage vs. Output Current




### Output Voltage vs. Output Current

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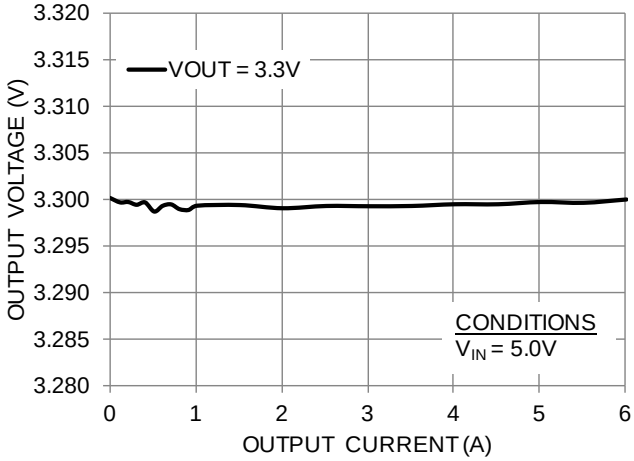
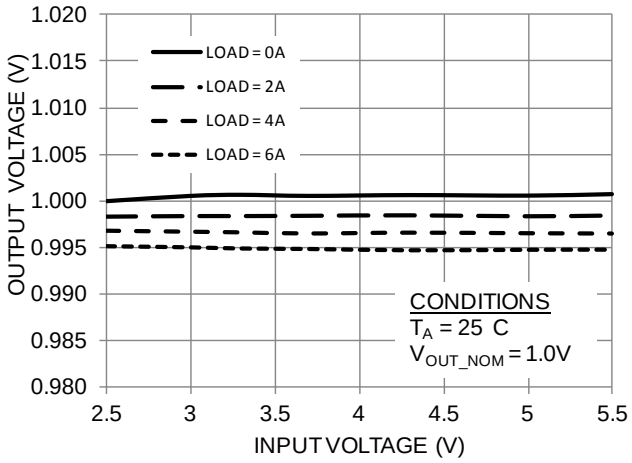



### Output Voltage vs. Input Voltage

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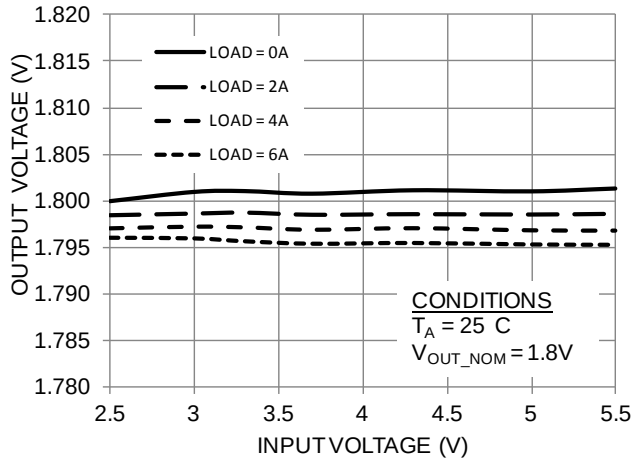
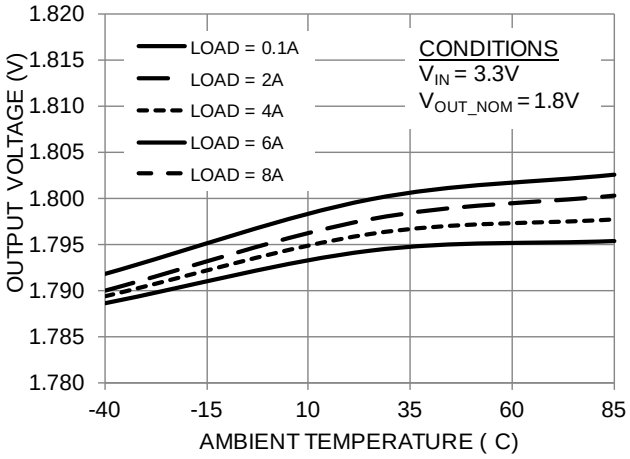


## Typical Performance Curves (Continued)

### Output Voltage vs. Temperature

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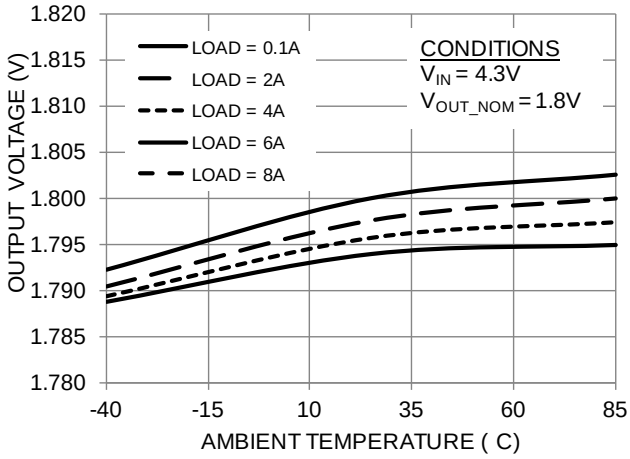


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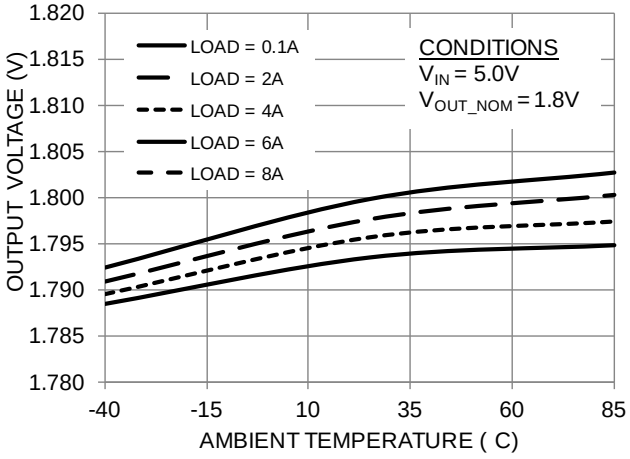


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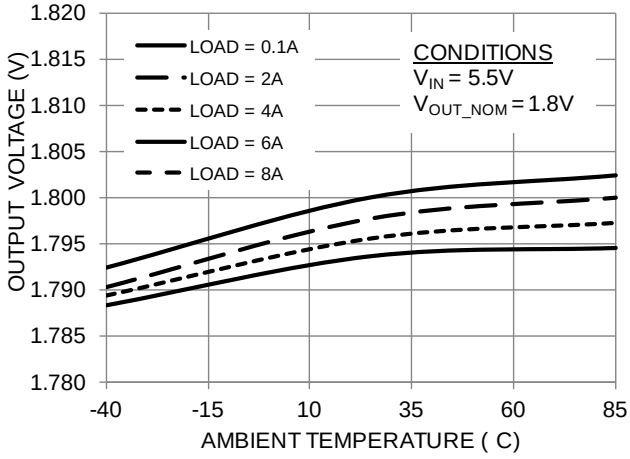
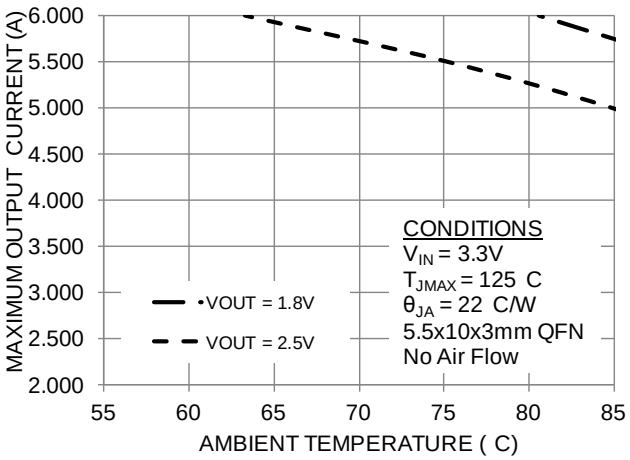



### Output Current De-rating

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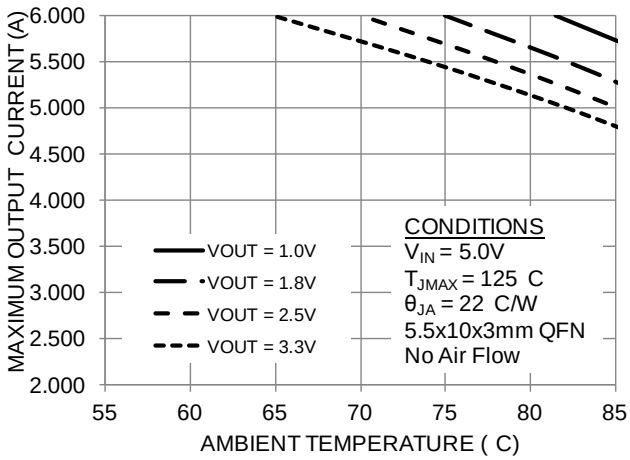
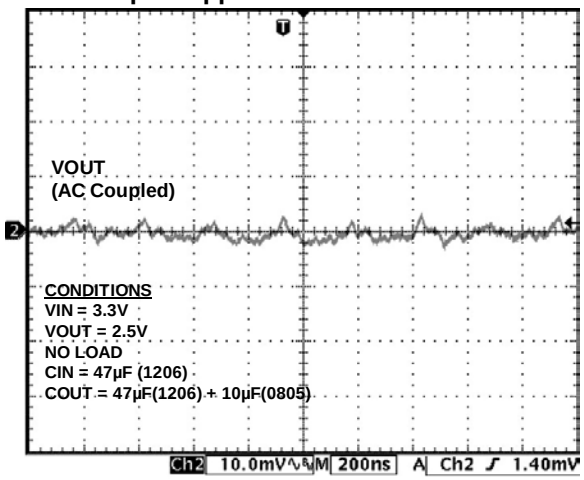


## Typical Performance Characteristics

**Output Ripple at 20MHz Bandwidth**

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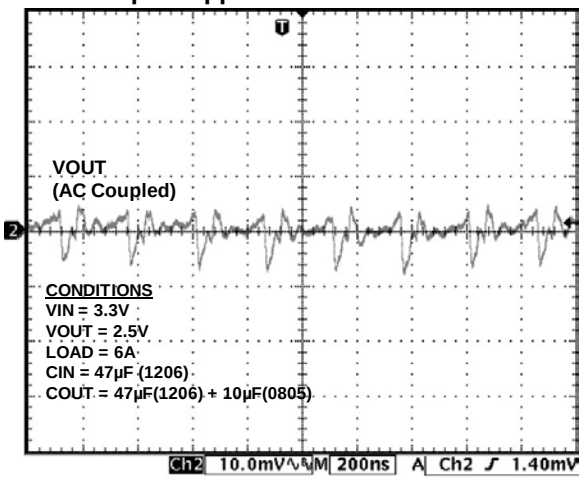


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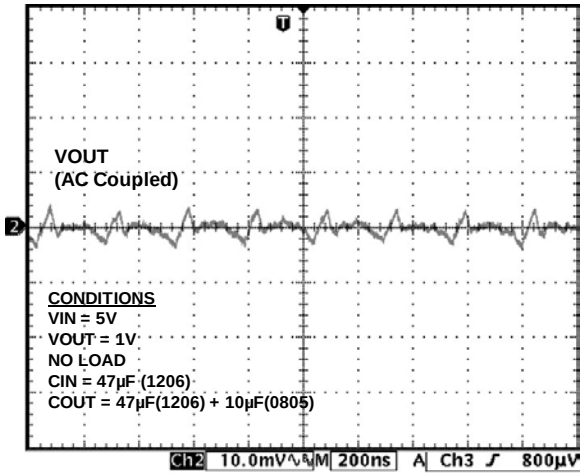


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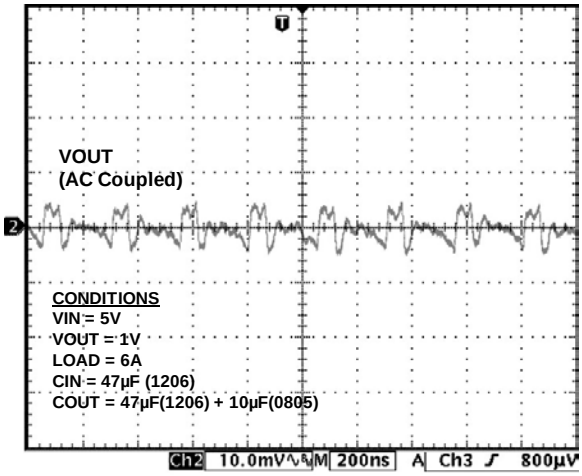
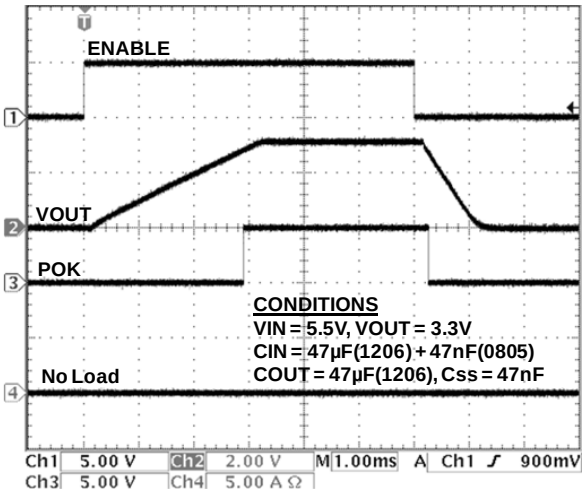



**Enable Power Up/Down**

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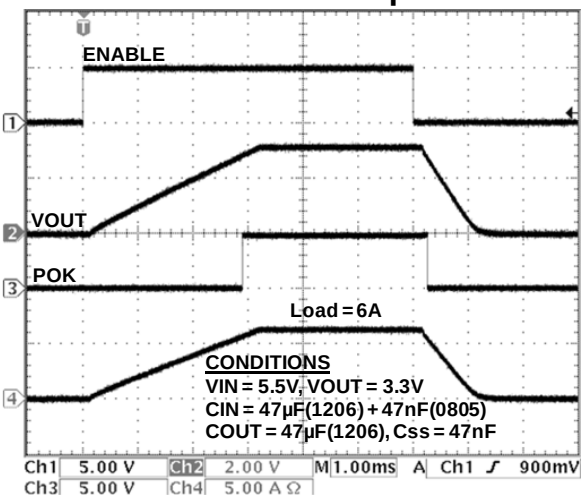
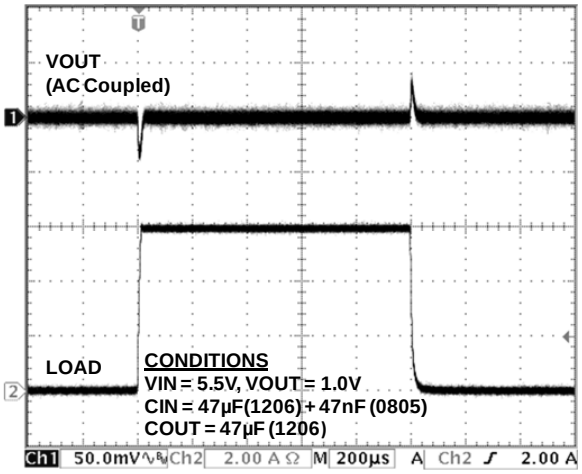
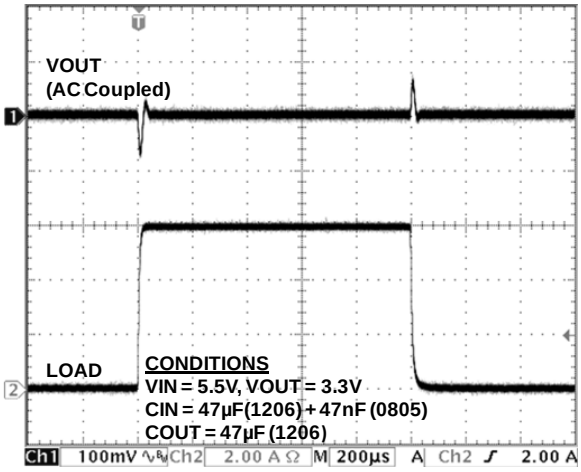


## Typical Performance Characteristics (Continued)

### Load Transient from 0.01 to 6A




### Load Transient from 0.01 to 6A



## Functional Block Diagram

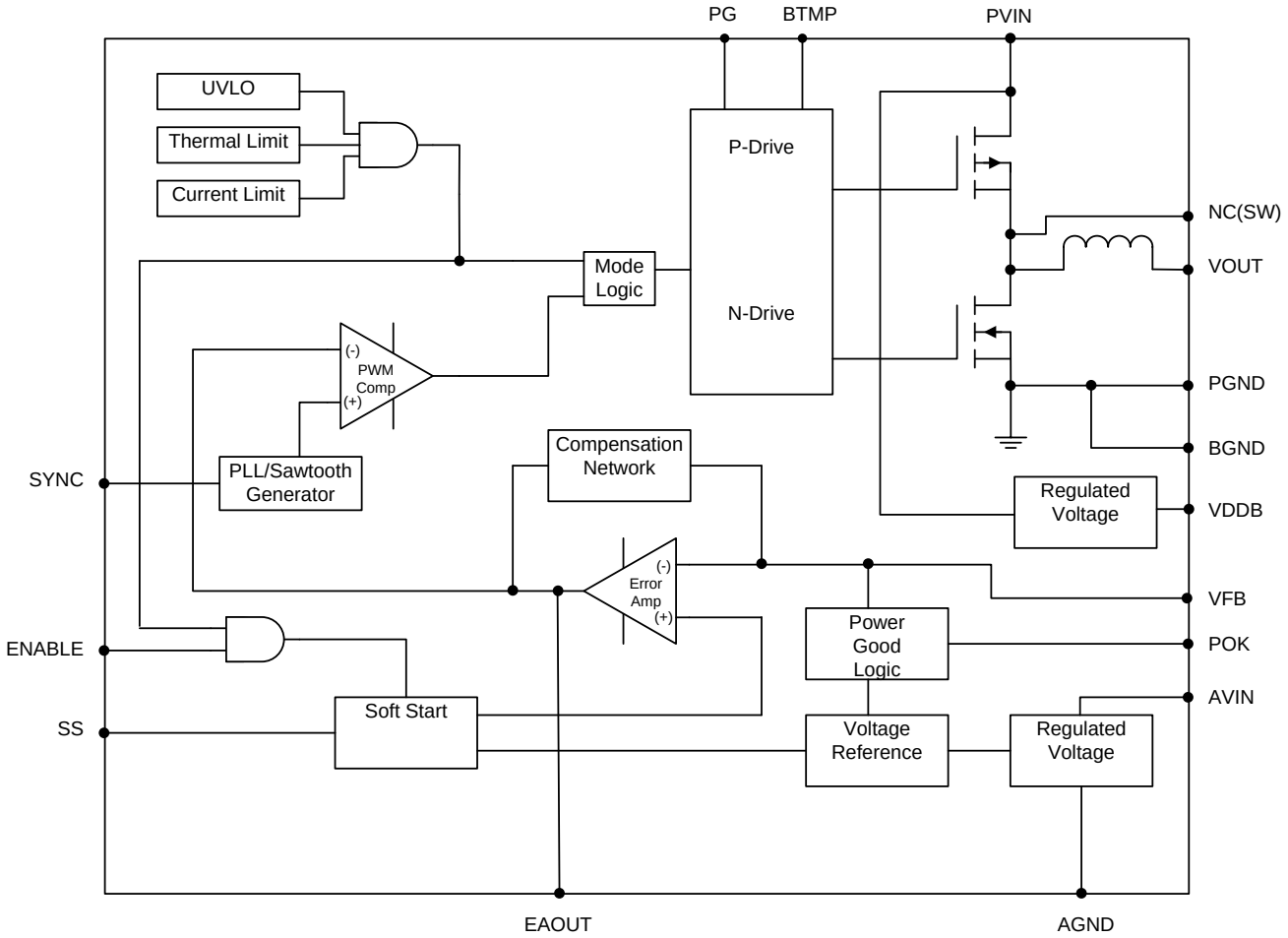



**Figure 4:** Functional Block Diagram

# Functional Description

## Synchronous Buck Converter

The EN5367QI is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.5V to 5.5V. The output voltage is programmed using an external resistor divider network. The control loop is voltage-mode with a type III compensation network. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the type III compensation network. The device uses a low-noise PWM topology. Up to 6A of continuous output current can be drawn from this converter. The 4 MHz switching frequency allows the use of small size input / output capacitors, and realizes a wide loop bandwidth within a small foot print.

## Protection Features:

The power supply has the following protection features:

- Over-Current Protection
- Thermal Shutdown with Hysteresis.
- Under-voltage Lockout

## Additional Features:

- Frequency Synchronization (External Clock)
- Programmable Soft-start
- Output Enable and Power OK

## Power Up-Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. Tying all three pins together meets these requirements. ENABLE can also be tied to AVIN and come up with it, while PVIN can be safely ramped up and down. Alternatively, PVIN can be brought high after AVIN is asserted, and the device can be turned on and off by toggling the ENABLE pin.

## Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft start. A logic low will disable the converter. A logic low will power down the device in a controlled manner and the device is subsequently shut down. The ENABLE signal has to be low for at least the ENABLE Lock-out Time (2.4ms) in order for the device to respond to a falling edge on this pin. Note that the device should not be enabled into a pre-biased output.

## Pre-Bias Operation

The EN5367QI is not designed to be turned on into a pre-biased output voltage. Be sure the output capacitors are not charged or the output of the EN5367QI is not pre-biased when the EN5367QI is first enabled.

## Frequency Synchronization

The switching frequency of the DC/DC converter can be phase-locked to an external clock source to move unwanted beat frequencies out of band. To avail this feature, the clock source should be connected to the SYNC pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the lock range specified in the Electrical Characteristics Table.
If the SYNC function is not to be used, this pin has to be grounded. Do not float this pin or tie it to a static high voltage.

## Spread Spectrum Mode

The external clock frequency may be swept within the SYNC frequency lock range at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

## Soft-Start Operation

During Soft-start, the output voltage is ramped up gradually upon start-up. The output rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (30) and the AGND pin (32).

$$\text{Rise Time [ms]: } T_R \approx (C_{ss}\ [\text{nF}] * 0.08) \pm 25\%$$

where rise time is in ms, and $C_{SS}$ is in nF. During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10uA. Typical soft-start rise time is ~3.75ms with a soft-start capacitor of 47nF. The rise time is measured from when $V_{IN} > V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold, to when $V_{OUT}$ reaches its programmed value.

## POK Operation

The POK signal is an open drain signal (requires a pull up resistor to $V_{IN}$ or similar voltage) from the converter indicating the output voltage is within the specified range. The POK signal will be logic high ($V_{IN}$) when the output voltage is above 90% of programmed $V_{OUT}$. If the output voltage goes below this threshold, the POK signal will be a logic low.

## Over-Current Protection

The current limit function is achieved by sensing the current flowing through the Power PFET. When the sensed current exceeds the over current trip point, both power FETs are turned off for the remainder of the switching cycle. If the over-current condition is removed, the over-current protection circuit will enable normal PWM operation. If the over-current condition persists, the soft start capacitor will gradually discharge causing the output voltage to fall. When the OCP fault is removed, the output voltage will ramp back up to the desired voltage. This circuit is designed to provide high noise immunity.

## Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the Junction temperature exceeds approximately 150ºC. After a thermal shutdown event, when the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

## Input Under-Voltage Lock-Out

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis, input de-glitch and output leading edge blanking ensure high noise immunity and prevent false UVLO triggers.

## Compensation

The EN5367QI uses a type 3 compensation network. As noted earlier, a piece of the compensation network is the phase lead capacitor CA in Figure 1. This network is optimized for use with about 50µF of output capacitance and will provide wide loop bandwidth and excellent transient performance for most applications. Voltage mode operation provides high noise immunity at light load.

In some applications modifications to the compensation may be required. For more information, contact Altera Power Applications support.

## Application Information

The EN5367QI output voltage is programmed using a simple resistor divider network. Figure 1 shows the resistor divider configuration.

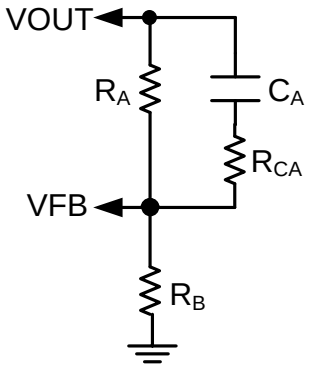



**Figure 1: $V_{OUT}$ Resistor Divider & Compensation Capacitor**

The feedback and compensation network values depend on the input voltage and output voltage. Calculate the external feedback and compensation network values with the equations below.

$R_A$ [kΩ] = 30 x $V_{IN}$ [V]
*Round $R_A$ up to closest standard value

$C_A$ [pF] = 2975 / $R_A$ [kΩ]
*Round $C_A$ down to closest standard value

$R_B$[kΩ] = ($V_{FB}$ x $R_A$) / ($V_{OUT}$ – $V_{FB}$) [V]
$V_{FB}$ = 0.75V nominal
*Use closest suitable value for $R_B$ [kΩ]

$R_{CA}$ = $V_{IN}$ x (1.95 – 0.46 x $V_{OUT}$) kΩ

### Input Capacitor Selection

The EN5367QI requires a 47µF/1206 and a 47nF/0805 input capacitor. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

The first capacitor next to the PVIN and PGND pins must be a 47nF, 0805, X7R capacitor. Behind this first capacitor there can be either a single 47µF capacitor or 2x22µF capacitors. Refer to Table 1 for recommendations.

### Recommended Input Capacitors

| Description | MFG | P/N |
|---|---|---|
| 47nF, 50V or 25V, 10% X7R, 0805 (1 capacitor needed right next to device input pins) | Murata | GRM21BR71H473KA01L |
| | Taiyo Yuden | TMK212B7473KD-T |
| 47µF, 10V, 20% X5R, 1206 (1 capacitor needed in parallel with 47nF above) | Murata | GRM31CR61A476ME15L |
| | Taiyo Yuden | LMK316BJ476ML-T |
| 22µF, 10V, 20% X5R, 1206 (2 capacitors needed in parallel with 47nF above) | Murata | GRM31CR61A226ME19L |
| | Taiyo Yuden | LMK316BJ226ML-T |

**Table 1.** Recommended Input Capacitors

### Output Capacitor Selection

The EN5367QI has been nominally optimized for use with a 47µF/1206 output capacitor. For better output ripple performance, use an additional 10µF/0805 capacitor. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. Refer to Table 2 for recommendations.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

$$Z = ESR + ESL$$

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

### Typical Ripple Voltages

| Output Capacitor Configuration | Typical Output Ripple (mVp-p) (as measured on EN5367QI Evaluation Board)* |
|---|---|
| 1 x 47µF | 17 |
| 47µF + 10µF | 9 |

* Note: 20 MHz BW limit

## Recommended Output Capacitors

| Description | MFG | P/N |
|---|---|---|
| 47µF, 6.3V, 20% X5R, 1206 (1 capacitor needed) | Murata | GRM31CR60J476ME19L |
| | Taiyo Yuden | JMK316BJ476ML-T |
| 10µF, 10V, 10% X5R, 1206 (Optional 1 capacitor in parallel with 47µF above) | Murata | GRM31CR71A106KA01L |
| | Taiyo Yuden | LMK316BJ226ML-T |

**Table 2.** Recommended Output Capacitors

## Power-Up Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. Tying all three pins together meets these requirements.

## Technical Suport

Contact Altera Power Applications support regarding the use of this product (www.altera.com/mysupport).

## Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for.

The Altera Enpirion EN5367QI DC-DC converter is packaged in a 5.5x10x3mm 54-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The following example and calculations illustrate the thermal performance of the EN5367QI.

Example:

$V_{IN}$ = 5V

$V_{OUT}$ = 3.3V

$I_{OUT}$ = 6A

First calculate the output power.

$P_{OUT}$ = 3.3V x 6A = 19.8W

Next, determine the input power based on the efficiency (η) shown in Figure 6.

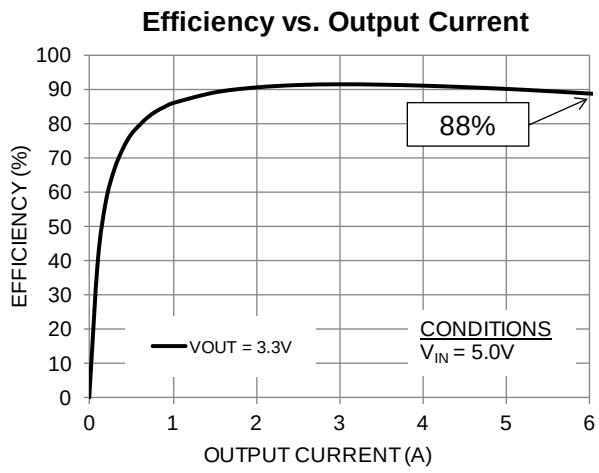



**Figure 6:** Efficiency vs. Output Current

For $V_{IN}$ = 5V, $V_{OUT}$ = 3.3V at 6A, η ≈ 88%

η = $P_{OUT}$ / $P_{IN}$ = 88% = 0.88

$P_{IN}$ = $P_{OUT}$ / η

$P_{IN}$ ≈ 19.8W / 0.88 ≈ 22.5W

The power dissipation ($P_D$) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_D$ = $P_{IN}$ – $P_{OUT}$

≈ 22.5W – 19.8W ≈ 2.7W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value ($\theta_{JA}$). The $\theta_{JA}$ parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN5367QI has a $\theta_{JA}$ value of 22 °C/W without airflow.

Determine the change in temperature (ΔT) based on $P_D$ and $\theta_{JA}$.

ΔT = $P_D$ x $\theta_{JA}$

ΔT ≈ 2.7W x 22°C/W = 59.4°C ≈ 60°C

The junction temperature ($T_J$) of the device is approximately the ambient temperature ($T_A$) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J$ = $T_A$ + ΔT

$T_J$ ≈ 25°C + 60°C ≈ 85°C

The maximum operating junction temperature ($T_{JMAX}$) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature ($T_{AMAX}$) allowed can be calculated.

$T_{AMAX}$ = $T_{JMAX}$ – $P_D$ x $\theta_{JA}$

≈ 125°C – 60°C ≈ 65°C

The maximum ambient temperature the device can reach is 65°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

## Engineering Schematic

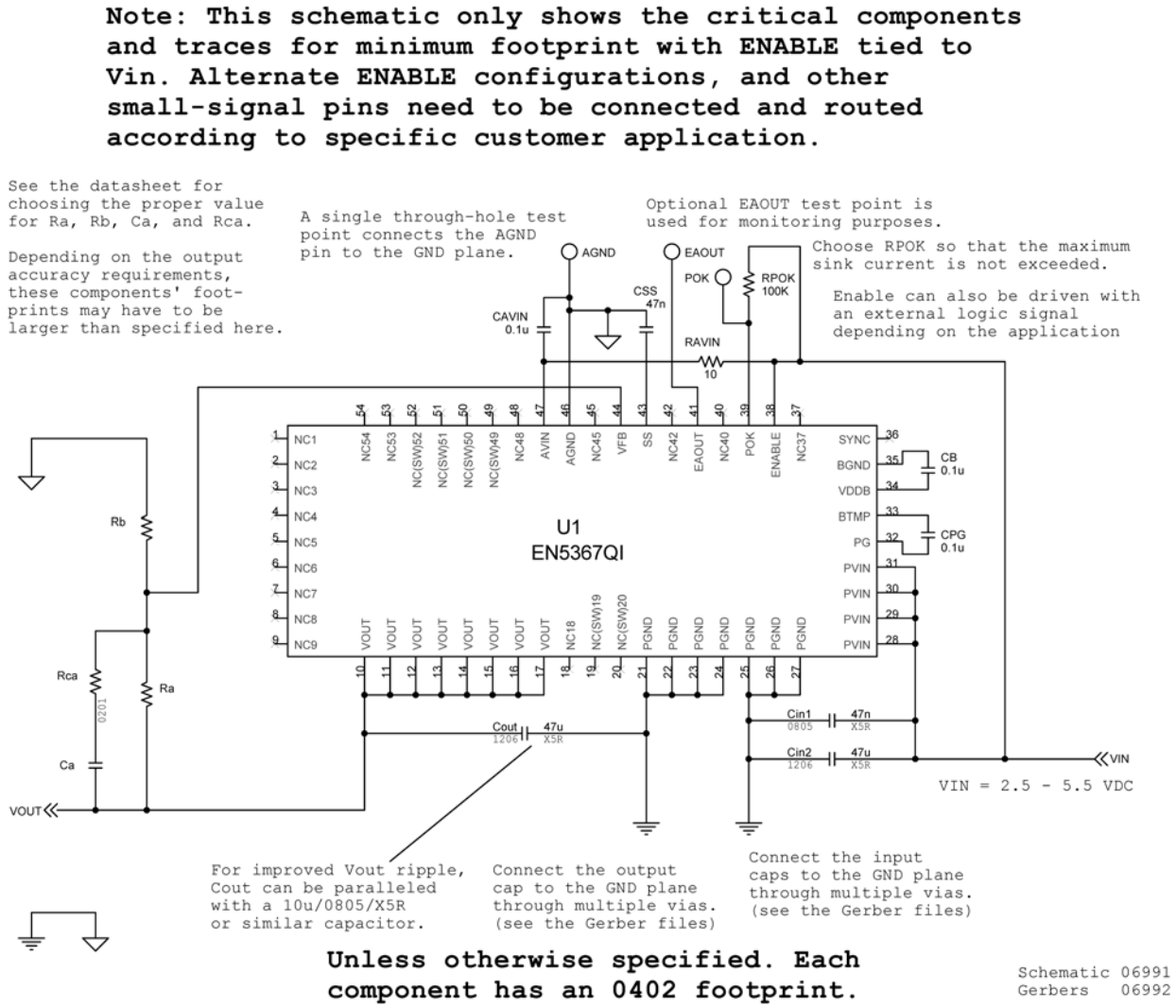



**Figure 7:** Engineering Schematic with Engineering Notes

## Layout Recommendation

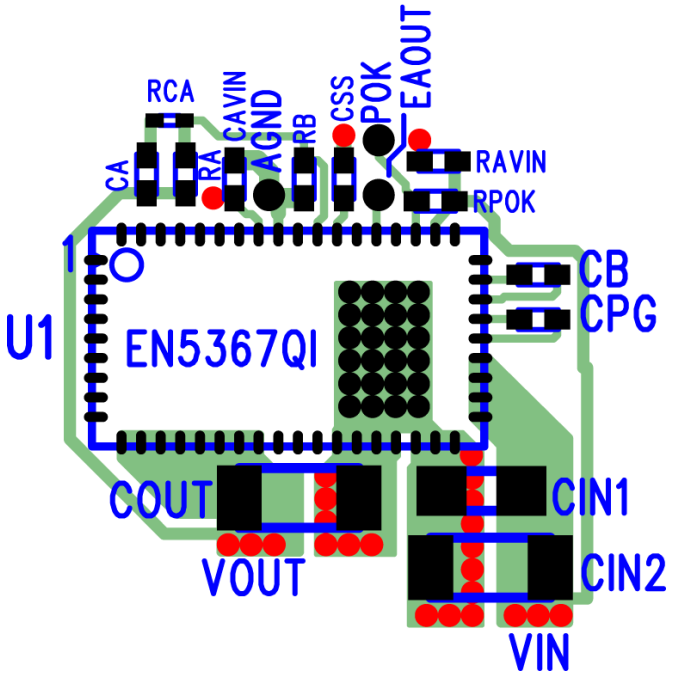



**Figure 8:** Top Layout with Critical Components Only (Top View). See Figure 7 for corresponding schematic.

*This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode with ENABLE tied to AVIN. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at [www.altera.com/enpirion](www.altera.com/enpirion) for details on all layers.*

**Recommendation 1:** Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5367QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5367QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

**Recommendation 2:** The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

**Recommendation 3:** The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

**Recommendation 4**: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

**Recommendation 5**: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

**Recommendation 6**: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 8 this connection is made at the input capacitor.

**Recommendation 7**: The layer 1 metal under the device must not be more than shown in Figure 8. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

**Recommendation 8:** The $V_{OUT}$ sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

**Recommendation 9**: Keep $R_A$, $C_A$, $R_B$, and $R_{CA}$ close to the VFB pin (Refer to Figure 8). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect $R_B$ directly to the AGND pin instead of going through the GND plane.

**Recommendation 10**: Follow all the layout recommendations as close as possible to optimize performance. Altera Enpirion provides schematic and layout reviews for all customer designs. Please contact local Sales Representatives for references to Altera Power Applications support.

# Design Considerations for Lead-Frame Based Modules

## Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 9.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5367QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 9 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult EN5367QI QFN Package Soldering Guidelines for more details and recommendations.

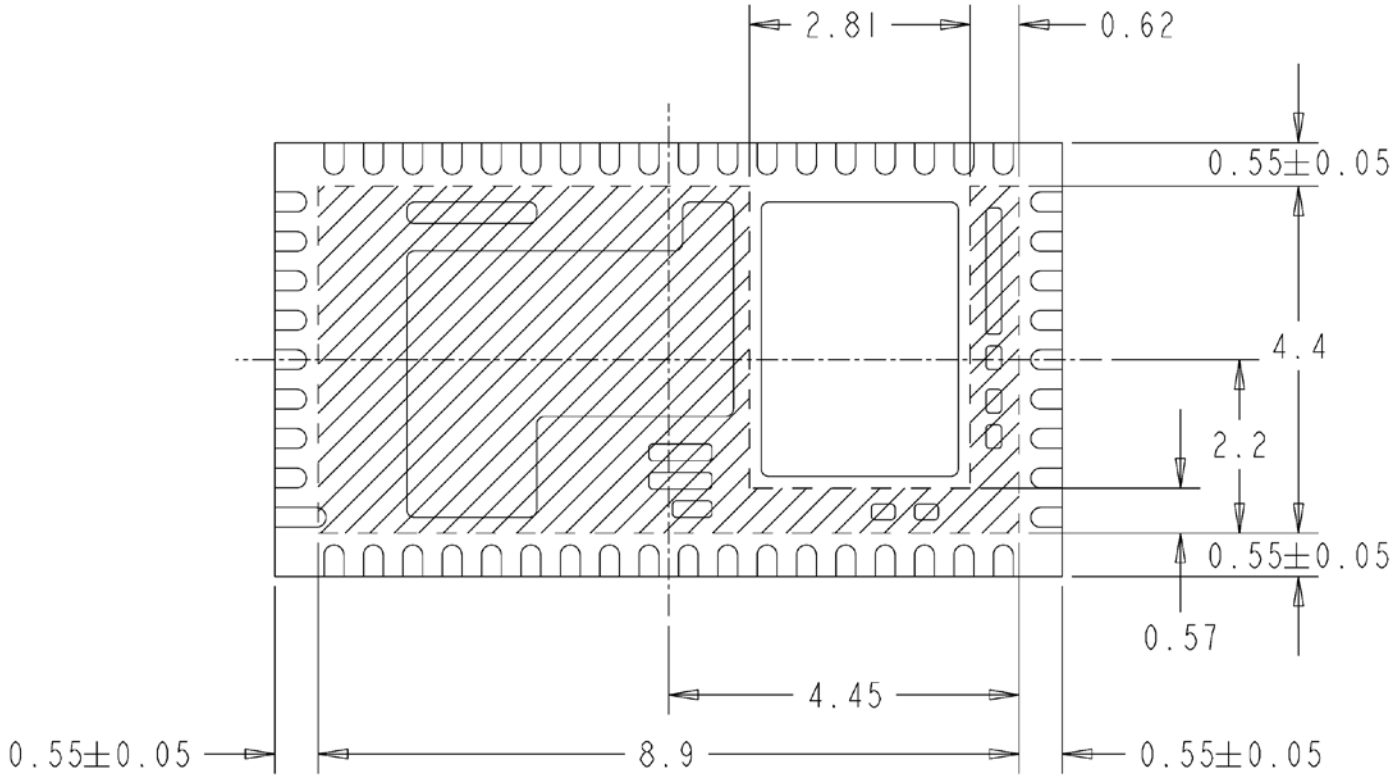



**Figure 9:** Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

## Recommended PCB Footprint

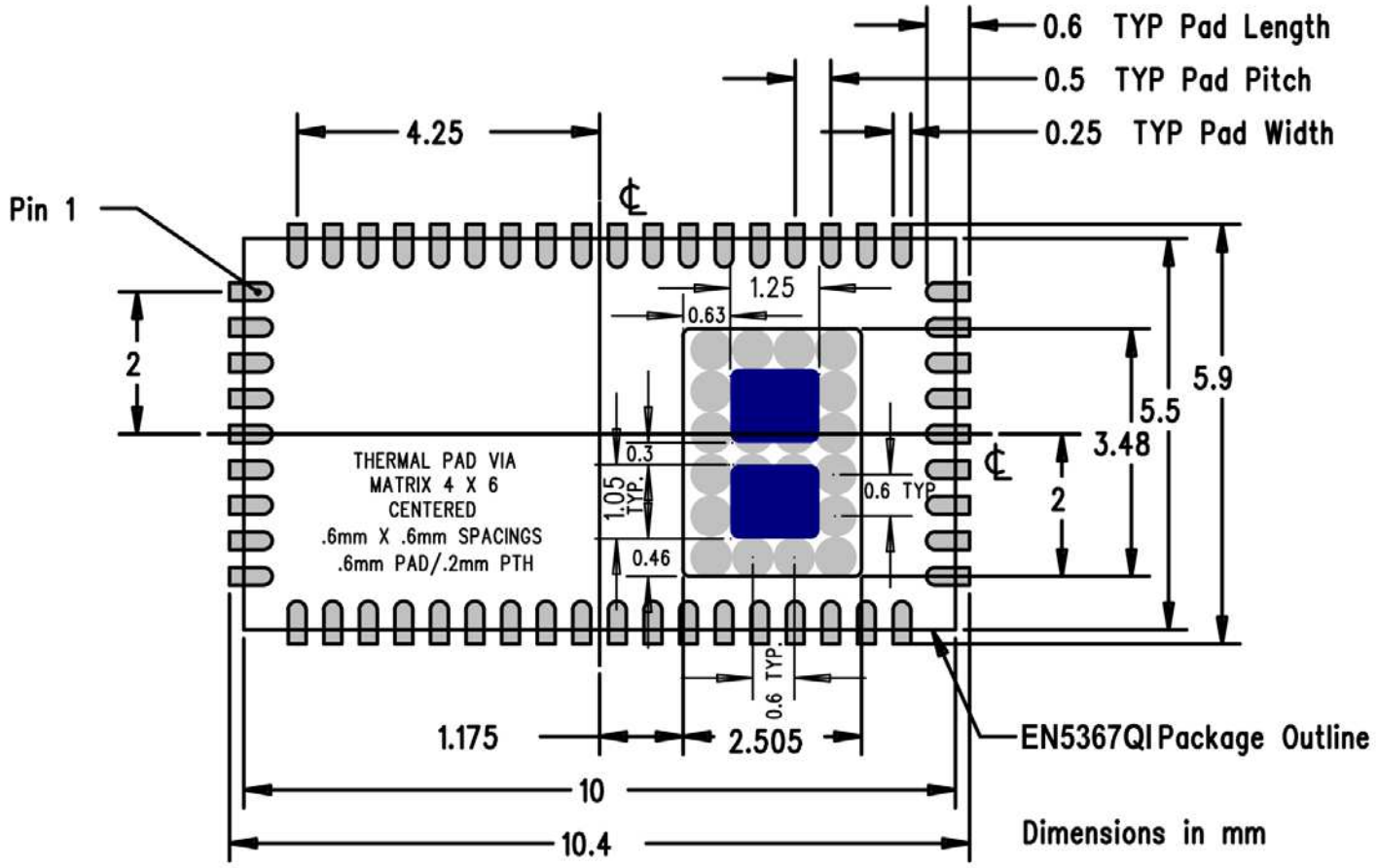



**Figure 10:** EN5367QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

## Package and Mechanical

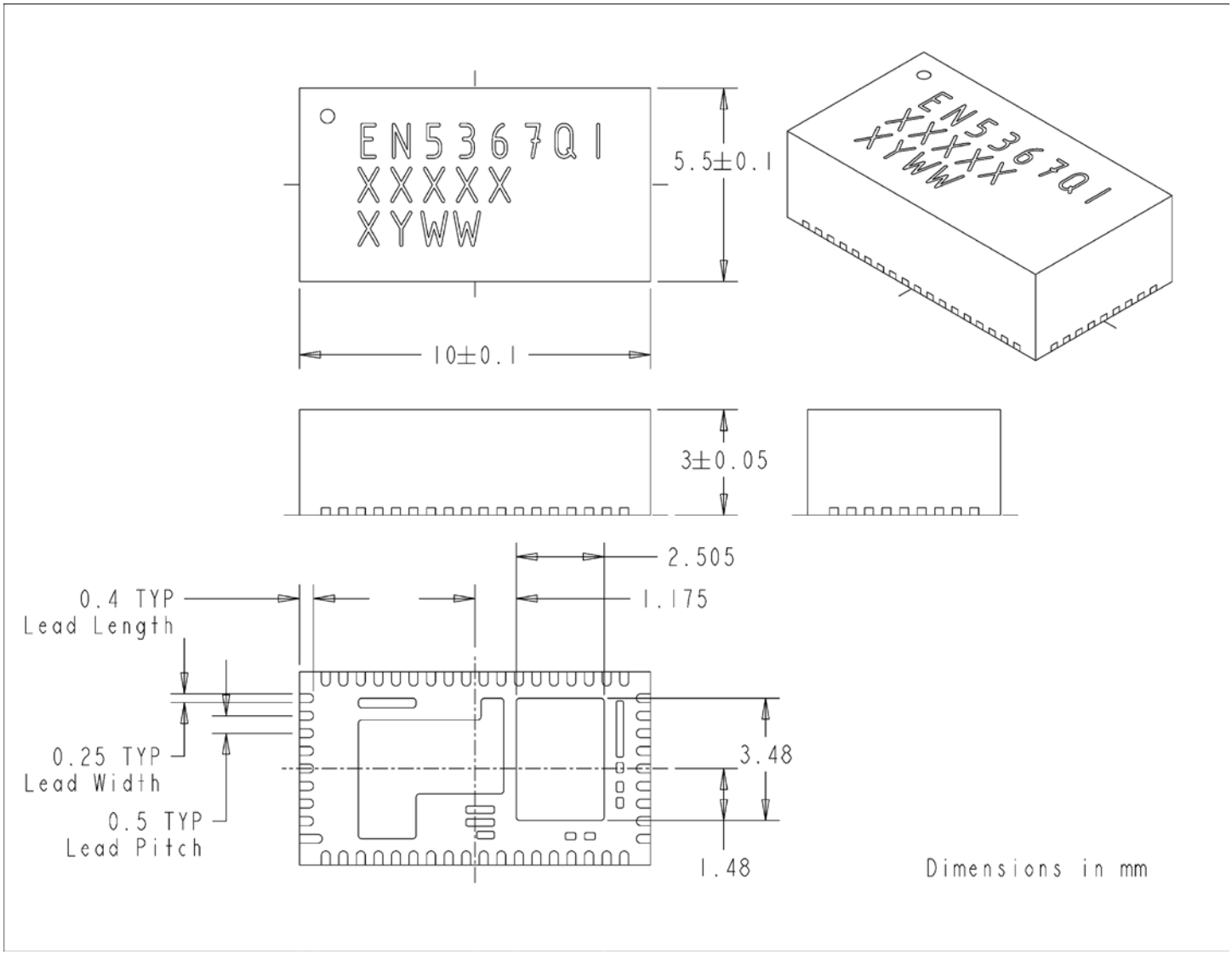



**Figure 11:** EN5367QI Package Dimensions (Bottom View)

**Packing and Marking Information**: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

## Contact Information

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