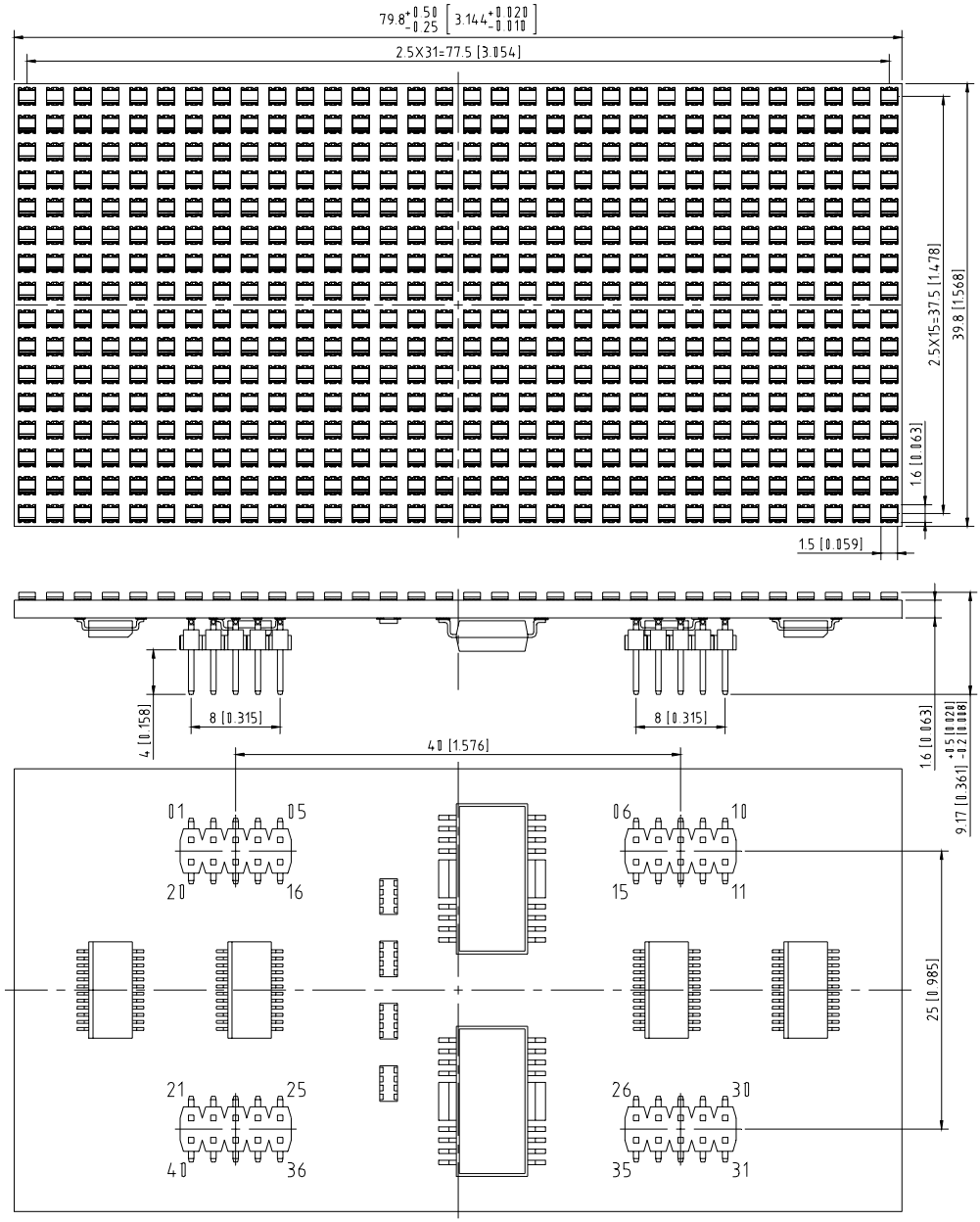
FEATURES

- 1.52 inch (38.6 mm) MATRIX HEIGHT
- LOW POWER REQUIREMENT
- SOLID STATE RELIABILITY
- 16×32 ARRAY WITH X-Y SELECT
- MULTICOLOR DISPLAYS ARE APPLICABLE TO THREE BRIGHT COLORS (GREEN AND RED)
- 1/16 DUTY DYNAMIC SCAN METHOD
- CONTROL METHOD: SHIFT REGISTER TYPE
- COMPATIBLE WITH USASCII AND EBCDIC CODES
- STACKABLE HORIZONTALLY
- CATEGORIZED FOR LUMINOUS INTENSITY

DESCRIPTION

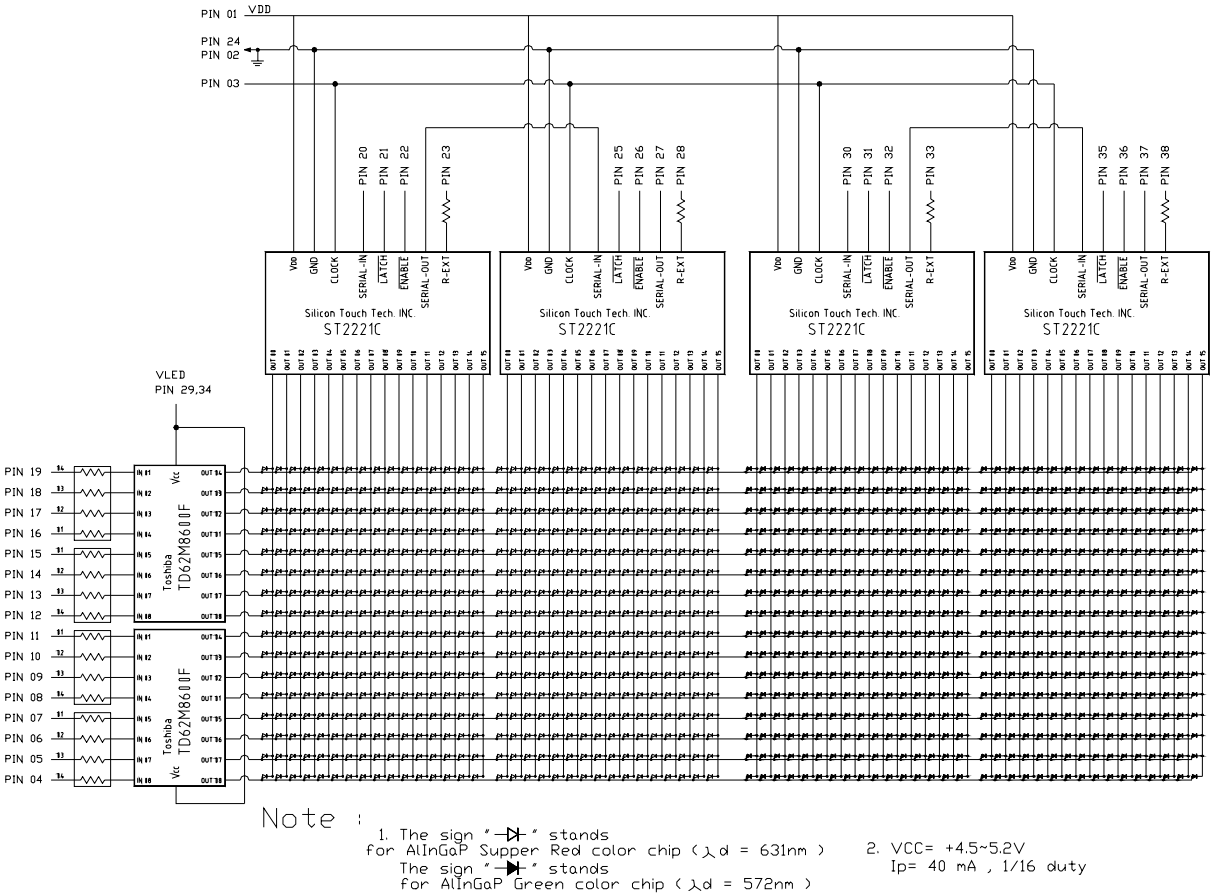
The LTM-0124M-01 is a 1.52 inch (38.6 mm) matrix height 16× 32 dot matrix display which is multicolor applicable and built with constant current drivers (shift register control type). This device uses AS-AlInGaP SUPER RED chip LED and AS-AlInGaP GREEN chip LED.

PACKAGE DIMENSIONS



NOTES: All dimensions are in millimeters. Tolerances are ± 0.25 mm (0.01“) unless otherwise noted.

INTERNAL CIRCUIT DIAGRAM



Note :

1. The sign "→|←" stands for AlInGaP Supper Red color chip (λd = 631nm)
   The sign "→|←" stands for AlInGaP Green color chip (λd = 572nm)
2. VCC= +4.5~5.2V
   Ip= 40 mA , 1/16 duty

PIN CONNECTION

No.	CONNECTION	No.	CONNECTION
1	V_{DD}	21	LATCH(Red Column1~16)
2	GND	22	ENABLE(Red Column1~16)
3	CLOCK	23	R-EXT(Red Column1~16)
4	Anode Row 16, Red & Green	24	GND
5	Anode Row 15, Red & Green	25	LATCH(Red Column17~32)
6	Anode Row 14, Red & Green	26	ENABLE(Red Column17~32)
7	Anode Row 13, Red & Green	27	Red Data Serial Out
8	Anode Row 12, Red & Green	28	R-EXT(Red Column17~32)
9	Anode Row 11, Red & Green	29	V_{LED}
10	Anode Row 10, Red & Green	30	Green Data Serial In
11	Anode Row 9, Red & Green	31	LATCH(Green Column1~16)
12	Anode Row 8, Red & Green	32	ENABLE(Green Column1~16)
13	Anode Row 7, Red & Green	33	R-EXT(Green Column1~16)
14	Anode Row 6, Red & Green	34	V_{LED}
15	Anode Row 5, Red & Green	35	LATCH(Green Column17~32)
16	Anode Row 4, Red & Green	36	ENABLE(Green Column17~32)
17	Anode Row 3, Red & Green	37	Green Data Serial Out
18	Anode Row 2, Red & Green	38	R-EXT(Green Column17~32)
19	Anode Row 1, Red & Green	39	No Connection
20	Red Data Serial In	40	No Connection

ELECTRICAL / OPTICAL CHARACTERISTICS AT Ta=25°C

Red

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	I_V	6	10		mcd	I_p=40mA 1/16Duty
Peak Emission Wavelength	λp		639		nm	I_F=20mA
Spectral Line Half-Width	$\Delta\lambda$		20		nm	I_F=20mA
Dominant Wavelength	λd		631		nm	I_F=20mA
Forward Voltage any Dot	V_F		2.0	2.4	V	I_F=20mA
Reverse Current any Dot	I_R			100	μA	V_R=5V
Luminous Intensity Matching Ratio	I_V-m			2:1		I_p=32mA 1/16Duty

Green

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	I_V	3.6	6.4		mcd	I_p=32mA 1/16Duty
Peak Emission Wavelength	λp		574		nm	I_F=20mA
Spectral Line Half-Width	$\Delta\lambda$		15		nm	I_F=20mA
Dominant Wavelength	λd		571		nm	I_F=20mA
Forward Voltage any Dot	V_F		2.0	2.4	V	I_F=20mA
Reverse Current any Dot	I_R			100	μA	V_R=5V
Luminous Intensity Matching Ratio	I_V-m			2:1		I_p=32mA 1/16Duty

Note: Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (Commision Internationale De L'Eclairage) eye-response curve.

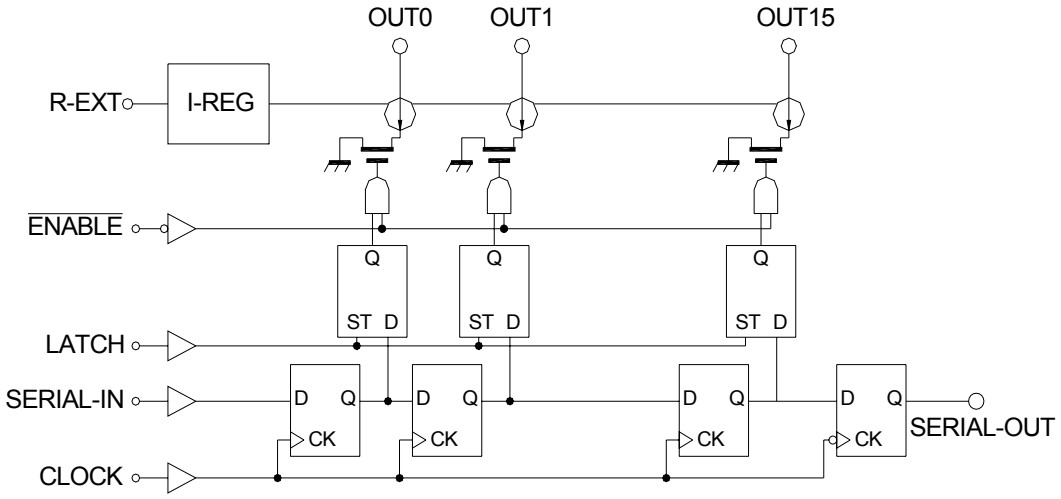
ABSOLUTE MAXIMUM RATING FOR SHIFT REGISTER AT Ta=25°C

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0～7.0	V
Input Voltage	V_{IN}	-0.4～V_{DD}+0.4	V
Output Current per V_{OUT}	I_{OUT}	120	mA
Output Voltage per V_{OUT}	V_{CE}	-0.5～9.5	V
Clock Frequency	f_{CK}	25	MHz
GND Terminal Current	I_{GND}	1920	mA
Power Dissipation	P_D	1.27(T=25℃)	W
		0.61(T=85℃)	
Operating Temperature	Topr	-25℃～45℃	℃
Storage Temperature	Tstg	-25℃～85℃	℃
Solder Temperature 1/16 inch Below Seating Plane for 3 Seconds at 260℃			

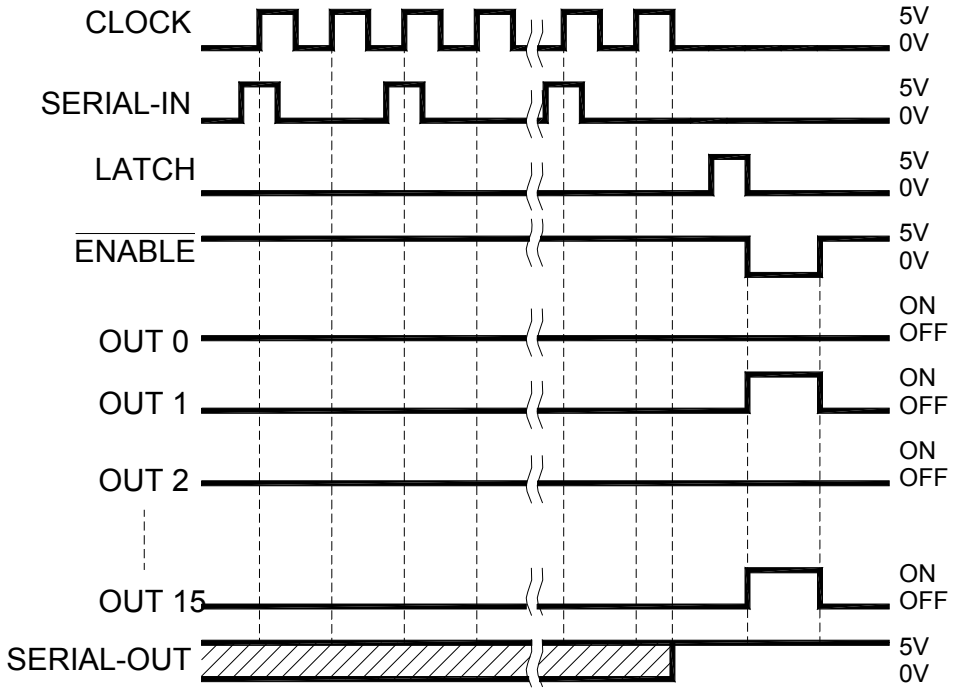
RECOMMENDED OPERATING CONDITION
(T=-40～85℃ unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LED Voltage	V_{LED}	-	3	3.5	4	V
Supply Voltage	V_{DD}	-	4.5	5.0	5.5	V
Output Voltage	V_{OUT}	-	-	-	9	V
Output Current per	I_O	OUTn	5	-	115	mA
	I_{OH}	SERIAL-OUT	-	-	1.0	
	I_{OL}	SERIAL-OUT	-	-	-1.0	
Input Voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}+0.3	V
	V_{IL}		-0.3		0.3V_{DD}	
LATCH Pulse Width	tw LAT	-	15	-	-	ns
CLOCK Pulse Width	tw CLK		15	-	-	ns
Set-up Time for DATA	tsetup(D)	V_{DD}=4.5~5.5V	20	-	-	ns
Hold Time for DATA	thold(D)		20	-	-	ns
Set-up Time for LATCH	tsetup(L)		15	-	-	ns
Clock Frequency	f_{CLK}	Cascde operation	-	-	25	MHz
Power Dissipation	P_D	T=85ºC	-	-	0.61	W

BLOCK DIAGRAM



TIMING DIAGRAM



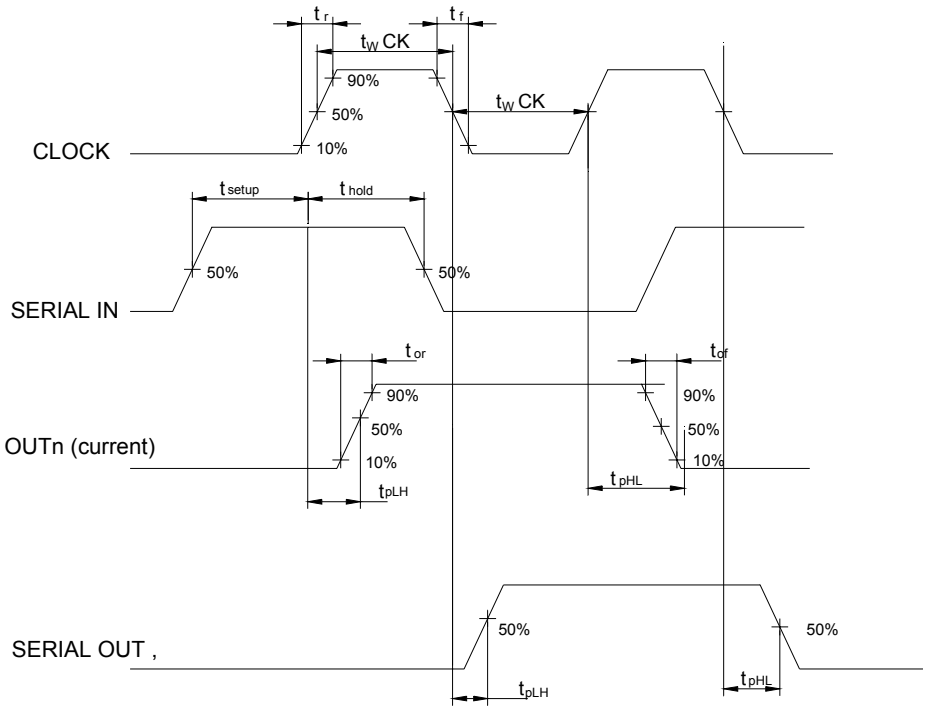
Latches are level sensitive(not edge triggered).

Latch-terminal= H level, latches become transparent; Latch-terminal= L level, hold data.

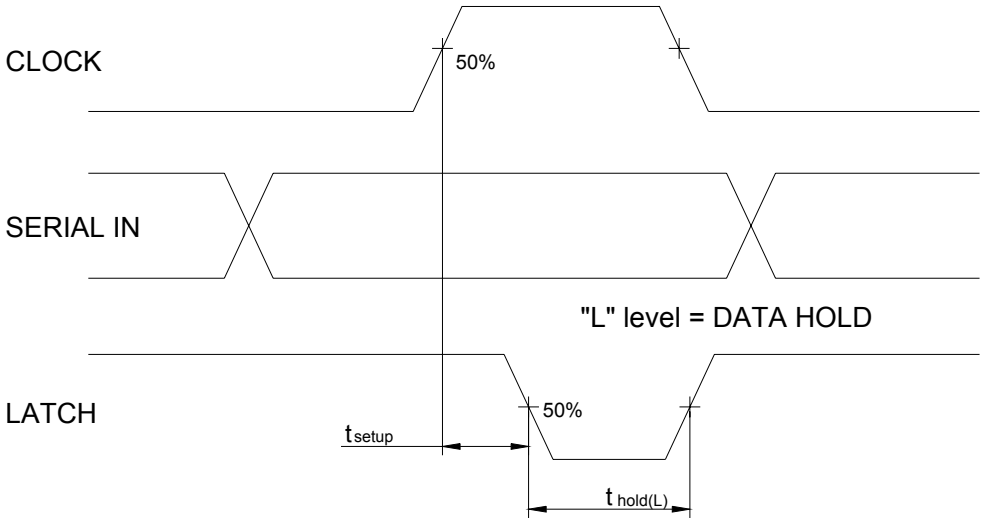
ENABLE-terminal= H level, all outputs(OUT0~15) are off.

SERIAL-OUT changes state on falling edges of clock.

CLOCK – SERIAL , OUT , OUTn



Clock - LATCH



ENABLE - OUTn