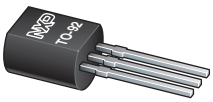


# ACT108-600D

## AC Thyristor power switch

Rev. 02 — 27 December 2010 Product data sheet

## 1. Product profile

### 1.1 General description

AC Thyristor power switch in a SOT54 plastic package with self-protective capabilities against low and high energy transients

### 1.2 Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- High noise immunity
- Remote gate separates the gate driver from the effects of the load current
- Safe clamping of low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Very sensitive gate for lowest gate trigger current

### 1.3 Applications

- Fan motor circuits
- Lower-power highly inductive, resistive and safety loads
- Pump motor circuits

### 1.4 Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | - | - | 600 | V |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 100 mA; LD- G-; $T_j$ = 25 ℃ | 0.5 | - | 5 | mA |
| | | $V_D$ = 12 V; $I_T$ = 100 mA; LD+ G-; $T_j$ = 25 ℃; see Figure 6 | 0.5 | - | 5 | mA |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead}$ ≤ 71 ℃; see Figure 2 | - | - | 0.8 | A |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 402 V; $T_j$ = 125 ℃; gate open circuit; exponential waveform; see Figure 10 | 300 | - | - | V/µs |
| $V_{CL}$ | clamping voltage | $I_{CL}$ = 100 µA; $t_p$ = 1 ms; $T_j$ ≤ 125 ℃; see Figure 13 | 650 | - | - | V |

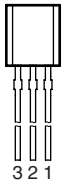
**Table 1. Quick reference data** *...continued*

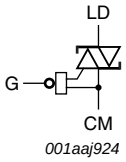
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 100 mA; $T_j$ = 25 °C | - | - | 0.9 | V |
| $V_{PP}$ | peak pulse voltage | $T_j$ = 25 °C; non-repetitive, off-state; see Figure 1 | - | - | 2 | kV |
| $V_T$ | on-state voltage | $I_T$ = 1.1 A; see Figure 9 | - | - | 1.3 | V |

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | CM | common | | |
| 2 | G | gate | | |
| 3 | LD | load | | |




**SOT54 (TO-92)**

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| ACT108-600D | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq 71$ °C; see Figure 2 | - | 0.8 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms | - | 8.8 | A |
| | | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; see Figure 3; see Figure 4 | - | 8 | A |
| $I^2t$ | I2t for fusing | $t_p = 10$ ms; sine-wave pulse | - | 0.32 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_T = 1$ A; $I_G = 10$ mA; $dI_G/dt = 0.2$ A/µs | - | 50 | A/µs |
| $I_{GM}$ | peak gate current | t = 20 µs | - | 1 | A |
| $V_{GM}$ | peak gate voltage | positive applied gate voltage | - | 15 | V |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| $T_{stg}$ | storage temperature | | -40 | 150 | °C |
| $T_j$ | junction temperature | | - | 125 | °C |
| $V_{PP}$ | peak pulse voltage | $T_j = 25$ °C; non-repetitive, off-state; see Figure 1 | - | 2 | kV |

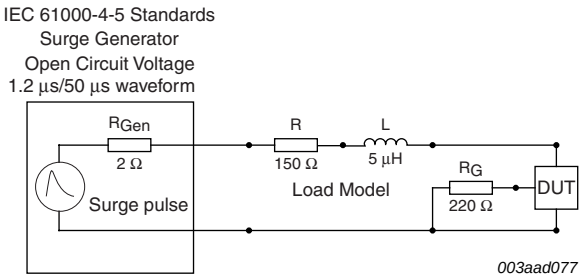
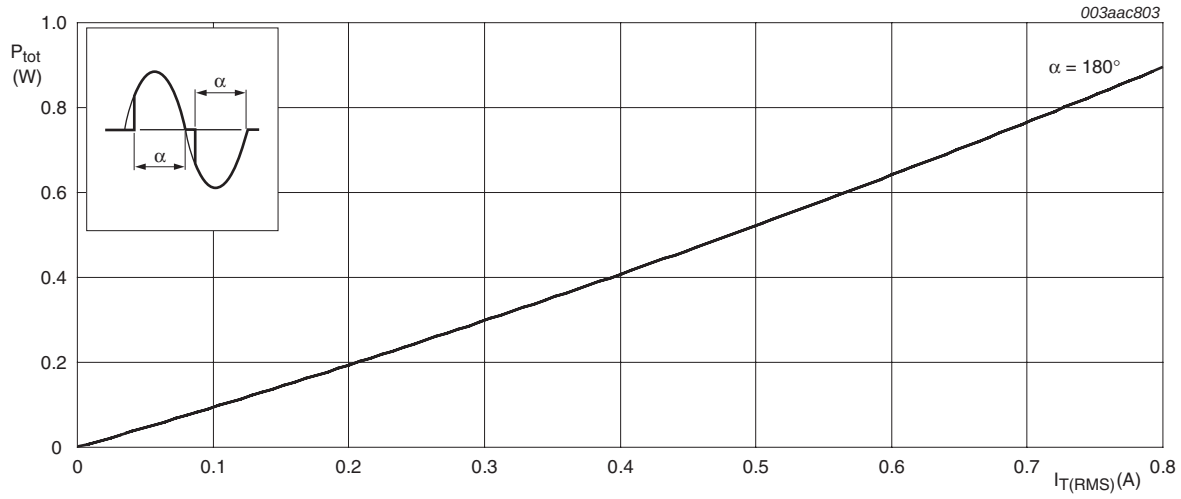
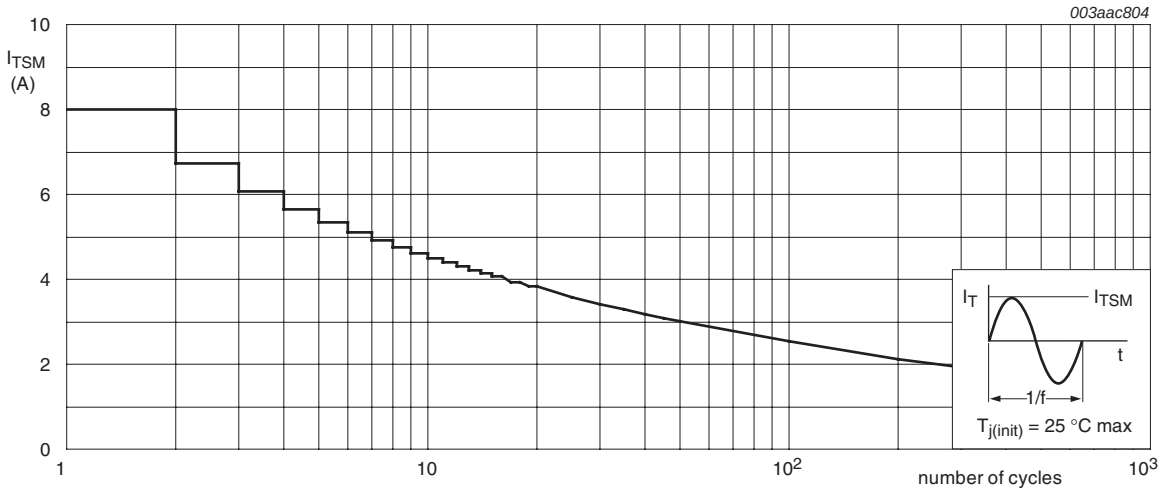



**Fig 1. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5**



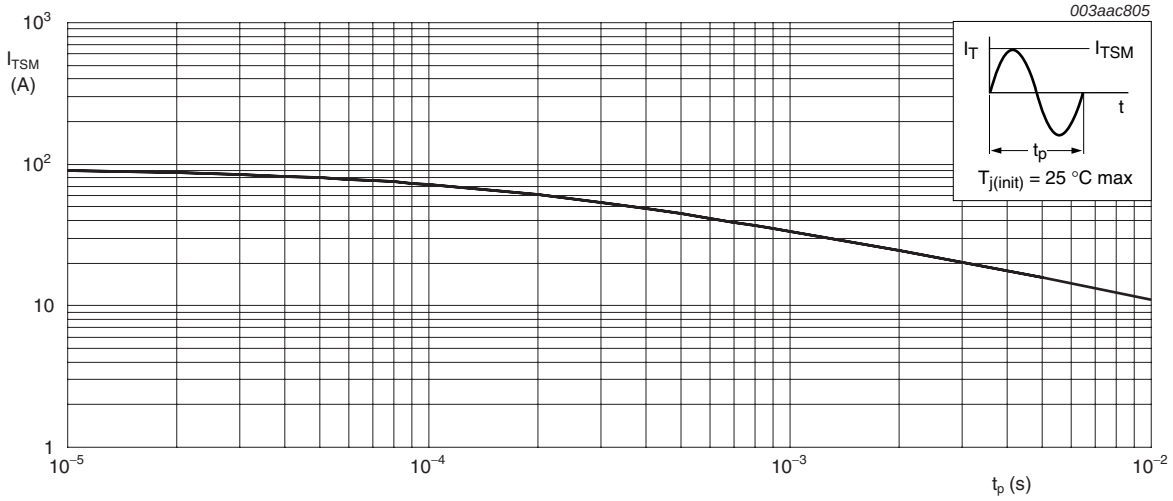

α = conduction angle

**Fig 2. Total power dissipation as a function of RMS on-state current; maximum values**




f = 50 Hz

**Fig 3. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**




$t_p \leq 20$ ms

**Fig 4. Non-repetitive peak on-state current as a function of pulse width; maximum values**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}lead)}$ | thermal resistance from junction to lead | full cycle with heatsink compound; see Figure 5 | - | - | 60 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | full cycle; printed-circuit board mounted; lead length 4 mm | - | 150 | - | K/W |

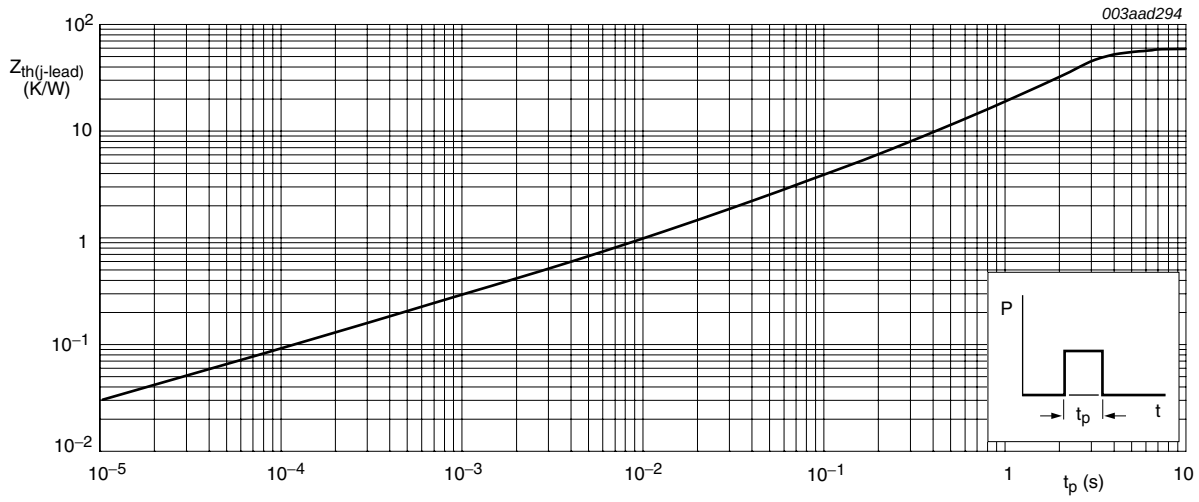
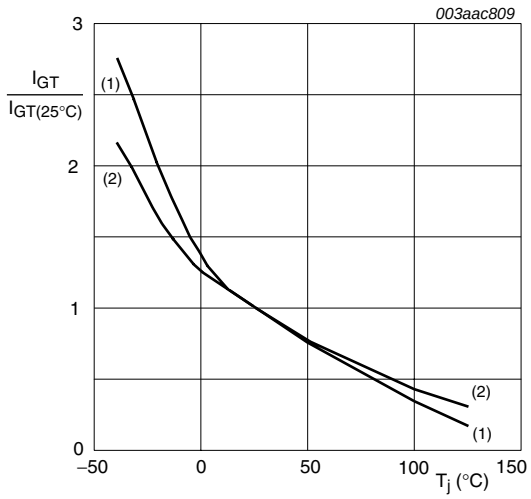



**Fig 5. Transient thermal impedance from junction to lead as a function of pulse width**

## 6. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 100 mA; LD- G-; $T_j$ = 25 ℃ | 0.5 | - | 5 | mA |
| | | $V_D$ = 12 V; $I_T$ = 100 mA; LD+ G-; $T_j$ = 25 ℃; see Figure 6 | 0.5 | - | 5 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 12 mA; $T_j$ = 25 ℃; see Figure 7 | - | - | 25 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 ℃; see Figure 8 | - | - | 20 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1.1 A; see Figure 9 | - | - | 1.3 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 100 mA; $T_j$ ≤ 125 ℃ | 0.15 | - | - | V |
| | | $V_D$ = 12 V; $I_T$ = 100 mA; $T_j$ = 25 °C | - | - | 0.9 | V |
| $I_D$ | off-state current | $V_D$ = 600 V; $T_j$ ≤ 25 ℃ | - | - | 2 | µA |
| | | $V_D$ = 600 V; $T_j$ ≤ 125 ℃ | - | - | 0.2 | mA |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 402 V; $T_j$ = 125 ℃; gate open circuit; exponential waveform; see Figure 10 | 300 | - | - | V/µs |
| $dI_{com}/dt$ | rate of change of commutating current | $V_D$ = 400 V; $T_j$ = 125 ℃; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 15 V/µs; gate open circuit; see Figure 11; see Figure 12 | 0.15 | - | - | A/ms |
| $V_{CL}$ | clamping voltage | $I_{CL}$ = 100 µA; $t_p$ = 1 ms; $T_j$ ≤ 125 ℃; see Figure 13 | 650 | - | - | V |




(1) LD+ G-

(2) LD- G-

**Fig 6. Normalized gate trigger current as a function of junction temperature**

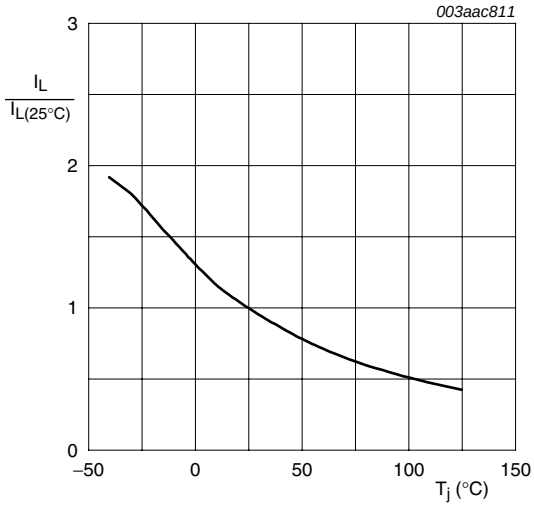



**Fig 7. Normalized latching current as a function of junction temperature**

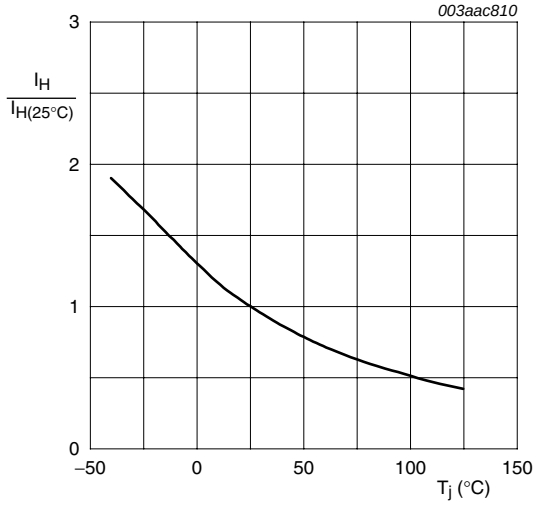
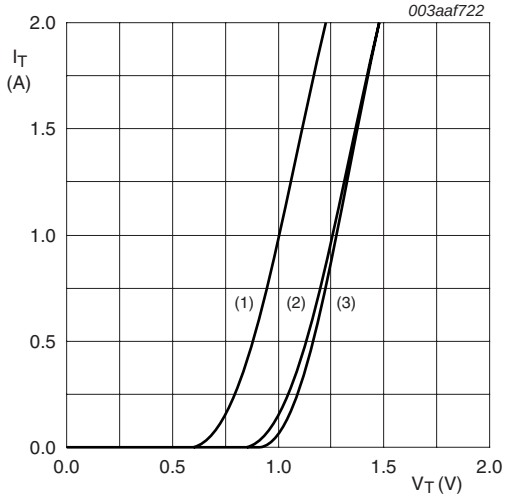



**Fig 8. Normalized holding current as a function of junction temperature**




$V_o = 0.758\,V$

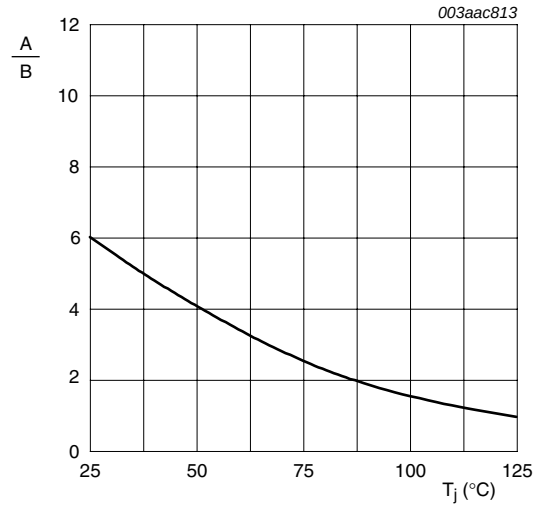
$R_s = 0.263\,\Omega$

(1) $T_j = 125\,°C$ ; typical values

(2) $T_j = 125\,°C$ ; maximum values

(3) $T_j = 25\,°C$ ; maximum values

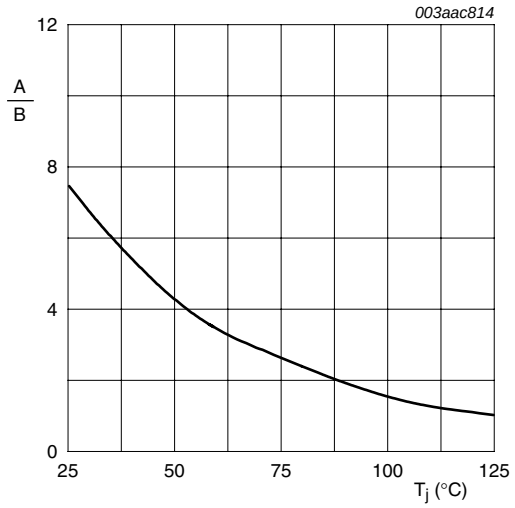
**Fig 9. On-state current as a function of on-state voltage**




A is $dV_D/dt$ at condition $T_j$ ℃

B is $dV_D/dt$ at condition $T_j$ 125 ℃

**Fig 10. Normalized rate of rise of off-state voltage as a function of junction temperature**

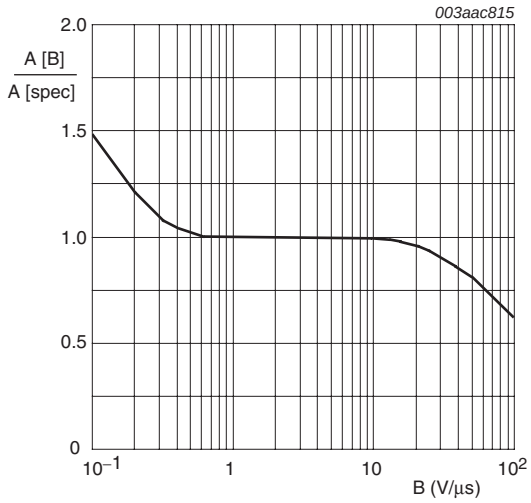



A is $dI_{com}/dt$ at condition $T_j$ ℃

B is $dI_{com}/dt$ at condition $T_j$ 125 ℃

$V_D$ = 400 V

**Fig 11. Normalized critical rate of rise of commutating current as a function of junction temperature**




A[B] is $dI_{com}/dt$ at condition B, $dV_{com}/dt$

A[spec] is the specified data sheet value of $dI_{com}/dt$

turn-off time < 20 ms

**Fig 12. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values**

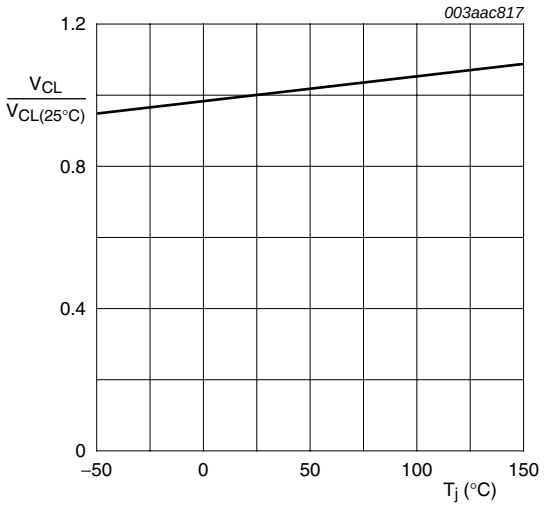
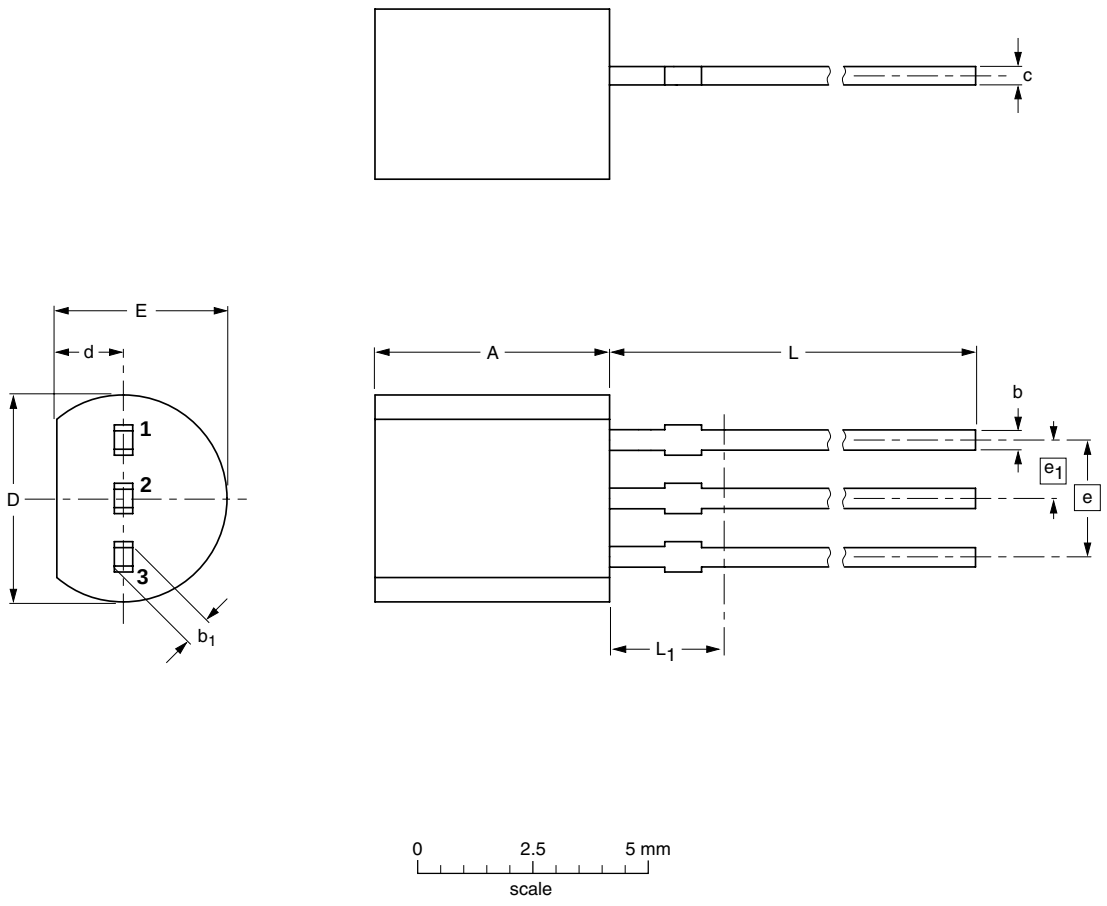



**Fig 13. Normalized clamping voltage (upper limit) as a function of junction temperature; minimum values**

## 7. Package outline

**Plastic single-ended leaded (through hole) package; 3 leads** **SOT54**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$ (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.55 | 0.45<br>0.38 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27 | 14.5<br>12.7 | 2.5 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT54 | | TO-92 | SC-43A | | | ~~04-06-28~~<br>04-11-16 |

**Fig 14. Package outline SOT54 (TO-92)**

## 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| ACT108-600D v.2 | 20101227 | Product data sheet | - | ACT108-600D v.1 |
| Modifications: | • Status changed from preliminary to product.<br>• Various changes to content. | | | |
| ACT108-600D v.1 | 20100902 | Preliminary data sheet | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

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