HD74LV166A

Parallel-Load 8-bit Shift Register

R04DS0002EJ0400
(Previous: REJ03D0321-0300)
Rev.4.00
Aug 16, 2010

Description

The HD74LV166A is 8-bit shift register with an output from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Shift/Load input is low, the data is loaded asynchronously in parallel. When the Shift/Load input is high, the data is loaded serially on the rising edge of either clock inhibit or Clock. Clear is asynchronous and active-low.

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.3 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV166AFPEL	SOP–16 pin(JEITA)	PRSP0016DH-B (FP–16DAV)	FP	EL (2,000 pcs/reel)
HD74LV166ATELL	TSSOP–16 pin	PTSP0016JB-A (TTP–16DAV)	T	ELL (2,000 pcs/reel)

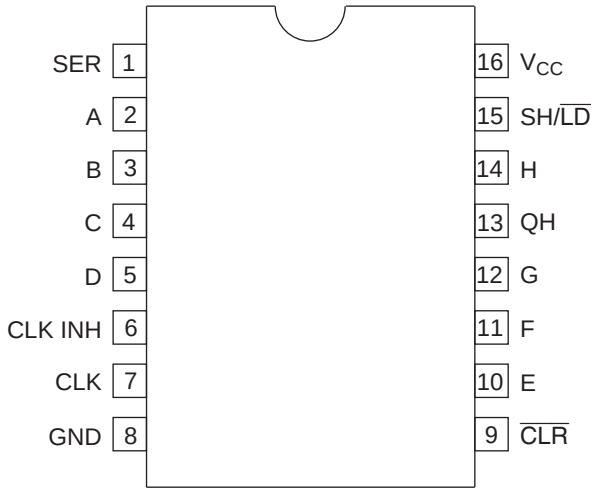
Note: Please consult the sales office for the above package availability.

Function Table

Inputs						Internal outputs		Output
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	CLK	SER	A ... H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a ... h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Note: H: High level
L: Low level
↑: Low to high transition
X: Immaterial
a ... h: Parallel data
Q_{A0} ... Q_{H0}: Outputs remain unchanged.
Q_{An} ... Q_{Gn}: Data shifted from the previous stage on a positive edge at the clock input.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		V_{CC}: OFF
Input clamp current	I_{IK}	–20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25℃ (in still air)* [3]	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	Tstg	–65 to 150	℃	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

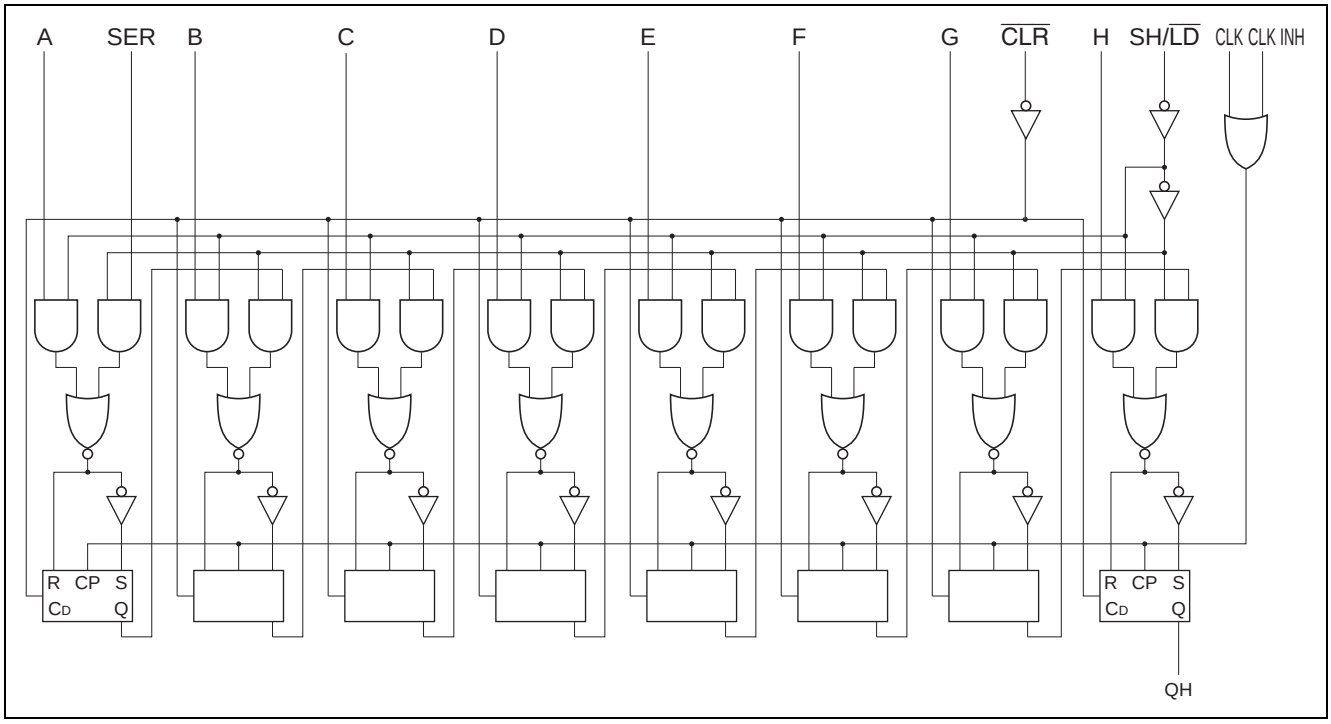
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150℃.

Recommended Operating Conditions

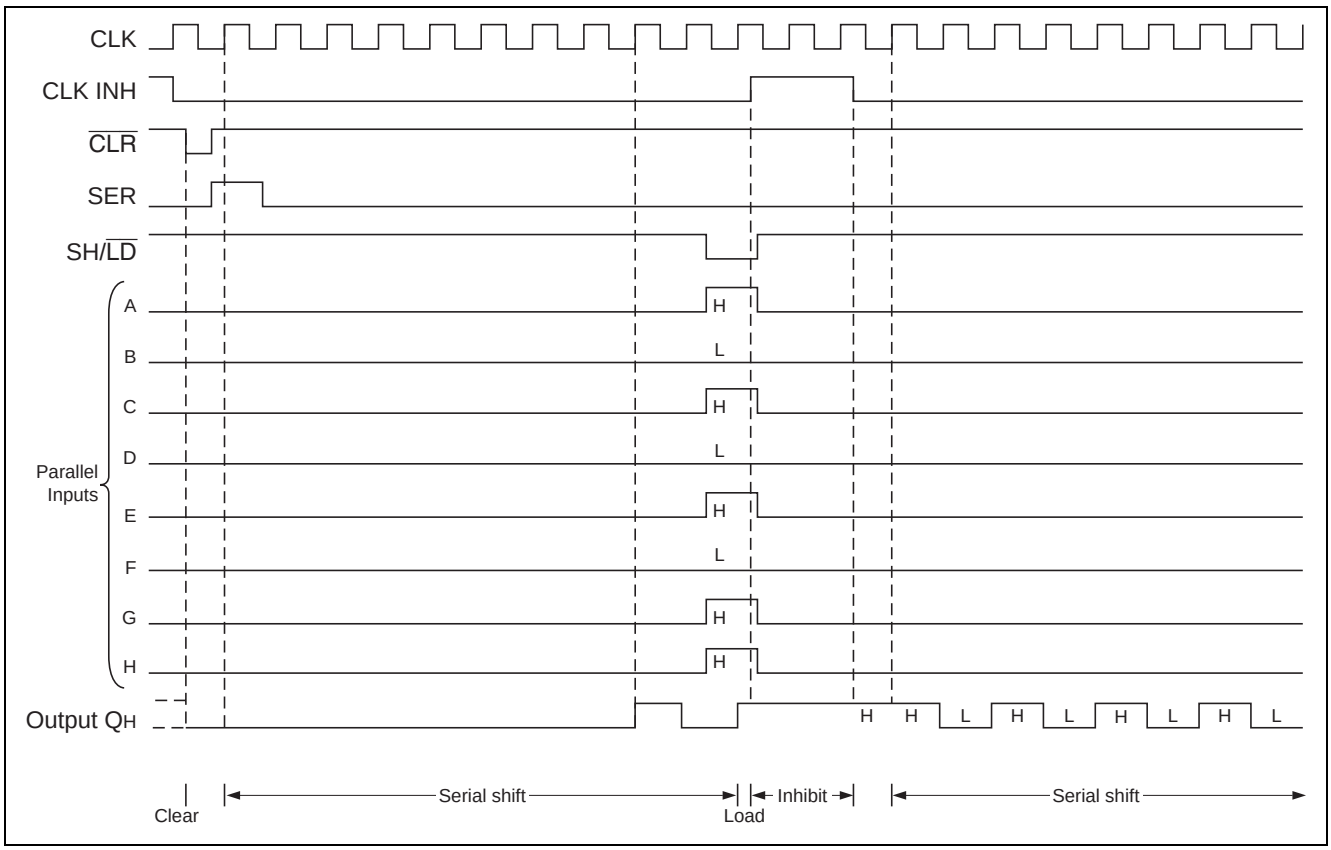
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	–50	μA	V_{CC} = 2.0 V
		—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	–6		V_{CC} = 3.0 to 3.6 V
		—	–12		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	50	μA	V_{CC} = 2.0 V
		—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	6		V_{CC} = 3.0 to 3.6 V
		—	12		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	Δt /Δv	0	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	100		V_{CC} = 3.0 to 3.6 V
		0	20		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	–40	85	℃	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

(Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OL} = –50 μA
		2.3	2.0	—	—		I_{OL} = –2 mA
		3.0	2.48	—	—		I_{OL} = –6 mA
		4.5	3.8	—	—		I_{OL} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 μA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 6 mA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	μA	V_I = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	μA	$V_I = V_{CC}$ or GND, I_O = 0
Output leakage current	I_{OFF}	0	—	—	5	μA	V_I or V_O = 0 V to 5.5 V
Input capacitance	C_{IN}	3.3	—	1.7	—	pF	$V_I = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

(V_{CC} = 2.5 ± 0.2 V)

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	50	80	—	45	—	MHz	C_L = 15 pF		
		40	65	—	35	—		C_L = 50 pF		
Propagation delay time	t_{PLH}/t_{PHL}	—	12.2	19.8	1.0	22.0	ns	C_L = 15 pF	CLK	Q_H
		—	15.3	23.3	1.0	26.0		C_L = 50 pF		
	t_{PHL}	—	10.8	16.0	1.0	18.0		C_L = 15 pF	$\overline{CLR}$	
		—	14.2	19.5	1.0	22.0		C_L = 50 pF		
Setup time	t_{su}	6.0	—	—	7.0	—	ns		$\overline{CLR}$ inactive before CLK ↑	
		7.0	—	—	7.0	—			CLK INH before CLK ↑	
		6.5	—	—	8.5	—			Data before CLK ↑	
		7.0	—	—	8.5	—			SH/$\overline{LD}$ high before CLK ↑	
		8.5	—	—	9.5	—			SER before CLK ↑	
Hold time	t_h	–0.5	—	—	0.0	—	ns		PAR data after SH/$\overline{LD}$ ↑	
		–0.5	—	—	0.0	—			SER data after CLK ↑	
		–0.5	—	—	0.0	—			SH/LD high after CLK ↑	
Pulse width	t_w	8.0	—	—	9.0	—	ns		$\overline{CLR}$ low	
		8.5	—	—	9.0	—			CLK H or L	

(V_{CC} = 3.3 ± 0.3 V)

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	65	115	—	55	—	MHz	C_L = 15 pF		
		60	90	—	50	—		C_L = 50 pF		
Propagation delay time	t_{PLH}/t_{PHL}	—	8.6	15.4	1.0	18.0	ns	C_L = 15 pF	CLK	Q_H
		—	10.9	18.9	1.0	21.5		C_L = 50 pF		
	t_{PHL}	—	7.9	12.5	1.0	15.0		C_L = 15 pF	$\overline{CLR}$	
		—	10.4	16.3	1.0	18.5		C_L = 50 pF		
Setup time	t_{su}	4.0	—	—	4.0	—	ns		$\overline{CLR}$ inactive before CLK ↑	
		5.0	—	—	5.0	—			CLK INH before CLK ↑	
		5.0	—	—	6.0	—			Data before CLK ↑	
		5.0	—	—	6.0	—			SH/$\overline{LD}$ high before CLK ↑	
		5.0	—	—	6.0	—			SER before CLK ↑	
Hold time	t_h	0.0	—	—	0.0	—	ns		PAR data after SH/$\overline{LD}$ ↑	
		0.0	—	—	0.0	—			SER data after CLK ↑	
		0.0	—	—	0.0	—			SH/LD high after CLK ↑	
Pulse width	t_w	6.0	—	—	7.0	—	ns		$\overline{CLR}$ low	
		6.0	—	—	7.0	—			CLK H or L	

Switching Characteristics (cont)

(V_{CC} = 5.0 ± 0.5 V)

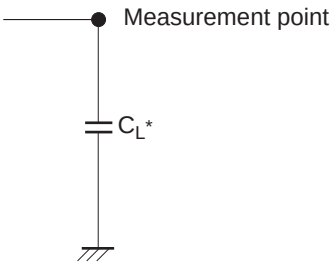
Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	110	165	—	90	—	MHz	C_L = 15 pF		
		95	125	—	85	—		C_L = 50 pF		
Propagation delay time	t_{PLH}/t_{PHL}	—	6.0	9.9	1.0	11.5	ns	C_L = 15 pF	CLK	Q_H
		—	7.7	11.9	1.0	13.5		C_L = 50 pF		
	t_{PHL}	—	5.4	8.6	1.0	10.0		C_L = 15 pF	$\overline{CLR}$	
		—	6.9	10.6	1.0	12.0		C_L = 50 pF		
Setup time	t_{su}	3.5	—	—	3.5	—	ns		$\overline{CLR}$ inactive before CLK ↑	
		3.5	—	—	3.5	—			CLK INH before CLK ↑	
		4.5	—	—	4.5	—			Data before CLK ↑	
		4.0	—	—	4.0	—			SH/$\overline{LD}$ high before CLK ↑	
		4.0	—	—	4.0	—			SER before CLK ↑	
Hold time	t_h	1.0	—	—	1.0	—	ns		PAR data after SH/$\overline{LD}$ ↑	
		1.0	—	—	1.0	—			SER data after CLK ↑	
		1.0	—	—	1.0	—			SH/LD high after CLK ↑	
Pulse width	t_w	5.0	—	—	5.0	—	ns		$\overline{CLR}$ low	
		4.0	—	—	4.0	—			CLK H or L	

Operating Characteristics

(C_L = 50 pF)

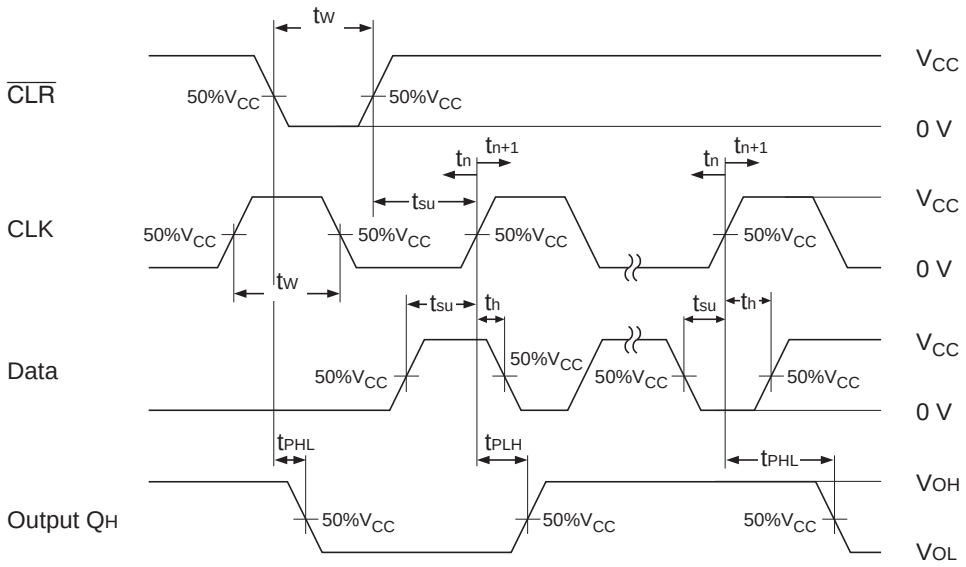
Item	Symbol	V_{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	36.1	—	pF	f = 10 MHz
		5.0	—	37.5	—		

Test Circuit



Note: C_L includes the probe and jig capacitance.

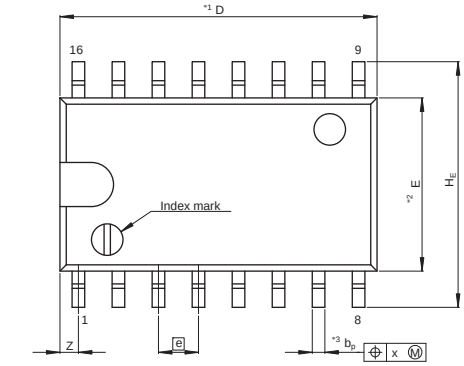
Waveforms

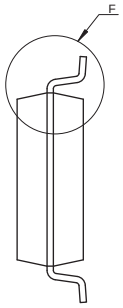


Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, $t_r \leq 3$ ns, $t_f \leq 3$ ns
2. The output are measured one at a time with one transition per measurement.

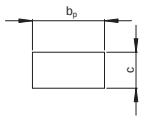
Package Dimensions

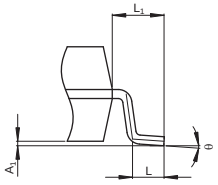
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g





Terminal cross section
(Ni/Pd/Au plating)



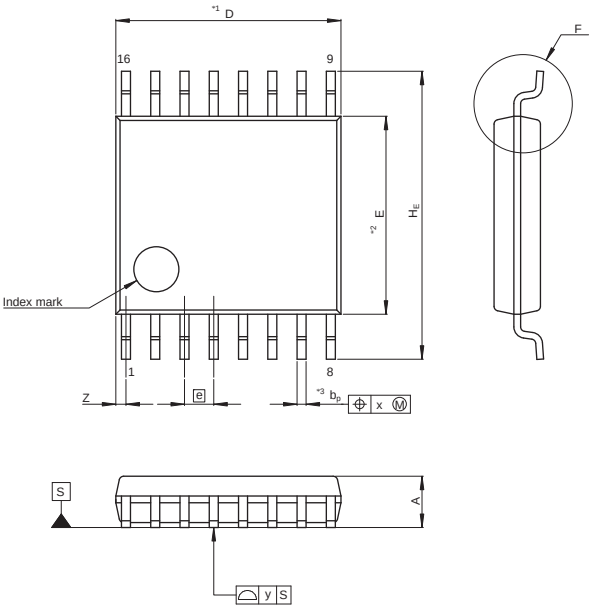


Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP16-4.4x5-0.65	PTSP0016JB-A	TTP-16DAV	0.05g



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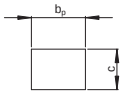
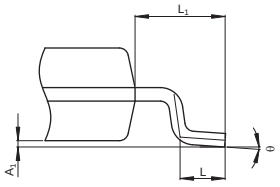
(Ni/Pd/Au plating)





Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.0	5.3
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L_1	—	1.0	—

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