To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

DATA SHEET

MOS FIELD EFFECT TRANSISTOR

NP82N055ELE, NP82N055KLE NP82N055CLE, NP82N055DLE, NP82N055MLE, NP82N055NLE

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

<R> **ORDERING INFORMATION**

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP82N055ELE-E1-AY Note1, 2	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZJ) typ. 1.4 g
NP82N055ELE-E2-AY Note1, 2			
NP82N055KLE-E1-AY Note1			TO-263 (MP-25ZK) typ. 1.5 g
NP82N055KLE-E2-AY Note1			
NP82N055CLE-S12-AZ Note1, 2	Sn-Ag-Cu	Tube 50 p/tube	TO-220 (MP-25) typ. 1.9 g
NP82N055DLE-S12-AY Note1, 2	Pure Sn (Tin)		TO-262 (MP-25 Fin Cut) typ. 1.8 g
NP82N055MLE-S18-AY Note1			TO-220 (MP-25K) typ. 1.9 g
NP82N055NLE-S18-AY Note1			TO-262 (MP-25SK) typ. 1.8 g

Notes 1. Pb-free (This product does not contain Pb in the external electrode.)

2. Not for new design

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance

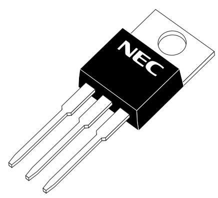
  $R_{DS(on)1}$ = 8.4 mΩ MAX. (V_{GS} = 10 V, I_D = 41 A)

  $R_{DS(on)2}$ = 11 mΩ MAX. (V_{GS} = 5.0 V, I_D = 41 A)

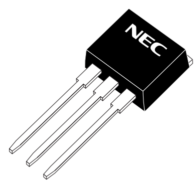
  $R_{DS(on)3}$ = 12 mΩ MAX. (V_{GS} = 4.5 V, I_D = 41 A)
- Low input capacitance

  C_{iss} = 4400 pF TYP.
- Built-in gate protection diode

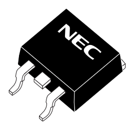
(TO-220)



(TO-262)



(TO-263)



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Date Published October 2007 NS
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C) **Note1**	$I_{D(DC)}$	±82	A
Drain Current (Pulse) **Note2**	$I_{D(pulse)}$	±300	A
Total Power Dissipation (T_C = 25°C)	P_T	163	W
Total Power Dissipation (T_A = 25°C)	P_T	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current **Note3**	I_{AS}	72/50/17	A
Single Avalanche Energy **Note3**	E_{AS}	51/250/289	mJ

Notes 1. Calculated constant current according to MAX. allowable channel temperature.

2. PW ≤ 10 μs, Duty cycle ≤ 1%

3. Starting T_{ch} = 25°C, V_{DD} = 28 V, R_G = 25 Ω, V_{GS} = 20 → 0 V (see **Figure 4.**)

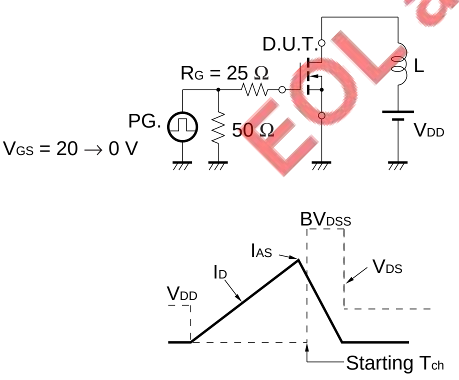
THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.92	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

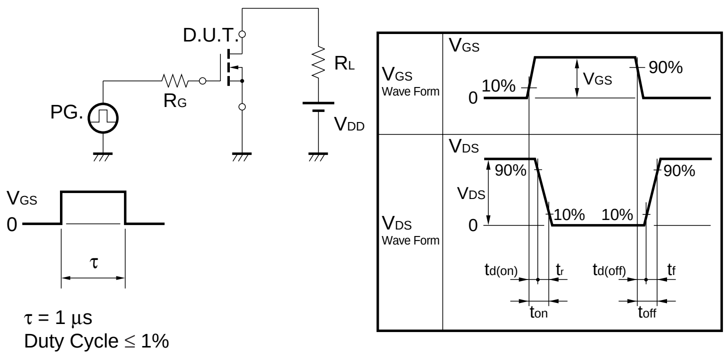
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = 10 V, I_D = 41 A	24	50		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 41 A		6.7	8.4	mΩ
	$R_{DS(on)2}$	V_{GS} = 5.0 V, I_D = 41 A		7.9	11	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.5 V, I_D = 41 A		8.4	12	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V,		4400	6600	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		550	830	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		270	490	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 28 V, I_D = 41 A,		28	61	ns
Rise Time	t_r	V_{GS} = 10 V,		16	39	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 1 Ω		92	180	ns
Fall Time	t_f			18	45	ns
Total Gate Charge	Q_{G1}	I_D = 82 A, V_{DD} = 44 V, V_{GS} = 10 V		80	120	nC
	Q_{G2}	V_{DD} = 44 V,		45	68	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5.0 V,		15		nC
Gate to Drain Charge	Q_{GD}	I_D = 82 A		24		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 82 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 82 A, V_{GS} = 0 V,		47		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		66		nC

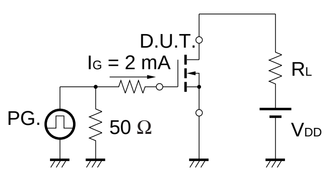
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

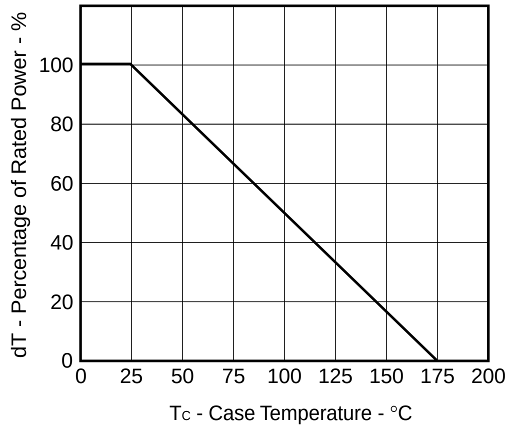


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

Figure.3 FORWARD BIAS SAFE OPERATING AREA

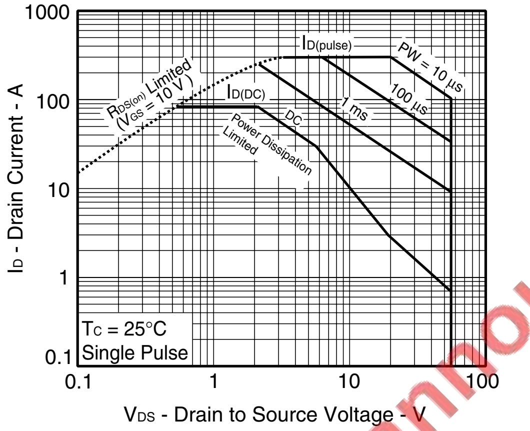


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

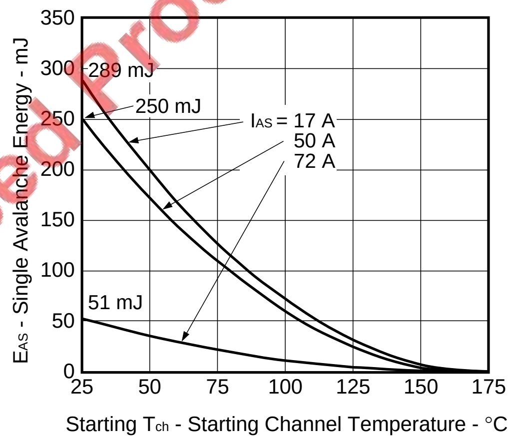


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

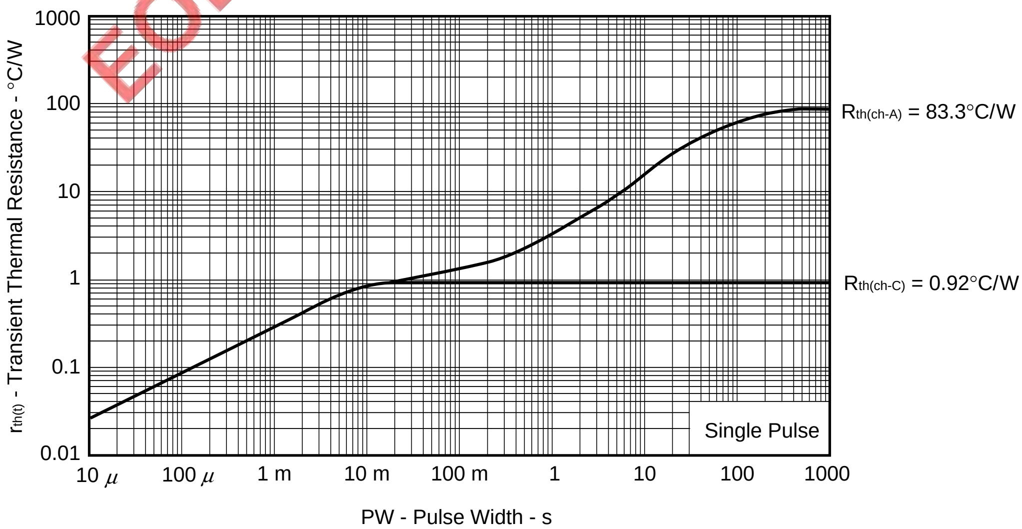


Figure6. FORWARD TRANSFER CHARACTERISTICS

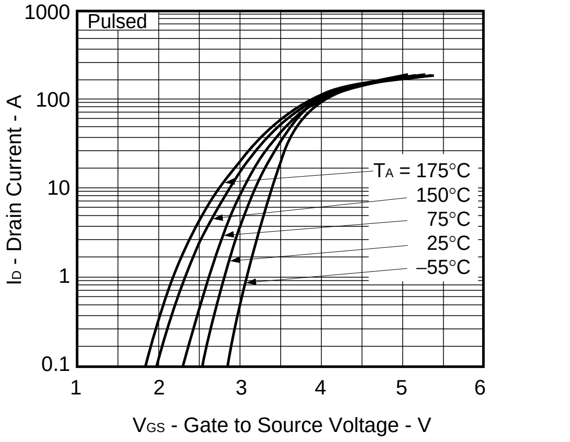


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

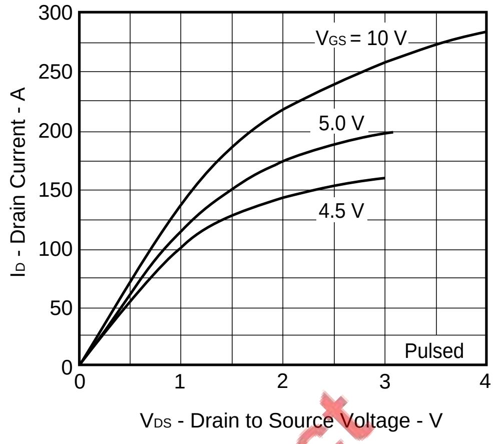


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

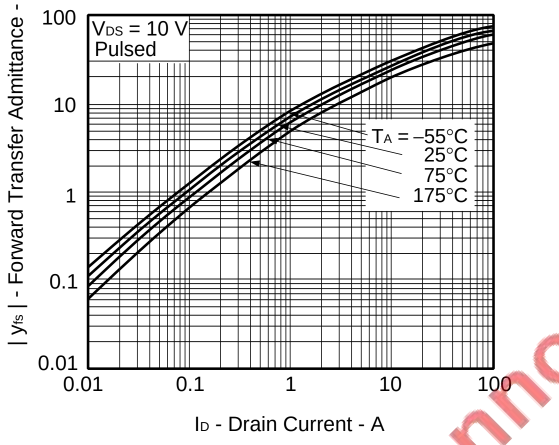


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

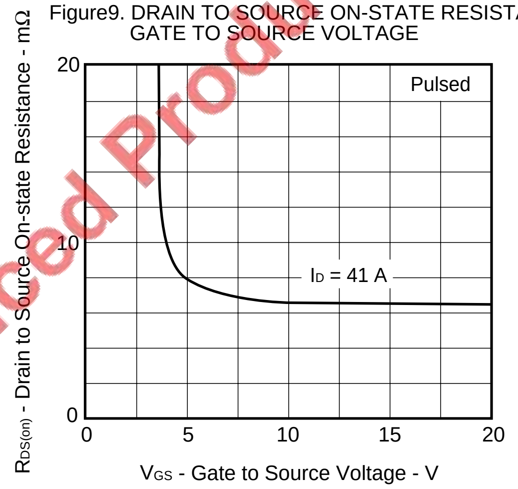


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

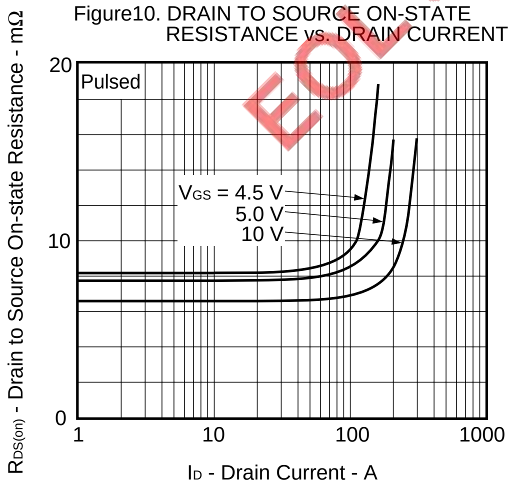


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

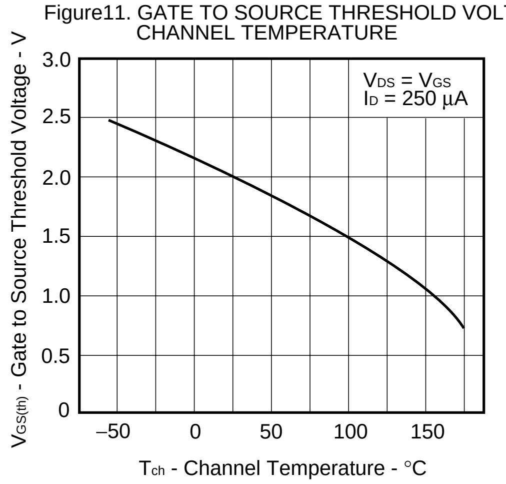


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

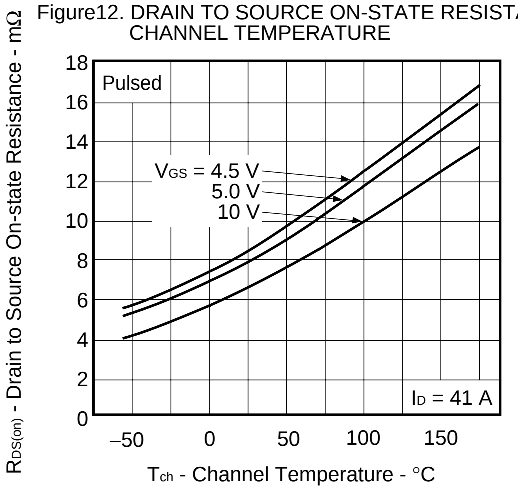


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

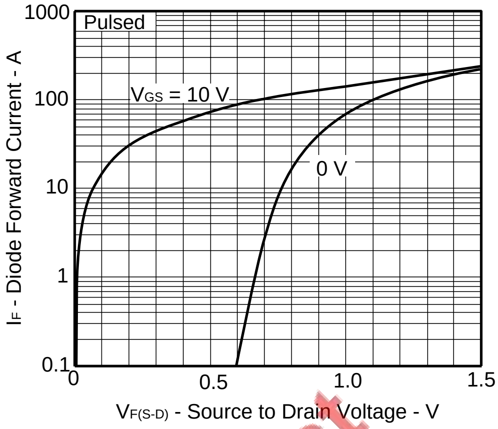


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

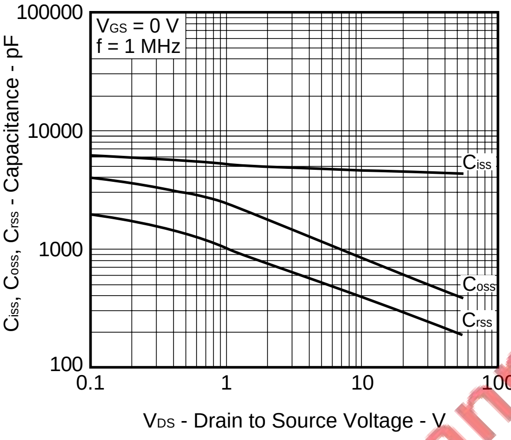


Figure15. SWITCHING CHARACTERISTICS

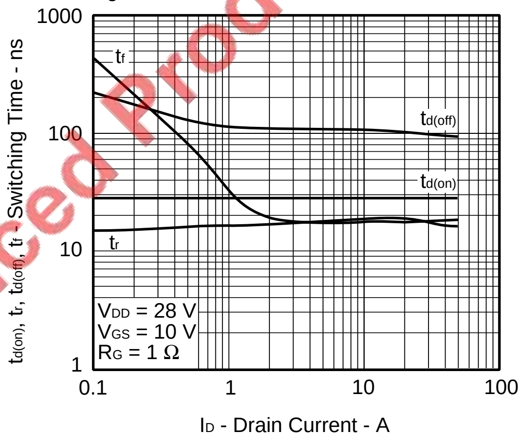


Figure16. REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

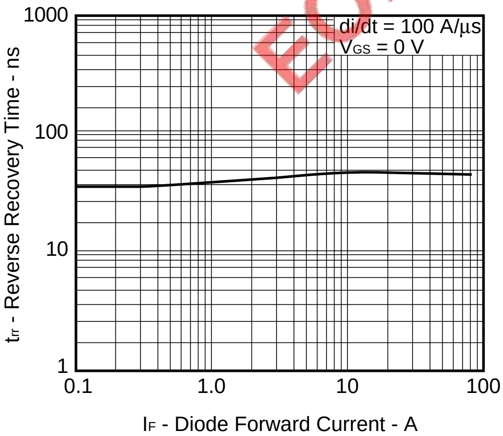
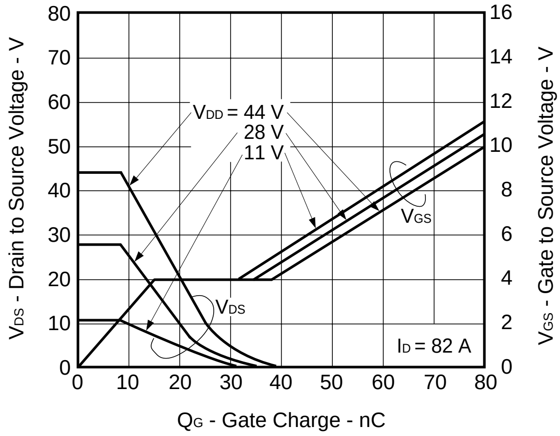
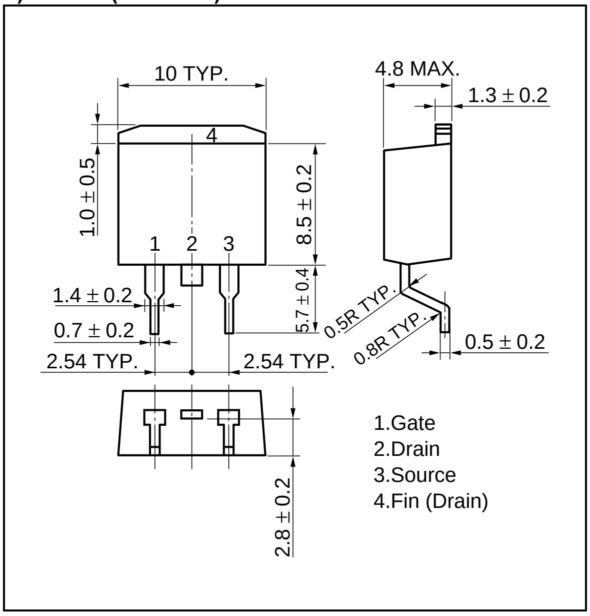


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

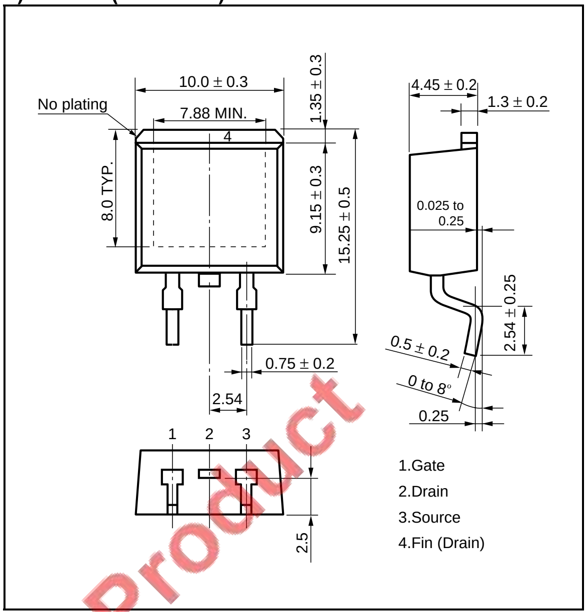


<R> **PACKAGE DRAWINGS (Unit: mm)**

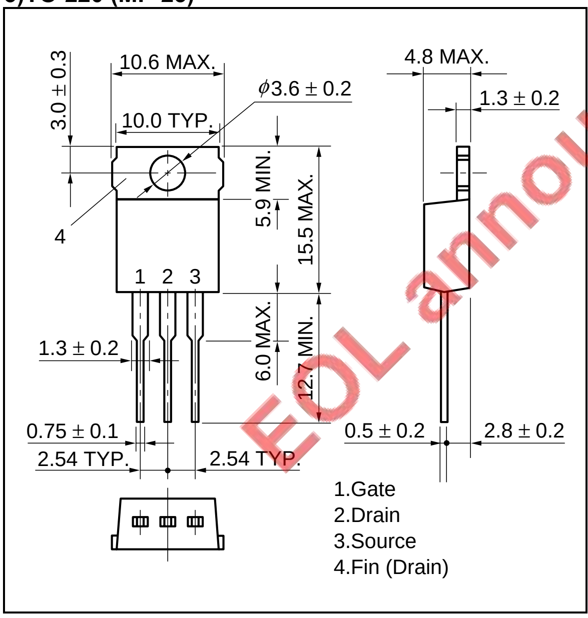
1)TO-263 (MP-25ZJ) Note



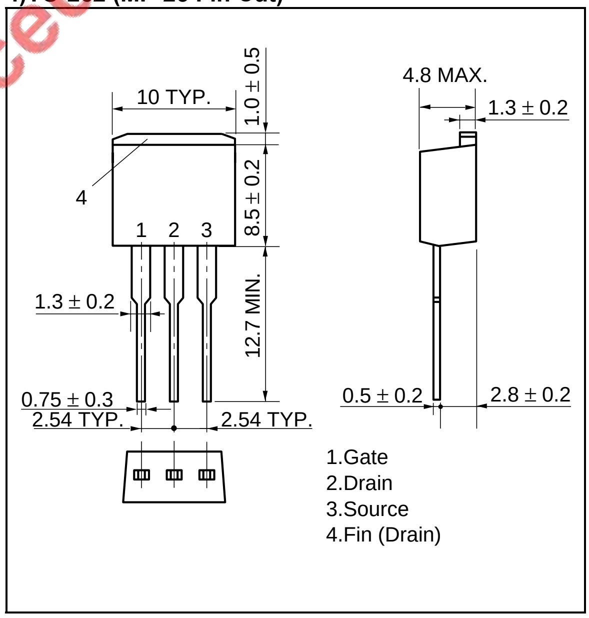
2)TO-263 (MP-25ZK)



3)TO-220 (MP-25) Note

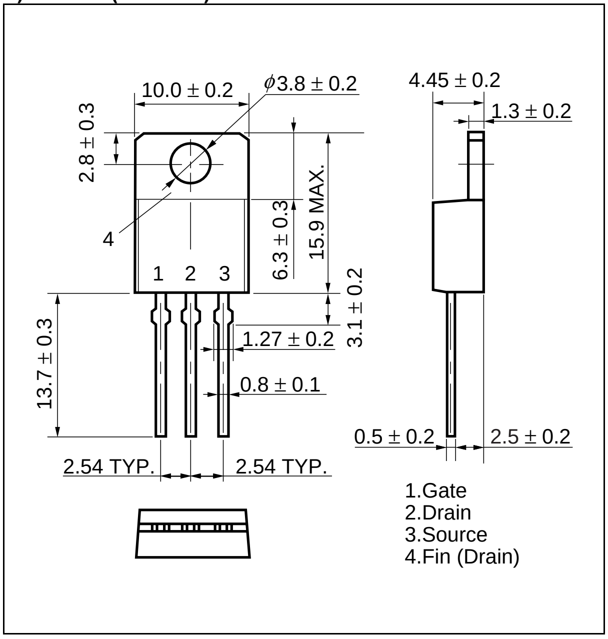


4)TO-262 (MP-25 Fin Cut) Note

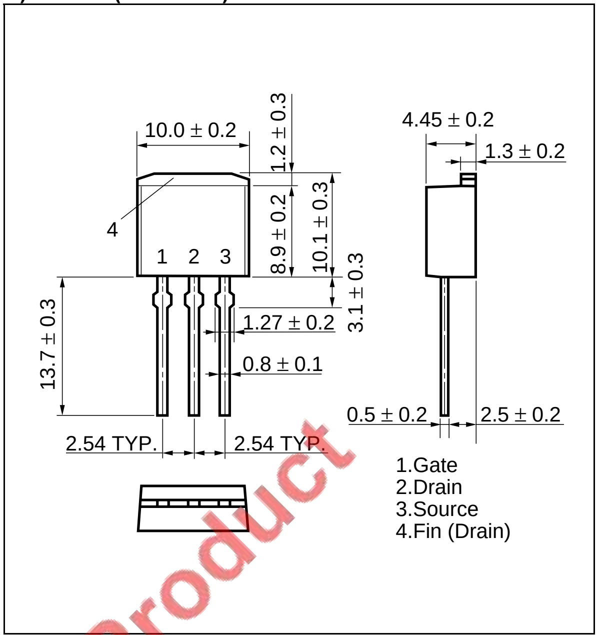


Note Not for new design

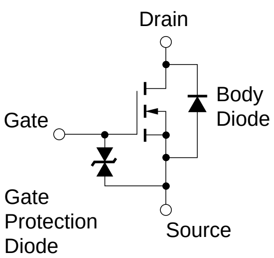
5)TO-220 (MP-25K)



6)TO-262 (MP-25SK)



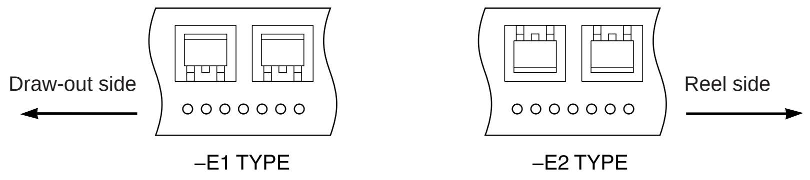
EQUIVALENT CIRCUIT



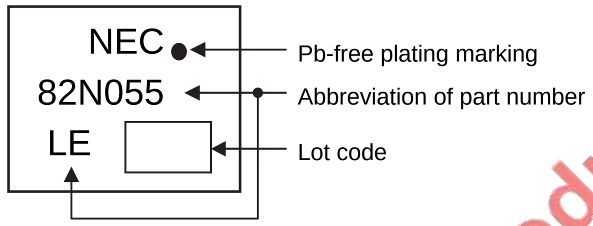
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

<R> TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



<R> MARKING INFORMATION



<R> RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow MP-25ZJ, MP-25ZK	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Wave soldering MP-25, MP-25K, MP-25SK, MP-25 Fin Cut	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating MP-25ZJ, MP-25ZK, MP-25K, MP-25SK	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350
Partial heating MP-25, MP-25 Fin Cut	Maximum temperature (Pin temperature): 300°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P300

Caution Do not use different soldering methods together (except for partial heating).