19-3361; Rev 3; 7/10

MAXIM

Dual, Quad, and Hex High-Speed Differential ESD-Protection ICs

General Description

The MAX3205E/MAX3207E/MAX3208E low-capacitance, ±15kV ESD-protection diode arrays with an integrated transient voltage suppressor (TVS) clamp are suitable for high-speed and general-signal ESD protection. Low input capacitance makes these devices ideal for ESD protection of signals in HDTV, PC monitors (DVI™, HDMI®), PC peripherals (FireWire®, USB 2.0), server interconnect (PCI Express®, InfiniBand™), datacom, and interchassis interconnect. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND.

The MAX3205E/MAX3207E/MAX3208E protect against ESD pulses up to ±15kV Human Body Model, ±8kV Contact Discharge, and ±15kV Air-Gap Discharge, as specified in IEC 61000-4-2. An integrated TVS ensures that the voltage rise seen on V_{CC} during an ESD event is clamped to a known voltage. These devices have a 2pF input capacitance per channel, and a channel-to-channel capacitance variation of only 0.05pF, making them ideal for use on high-speed, single-ended, or differential signals.

The MAX3207E is a two-channel device suitable for USB 1.1, USB 2.0 (480Mbps), and USB OTG applications. The MAX3208E is a four-channel device for Ethernet and FireWire applications. The MAX3205E is a six-channel device for cell phone connectors and SVGA video connections.

The MAX3205E is available in 9-bump, tiny wafer-level package (WLP) and 16-pin, 3mm x 3mm, thin QFN packages. The MAX3207E is available in a small 6-pin SOT23 package. The MAX3208E is available in 10-pin µMAX® and 16-pin, 3mm x 3mm TQFN packages. All devices are specified for the -40°C to +125°C automotive operating temperature range.

Applications

DVI Input/Output Protection

Set-Top Boxes

PDAs/Cell Phones

Graphics Controller Cards

Displays/Projectors

High-Speed, Full-Speed and Low-Speed USB Port Protection

FireWire IEEE 1394 Ports

Consumer Equipment

High-Speed Differential Signal Protection

Typical Operating Circuit and Pin Configurations appear at end of data sheet.

Features

- **Low Input Capacitance of 2pF Typical**
- **Low Channel-to-Channel Variation of 0.05pF from I/O to I/O**
- **High-Speed Differential or Single-Ended ESD Protection**
  - **±15kV–Human Body Model**
  - **±8kV–IEC 61000-4-2, Contact Discharge**
  - **±15kV–IEC 61000-4-2, Air-Gap Discharge**
- **Integrated Transient Voltage Suppressor (TVS)**
- **Optimized Pinout for Minimized Stub Inductance on Controlled-Impedance Differential-Transmission Line Routing**
- **-40°C to +125°C Automotive Operating Temperature Range**
- **WLP Packaging Available**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3205EAWL+T	-40°C to +125°C	9 WLP
MAX3205EATE+	-40°C to +125°C	16 TQFN-EP*
MAX3207EAUT+T	-40°C to +125°C	6 SOT23
MAX3208EAUB+	-40°C to +125°C	10 µMAX
MAX3208EATE+	-40°C to +125°C	16 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Selector Guide

PART	ESD-PROTECTED I/O PORTS	TOP MARK
MAX3205EAWL+T	6	AIN
MAX3205EATE+	6	ACO
MAX3207EAUT+T	2	ABVG
MAX3208EAUB+	4	—
MAX3208EATE+	4	ACN

FireWire is a registered trademark of Apple Inc.

PCI Express is a registered service mark of PCI-SIG Corporation.

DVI is a trademark of Digital Display Working Group.

HDMI is a registered trademark and registered service mark of HDMI Licensing, LCC.

InfiniBand is a trademark and service mark of InfiniBand Trade Association.

µMAX is a registered trademark of Maxim Integrated Products, Inc.

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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
I/O_ to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW
9-Bump WLP (derate 14.1mW/°C above +70°C).....0mW
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
16-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (excluding WLP; soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}			0.9		5.5	V
Supply Current	I_{CC}				1	100	nA
Diode Forward Voltage	V_F	I_F = 10mA		0.65		0.95	V
Channel Clamp Voltage (Note 2)	V_C	T_A = +25°C, ±15kV Human Body Model, I_F = 10A	Positive transients			V_{CC} + 25	V
			Negative transients			-25	
		T_A = +25°C, ±8kV Contact Discharge (IEC 61000-4-2), I_F = 24A	Positive transients			V_{CC} + 60	
			Negative transients			-60	
		T_A = +25°C, ±15kV Air-Gap Discharge (IEC 61000-4-2), I_F = 45A	Positive transients			V_{CC} + 100	
			Negative transients			-100	
Channel Leakage Current				-0.1		+0.1	µA
Channel I/O Capacitance		V_{CC} = +3.3V, bias of V_{CC} / 2	MAX3205EAWL+T MAX3207EAUT+T		2.5	3	pF
			MAX3205EATE+ MAX3208EATE+		2.7	3.2	
			MAX3208EAUB+		2.6	3.1	
Channel I/O to I/O Variation in Capacitance	ΔC_{IN}	V_{CC} = +3.3V, bias of V_{CC} / 2, $C_{I/O\_}$ to GND			±0.05		pF
TRANSIENT SUPPRESSOR							
V_{CC} Capacitance to GND					10		pF
ESD Trigger Voltage		dV/dt ≤ 1V/ns (Note 3)			9		V

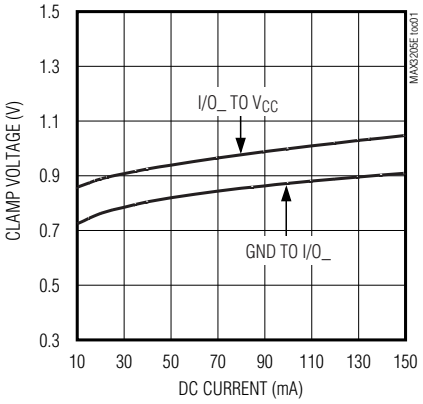
Note 1: Parameters are 100% production tested at +25°C. Limits over temperature are guaranteed by design only.
Note 2: Idealized clamp voltages. See the *Applications Information* section for more information.
Note 3: Guaranteed by design, not production tested.

Dual, Quad, and Hex High-Speed Differential ESD-Protection ICs

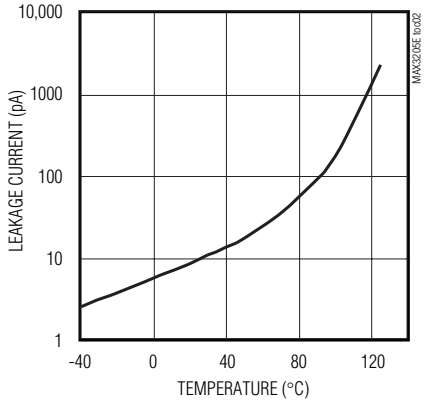
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

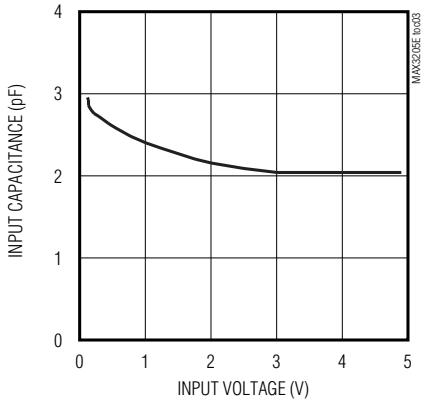
CLAMP VOLTAGE vs. DC CURRENT



LEAKAGE CURRENT vs. TEMPERATURE



INPUT CAPACITANCE vs. INPUT VOLTAGE



Pin Description

PIN					NAME	FUNCTION
MAX3205E		MAX3207E	MAX3208E			
TQFN-EP	WLP	SOT23	µMAX	TQFN-EP		
4, 5, 7, 12, 13, 15	A2, A3, B1, B3, C1, C2	1, 4	1, 4, 6, 9	4, 7, 12, 15	I/O_	ESD-Protected Channel
1, 3, 6, 8, 9, 11, 14, 16	—	3, 6	2, 5, 7, 10	1, 3, 5, 6, 8, 9, 11, 13, 14, 16	N.C.	No Connection. Not internally connected.
—	B2	—	—	—	N.C.	No Connection. The solder sphere is omitted from this location (see the *Package Information* section).
2	A1	2	3	2	GND	Ground. Connect GND with a low-impedance connection to the ground plane.
10	C3	5	8	10	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor as close to the device as possible.
—	—	—	—	—	EP	Exposed Pad (TQFN Only). Connect EP to GND.

Dual, Quad, and Hex High-Speed Differential ESD-Protection ICs

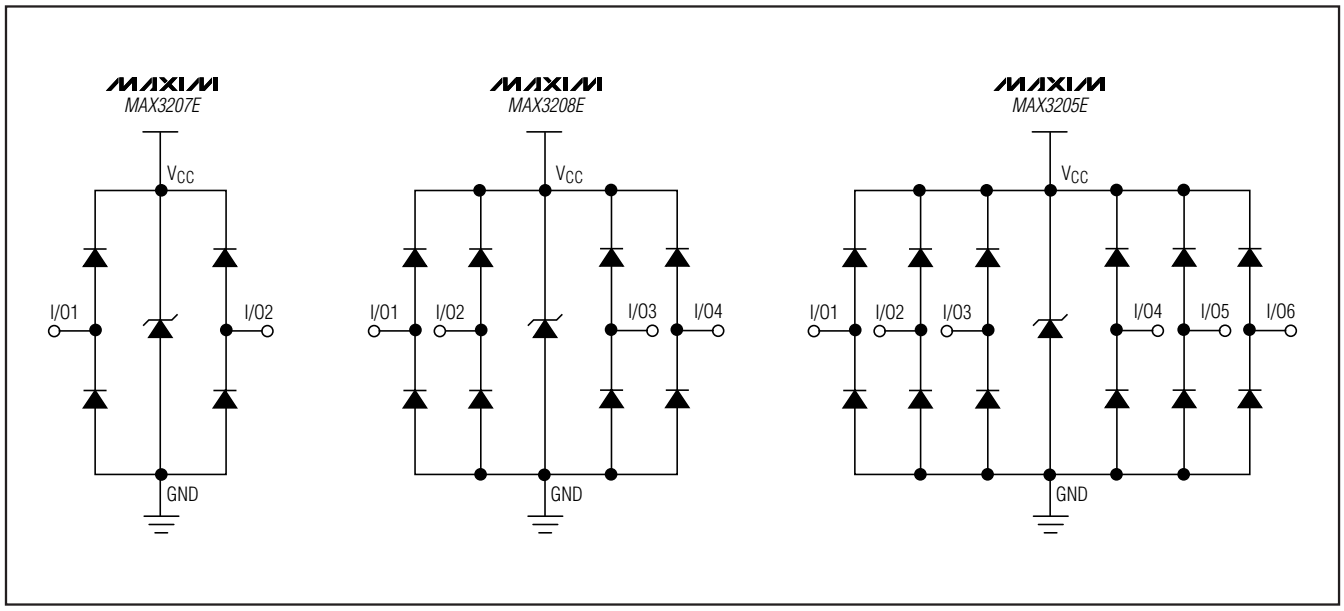
Detailed Description

The MAX3205E/MAX3207E/MAX3208E low-capacitance, ±15kV ESD-protection diode arrays with an integrated transient voltage suppressor (TVS) clamp are suitable for high-speed and general-signal ESD protection. Low input capacitance makes these devices ideal for ESD protection of signals in HDTV, PC monitors (DVI, HDMI), PC peripherals (FireWire, USB 2.0), server interconnect (PCI Express, InfiniBand), datacom, and interchassis interconnect. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The MAX3207E, MAX3208E, and MAX3205E are two, four, and six channels (see the *Functional Diagram*).

The MAX3205E/MAX3207E/MAX3208E are designed to work in conjunction with a device's intrinsic ESD protection. The MAX3205E/MAX3207E/MAX3208E limit the excursion of the ESD event to below ±25V peak voltage when subjected to the Human Body Model waveform. When subjected to the IEC 61000-4-2 waveform and Contact Discharge, the peak voltage is limited to ±60V. The peak voltage is limited to ±100V when subjected to Air-Gap Discharge. The device protected by the MAX3205E/MAX3207E/MAX3208E must be able to withstand these peak voltages, plus any additional voltage generated by the parasitic of the board.

A TVS is integrated into the MAX3205E/MAX3207E/MAX3208E to help clamp ESD to a known voltage. This helps reduce the effects of parasitic inductance on the V_{CC} rail by clamping V_{CC} to a known voltage during an ESD event. For the lowest possible clamp voltage during an ESD event, placing a 0.1µF capacitor as close to V_{CC} as possible is recommended.

Functional Diagram



Applications Information

Design Considerations

Maximum protection against ESD damage results from proper board layout (see the *Layout Recommendations* section). A good layout reduces the parasitic series inductance on the ground line, supply line, and protected signal lines. The MAX3205E/MAX3207E/MAX3208E ESD diodes clamp the voltage on the protected lines during an ESD event and shunt the current to GND or V_{CC}. In an ideal circuit, the clamping voltage (V_C) is defined as the forward voltage drop (V_F) of the protection diode, plus any supply voltage present on the cathode.

For positive ESD pulses:

$$V_C = V_{CC} + V_F$$

For negative ESD pulses:

$$V_C = -V_F$$

The effect of the parasitic series inductance on the lines must also be considered (Figure 1).

For positive ESD pulses:

$$V_C = V_{CC} + V_{F(D1)} + \left(L1 \times \frac{d(I_{ESD})}{dt}\right) + \left(L2 \times \frac{d(I_{ESD})}{dt}\right)$$

For negative ESD pulses:

$$V_C = -\left(V_{F(D2)} + \left(L1 \times \frac{d(I_{ESD})}{dt}\right) + \left(L3 \times \frac{d(I_{ESD})}{dt}\right)\right)$$

where I_{ESD} is the ESD current pulse.

During an ESD event, the current pulse rises from zero to peak value in nanoseconds (Figure 2). For example, in a 15kV IEC 61000 Air-Gap Discharge ESD event, the pulse current rises to approximately 45A in 1ns (di/dt = 45 x 10^9). An inductance of only 10nH adds an additional 450V to the clamp voltage and represents approximately 0.5in of board trace. Regardless of the device's specified diode clamp voltage, a poor layout with parasitic inductance significantly increases the effective clamp voltage at the protected signal line. Minimize the effects of parasitic inductance by placing the MAX3205E/MAX3207E/MAX3208E as close to the connector (or ESD contact point) as possible.

A low-ESR 0.1µF capacitor is recommended between V_{CC} and GND in order to get the maximum ESD protection possible. This bypass capacitor absorbs the charge transferred by a positive ESD event. Ideally, the supply rail (V_{CC}) would absorb the charge caused by a positive ESD strike without changing its regulated value. All power supplies have an effective output impedance on their positive rails. If a power supply's effective output impedance is 1Ω, then by using V = I x R, the clamping voltage of V_C increases by the equation $V_C = I_{ESD} \times R_{OUT}$. A +8kV IEC 61000-4-2 ESD event generates a current spike of 24A. The clamping voltage increases by V_C = 24A x 1Ω, or V_C = 24V. Again, a poor layout without proper bypassing increases the clamping voltage. A ceramic chip capacitor mounted as close as possible to the MAX3205E/MAX3207E/MAX3208E V_{CC} pin is the best choice for this application. A bypass capacitor should also be placed as close to the protected device as possible.

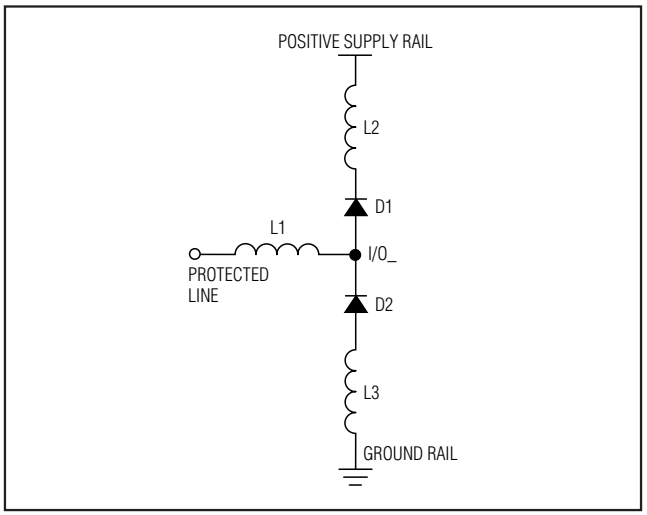


Figure 1. Parasitic Series Inductance

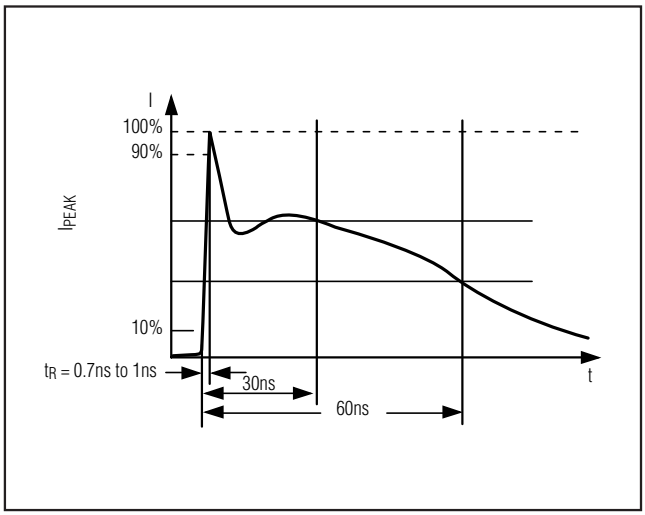


Figure 2. IEC 61000-4-2 ESD Generator Current Waveform

Dual, Quad, and Hex High-Speed Differential ESD-Protection ICs

±15kV ESD Protection

ESD protection can be tested in various ways. The MAX3205E/MAX3207E/MAX3208E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge Method specified in IEC 61000-4-2
- ±15kV using the IEC 61000-4-2 Air-Gap Discharge Method

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX3205E/MAX3207E/MAX3208E help users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 5), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 2 shows the current waveform for the ±8kV, IEC 61000-4-2 Level 4, ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

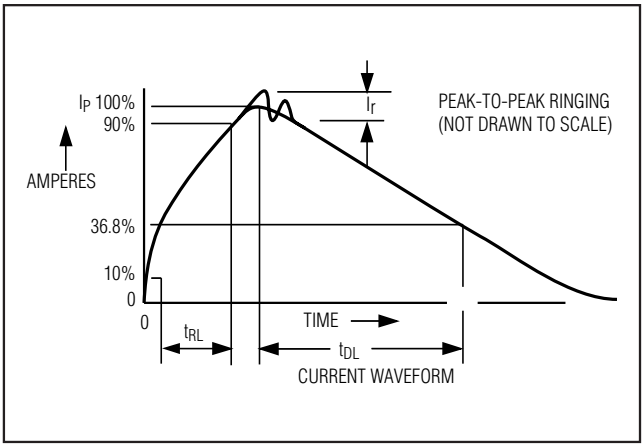


Figure 4. Human Body Model Current Waveform

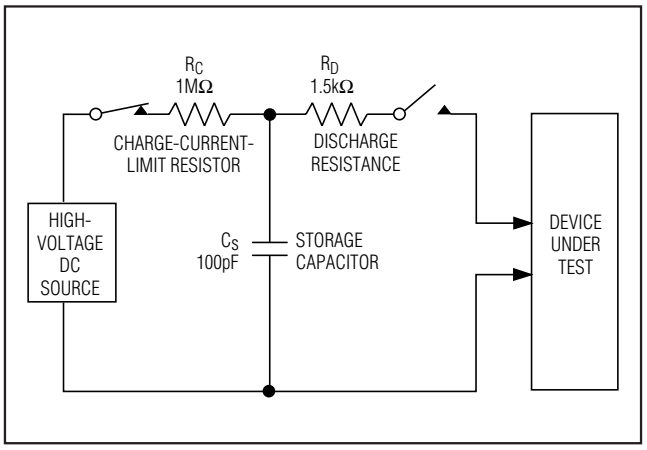


Figure 3. Human Body ESD Test Model

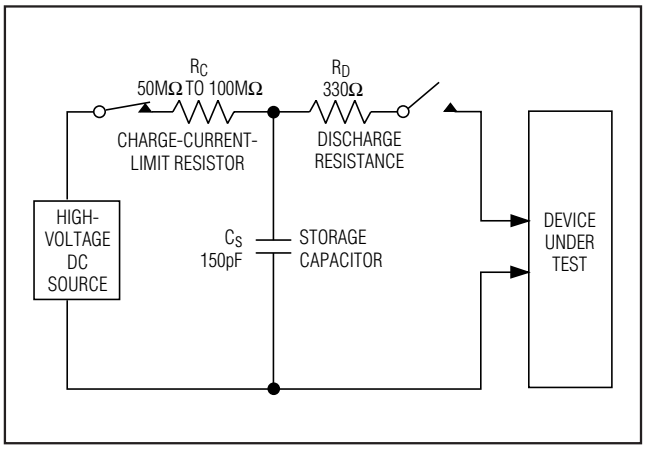


Figure 5. IEC 61000-4-2 ESD Test Model

Layout Recommendations

Proper circuit-board layout is critical to suppress ESD-induced line transients (See Figure 6). The MAX3205E/MAX3207E/MAX3208E clamp to 100V; however, with improper layout, the voltage spike at the device can be much higher. A lead inductance of 10nH with a 45A current spike results in an additional 450V spike on the protected line. It is essential that the layout of the PC board follows these guidelines:

1) Minimize trace length between the connector or input terminal, I/O_, and the protected signal line.
2) Use separate planes for power and ground to reduce parasitic inductance and to reduce the impedance to the power rails for shunted ESD current.
3) Ensure short low-inductance ESD transient return paths to GND and V_{CC}.
4) Minimize conductive power and ground loops.
5) Do not place critical signals near the edge of the PC board.
6) Bypass V_{CC} to GND with a low-ESR ceramic capacitor as close to V_{CC} as possible.
7) Bypass the supply of the protected device to GND with a low-ESR ceramic capacitor as close to the supply pin as possible.

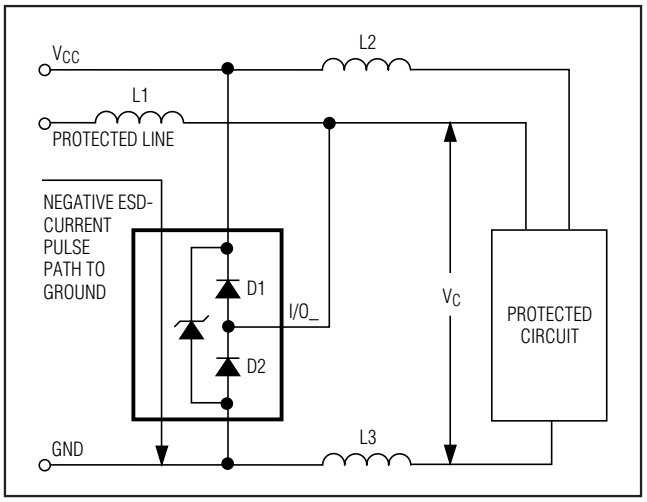


Figure 6. Layout Considerations

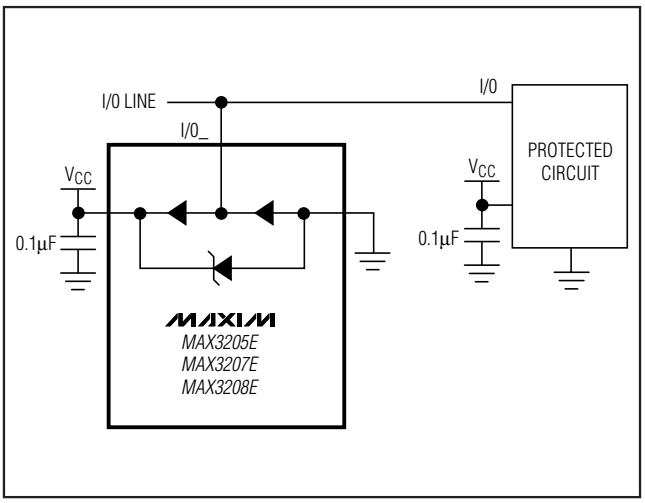
WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*.

Chip Information

PROCESS: BiCMOS

Typical Operating Circuit



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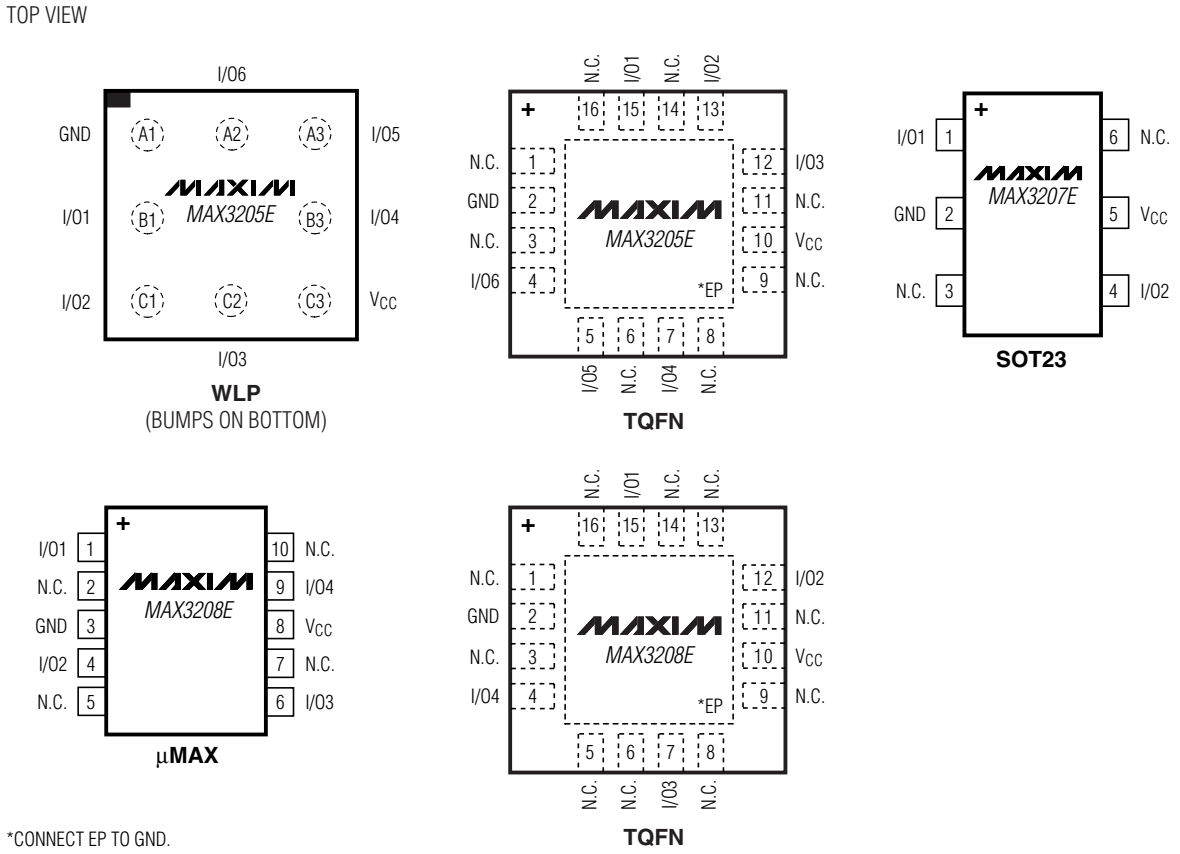
Pin Configurations



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91B1+5	21-0067	—
16 TQFN-EP	T1633+4	21-0136	90-0031
6 SOT23	U6+1	21-0058	90-0175
10 µMAX	U10+2	21-0061	90-0330

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	7/10	Changed the 9 UCSP package to a 9 WLP package in the *Ordering Information* table, *Absolute Maximum Ratings*, *Pin Description* table, and the *Pin Configurations*; changed leaded packages to lead-free packages in the *Ordering Information* table; changed the MAX3205EAWL+T part number and its top mark in the *Selector Guide*; deleted all information in the *Chip Information* section except “Process: BiCMOS”	1, 2, 3, 7, 8