Precision Monolithic Low-Voltage CMOS Analog Switches

DESCRIPTION

The DG417L, DG418L, DG419L are low voltage pin-for-pin compatible companion devices to the industry standard DG417, DG418, DG419 with improved performance.

Using BiCMOS wafer fabrication technology allows the DG417L, DG418L, DG419L to operate on single and dual supplies. Single supply voltage ranges from 3 V to 12 V while dual supply operation is recommended with ± 3 V to ± 6 V.

Combining high speed (t_{ON}: 28 ns), flat R_{ON} over the analog signal range (6 Ω), minimal insertion lose (up to 100 MHz), and excellent crosstalk and off-isolation performance (- 70 dB at 1 MHz), the DG417L, DG418L, DG419L are ideally suited for audio and video signal switching.

The DG417L and DG418L respond to opposite control logic as shown in the truth table. The DG419L has an SPDT configuration.

FEATURES

- 2.7 V- thru 12 V single supply or ± 3- thru ± 6 dual supply
- On-resistance - R_{ON}: 14 Ω
- Fast switching - t_{ON}: 28 ns
  - t_{OFF}: 13 ns
- TTL, CMOS compatible
- Low leakage: < 100 pA
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available

RoHS* Available

APPLICATIONS

- Precision automatic test equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals
- SDSL, DSLAM
- Audio and video signal routing

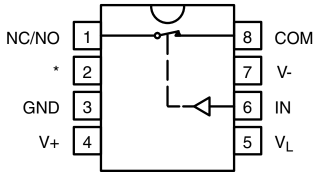
BENEFITS

- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG417L, DG418L

Dual-In-Line, MSOP-8 and SOIC-8

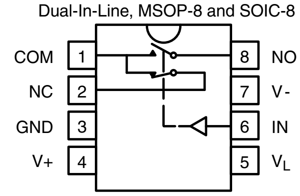


Top View

* Not Connected

DG419L

Dual-In-Line, MSOP-8 and SOIC-8



Top View

TRUTH TABLE

Logic	DG417L	DG418L
0	ON	OFF
1	OFF	ON

TRUTH TABLE (DG419L)

Logic	NC	NO
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION (DG417L, DG418L)

Temp. Range	Package	Part Number
	8-Pin Narrow SOIC	DG417LDY DG417LDY-E3 DG417LDY-T1 DG417LDY-T1-E3
		DG418LDY DG418LDY-E3 DG418LDY-T1 DG418LDY-T1-E3
	8-Pin MSOP	DG417LDQ-T1-E3
		DG418LDQ-T1-E3

ORDERING INFORMATION (DG419L)

Temp. Range	Package	Part Number
- 40 °C to 85 °C	8-Pin Narrow SOIC	DG419LDY DG419LDY-E3 DG419LDY-T1 DG419LDY-T1-E3
	8-Pin MSOP	DG419LDQ-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V+ to V-		- 0.3 to 13	V
GND to V-		7	
V_L		(GND - 0.3) to (V+) + 0.3	
I_N, COM, NC, NO[a]		- 0.3 to (V+ + 0.3) or 30 mA, whichever occurs first	
Continuous Current (Any Terminal)		30	mA
Peak Current, S or D (Pulsed 1 ms, 10 % Duty Cycle)		100	
Storage Temperature	(AK, DQ, DY Suffix)	- 65 to 150	°C
Power Dissipation (Packages)[b]	8-Pin MSOP[c]	320	mW
	8-Pin SOIC[c]	400	
	8-Pin CerDIP[d]	600	

Notes:
a. Signals on NC, NO, COM, or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.5 mW/°C above 25 °C.
d. Derate 12 mW/°C above 75 °C.

SPECIFICATIONS (Single Supply 12 V)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix Limits - 55 °C to 125 °C Min.[d]	A Suffix Limits Max.[d]	D Suffix Limits - 40 °C to 85 °C Min.[d]	D Suffix Limits Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
On-Resistance	R_{ON}	V+ = 10.8 V, V- = 0 V I_{NO}, I_{NC} = 5 mA, V_{COM} = 2 V / 9 V	Room Full	13		20 32		20 23.5	Ω
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V_{COM} = 1 V / 11 V V_{NO}, V_{NC} = 11 V / 1 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	$I_{COM(off)}$		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current	$I_{COM(on)}$	V_{NO}, V_{NC} = V_{COM} = 11 V / 1 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Input Current	I_{INL} or I_{INH}		Full	0.01	- 1.5	1.5	- 1	1	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 5 V, see figure 2	Room Full	28		43 50		43 46	ns
Turn-Off Time	t_{OFF}		Room Full	13		31 35		31 32	
Break-Before-Make Time Delay	t_D	DG419L only, V_{NC}, V_{NO} = 5 V R_L = 300 Ω, C_L = 35 pF	Room	13					
Charge Injection[e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	1					pC
Off-Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF , f = 1 MHz	Room	- 71					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	- 71					
Source Off Capacitance[e]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room	5					pF
Channel-On Capacitance[e]	C_{ON}		Room	15					
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 or V_L	Room Full	0.02		1 7.5		1 5	µA
Negative Supply Current	I-		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		
Logic Supply Current	I_L		Room Full	0.002		1 7.5		1 5	
Ground Current	I_{GND}		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		

SPECIFICATIONS (Dual Supply ± 5 V)									
		Test Conditions Unless Otherwise Specified $V+ = 5$ V, $V- = -5$ V			**A Suffix Limits** - 55 °C to 125 °C		**D Suffix Limits** - 40 °C to 85 °C		
Parameter	**Symbol**	$V_L = 5$ V, $V_{IN} = 2.4$ V, 0.8 V[f]	**Temp.**[b]	**Typ.**[c]	**Min.**[d]	**Max.**[d]	**Min.**[d]	**Max.**[d]	**Unit**
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		- 5	5	- 5	5	V
On-Resistance	R_{ON}	$V+ = 5$ V, $V- = -5$ V I_{NO}, $I_{NC} = 5$ mA, $V_{COM} = \pm 3.5$ V	Room Full	14		18.5 30		18.5 21	Ω
Switch Off Leakage Current[a]	$I_{NO(off)}$ $I_{NC(off)}$	$V+ = 5.5$, $V- = -5.5$ V $V_{COM} = \pm 4.5$ V V_{NO}, $V_{NC} = \pm 4.5$ V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	$I_{COM(off)}$		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current[a]	$I_{COM(on)}$	$V+ = 5.5$ V, $V- = -5.5$ V V_{NO}, $V_{NC} = V_{COM} = \pm 4.5$ V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Input Current[a]	I_{INL} or I_{INH}		Full	0.05	- 1.5	1.5	- 1	1	µA
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	$R_L = 300$ Ω, $C_L = 35$ pF V_{NO}, $V_{NC} = \pm 3.5$ V, see figure 2	Room Full	30		41 50		41 44	ns
Turn-Off Time[e]	t_{OFF}		Room Full	16		32 36		32 33	
Break-Before-Make Time Delay[e]	t_D	DG419L only, V_{NO}, $V_{NC} = 3.5$ V $R_L = 300$ Ω, $C_L = 35$ pF	Room	10					
TransitionTime	t_{TRANS}	$R_L = 300$ Ω, $C_L = 35$ pF $V_{S1} = \pm 3.5$ V, $V_{S2} = \pm 3.5$ V	Room	33		47		47	
Charge Injection[e]	Q_{INJ}	$V_g = 0$ V, $R_g = 0$ Ω, $C_L = 1$ nF	Room	3					pC
Off-Isolation[e]	OIRR	$R_L = 50$ Ω, $C_L = 5$ pF, f = 1 MHz	Room	- 71					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	- 76					
Source Off Capacitance[e]	$C_{NO(off)}$ $C_{NC(off)}$	f = 1 MHz	Room	5.2					pF
Channel-On Capacitance[e]	C_{ON}		Room	15					
Power Supplies									
Positive Supply Current[e]	I+	$V_{IN} = 0$ or V_L	Room Full	0.03		1 7.5		1 5	µA
Negative Supply Current[e]	I-		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		
Logic Supply Current[e]	I_L		Room Full	0.002		1 7.5		1 5	
Ground Current[e]	I_{GND}		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		

SPECIFICATIONS (Single Supply 5 V)									
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 5 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**Typ.**[c]	**A Suffix Limits** - 55 °C to 125 °C **Min.**[d]	**A Suffix Limits** - 55 °C to 125 °C **Max.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Min.**[d]	**D Suffix Limits** - 40 °C to 85 °C **Max.**[d]	**Unit**
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full			5		5	V
On-Resistance[e]	R_{ON}	V+ = 4.5 V, I_{NO}, I_{NC} = 5 mA V_{COM} = 1 V, 3.5 V	Room Full	26		36.5 50		36.5 40.5	Ω
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 3.5 V, see figure 2	Room Full	37		49 60		49 54	ns
Turn-Off Time[e]	t_{OFF}		Room Full	16		31 35		31 32	
Break-Before-Make Time Delay[e]	t_D	DG419L only, V_{NO}, V_{NC} = 3.5 V R_L = 300 Ω, C_L = 35 pF	Room	19					
Charge Injection[e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	0.4					pC
Power Supplies									
Positive Supply Current[e]	I+	V_{IN} = 0 or V_L	Room Full	0.02		1 7.5		1 5	µA
Negative Supply Current[e]	I-		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		
Logic Supply Current[e]	I_L		Room Full	0.002		1 7.5		1 5	
Ground Current[e]	I_{GND}		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		

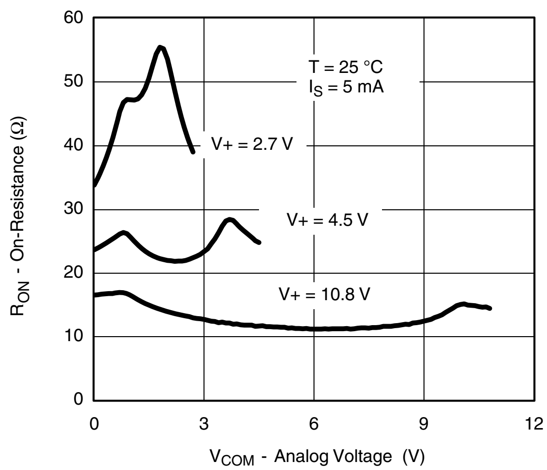
SPECIFICATIONS (Single Supply 3 V)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3 V, V- = 0 V V_L = 3 V, V_{IN} = 2 V, 0.4 V[f]	Temp.[b]	Typ.[c]	A Suffix Limits - 55 °C to 125 °C Min.[d]	A Suffix Limits Max.[d]	D Suffix Limits - 40 °C to 85 °C Min.[d]	D Suffix Limits Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	3	0	3	V
On-Resistance	R_{ON}	V+ = 2.7 V, V- = 0 V I_{NO}, I_{NC} = 5 mA, V_{COM} = 0.5 V, 2.2 V	Room Full	47		70 80		70 75	Ω
Switch Off Leakage Current[a]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 , V- = 0 V V_{COM} = 1, 2 V, V_{NO}, V_{NC} = 2, 1 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	$I_{COM(off)}$		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current[a]	$I_{COM(on)}$	V+ = 3.3 V, V- = 0 V V_{NO}, V_{NC} = V_{COM} = 1 V, 2 V	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Input Current[a]	I_{INL} or I_{INH}		Full	0.005	- 1.5	1.5	- 1	1	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 1.5 V, see figure 2	Room Full	65		75 95		75 85	ns
Turn-Off Time	t_{OFF}		Room Full	26		41 45		41 43	
Break-Before-Make Time Delay	t_D	DG419L only, V_{NO}, V_{NC} = 1.5 V R_L = 300 Ω, C_L = 35 pF	Room	33					
Charge Injection[e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	1					pC
Off-Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF , f = 1 MHz	Room	- 71					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	- 77					
Source Off Capacitance[e]	$C_{NO(off)}$ $C_{NC(off)}$	f = 1 MHz	Room	5.6					pF
Channel On Capacitance[e]	$C_{D(on)}$		Room	16					

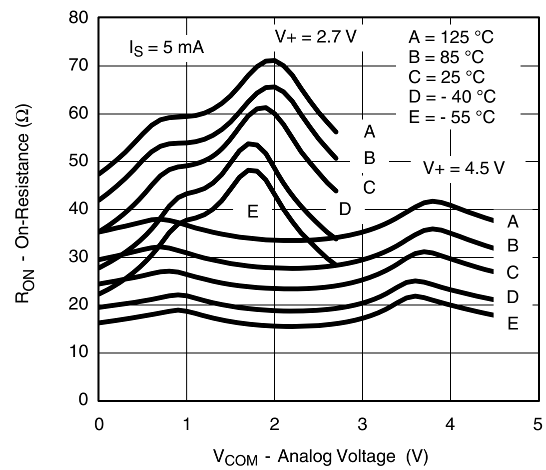
Notes:
a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

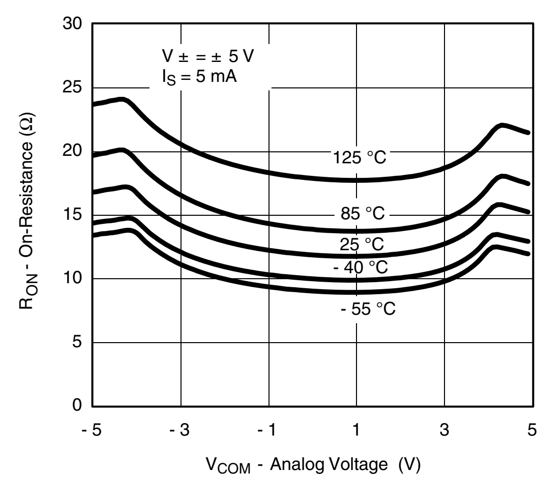
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



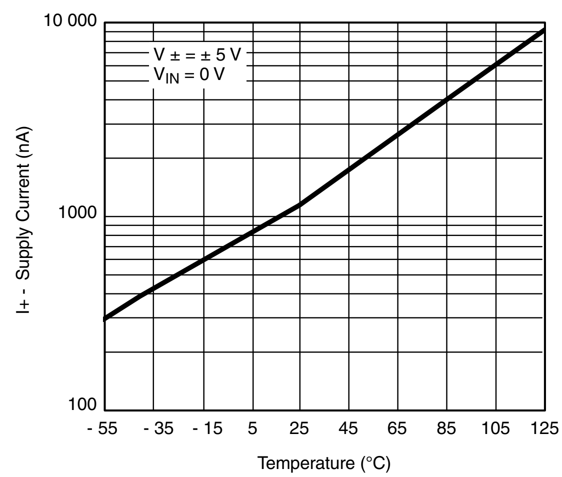
R_{ON} vs. V_{COM} and Supply Voltage



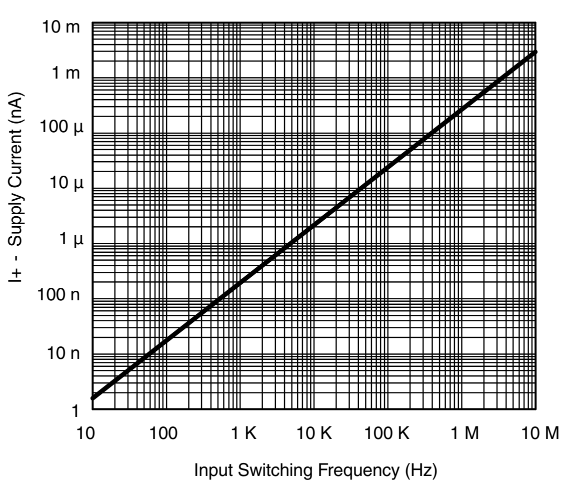
R_{ON} vs. Analog Voltage and Temperature



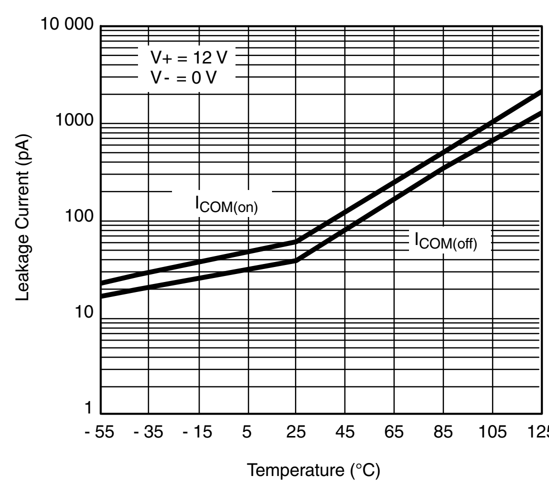
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

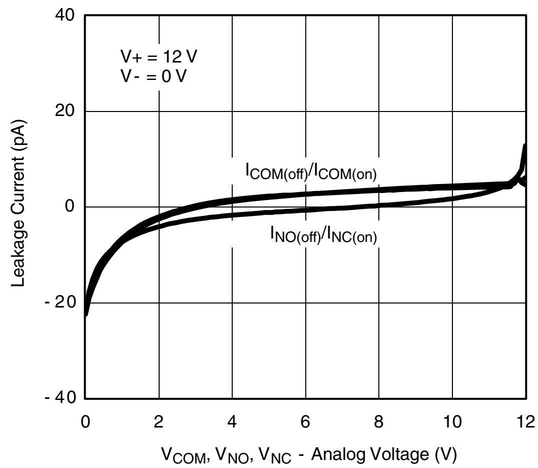


Supply Current vs. Input Switching Frequency

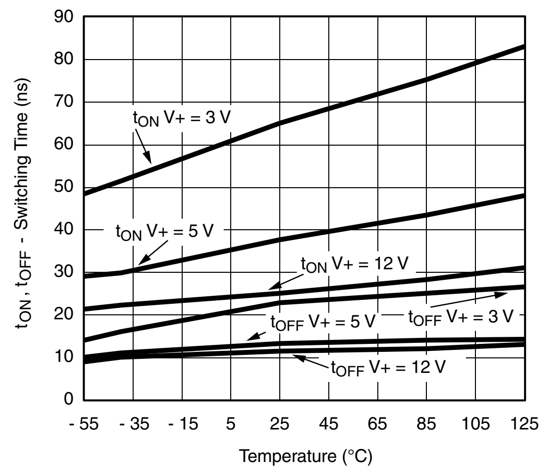


Leakage Current vs. Temperature

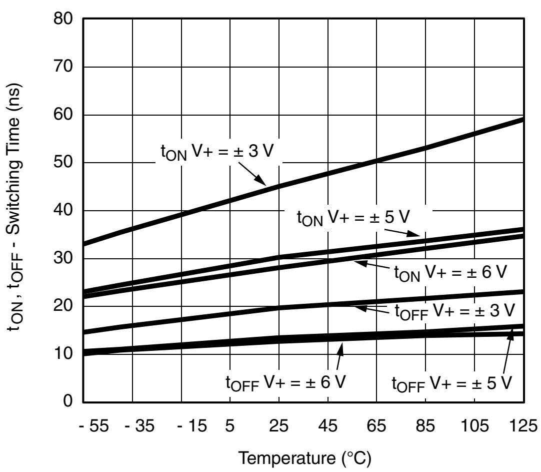
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



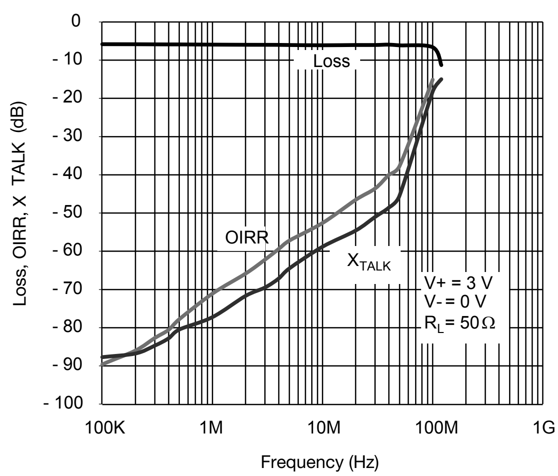
Leakage vs. Analog Voltage



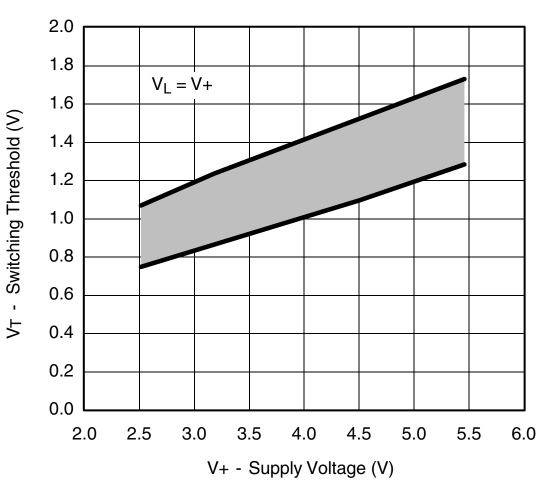
Switching Time vs. Temperature and Single Supply Voltage



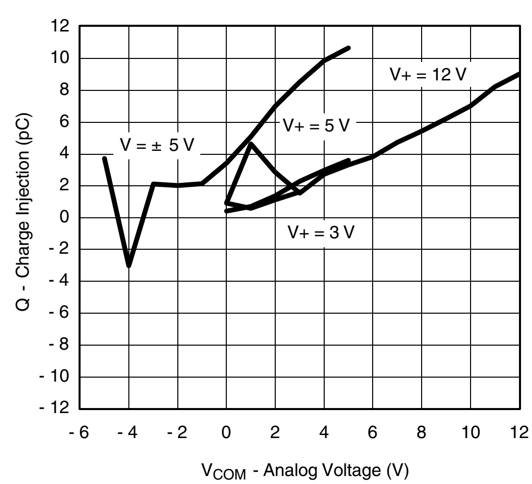
Switching Time vs. Temperature and Dual Supply Voltage



Insertion Loss, Off -Isolation Crosstalk vs. Frequency



Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage)

SCHEMATIC DIAGRAM (Typical Channel)

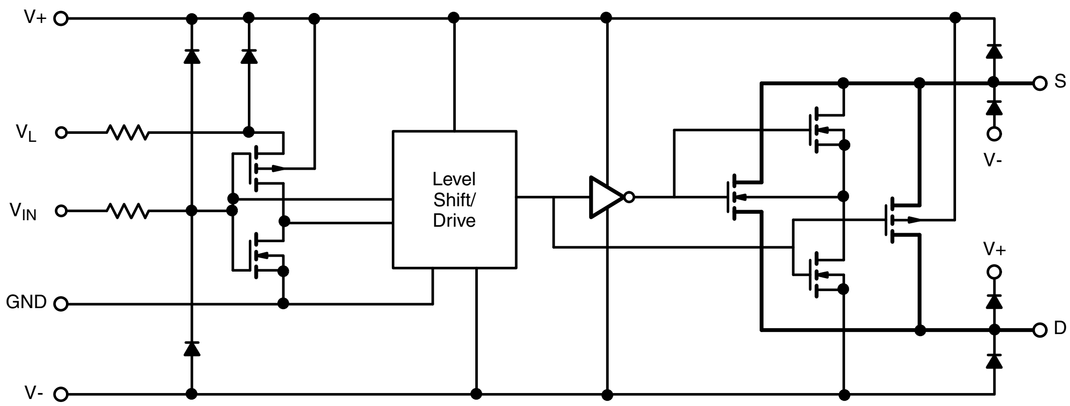
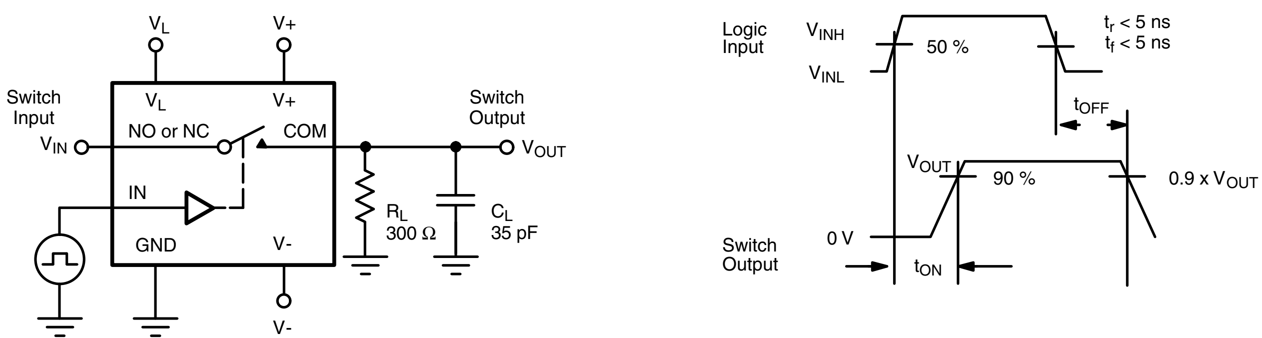


Figure 1.

TEST CIRCUITS

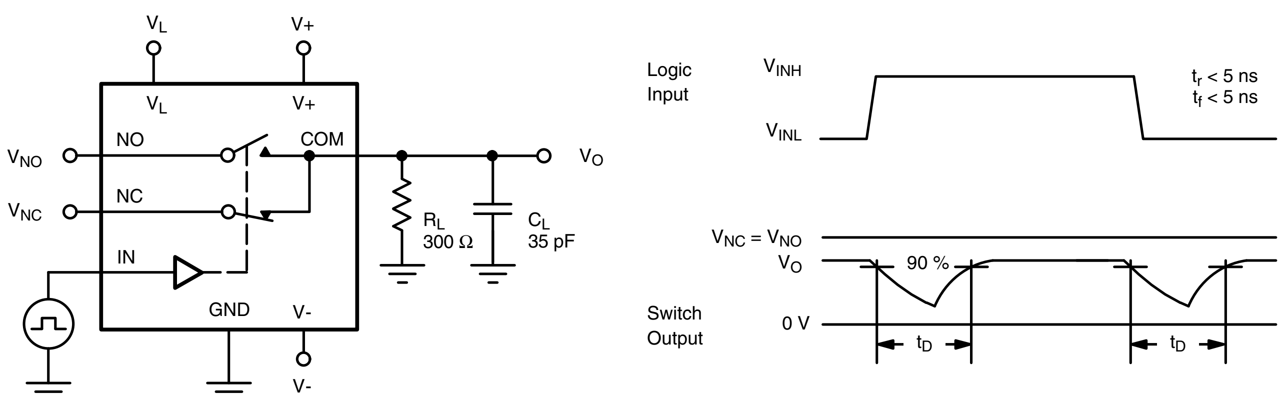


C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

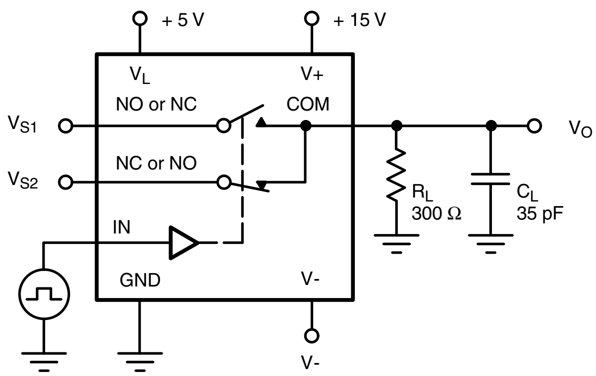
Figure 2. Switching Time

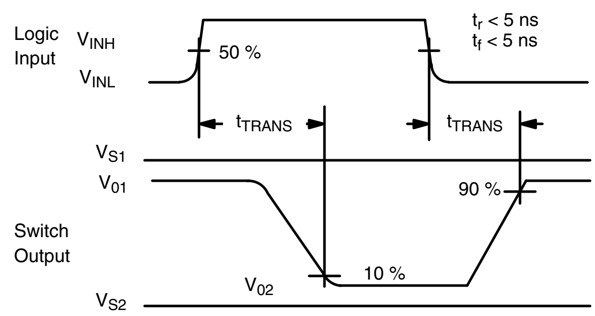


C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make (DG419L)

TEST CIRCUITS

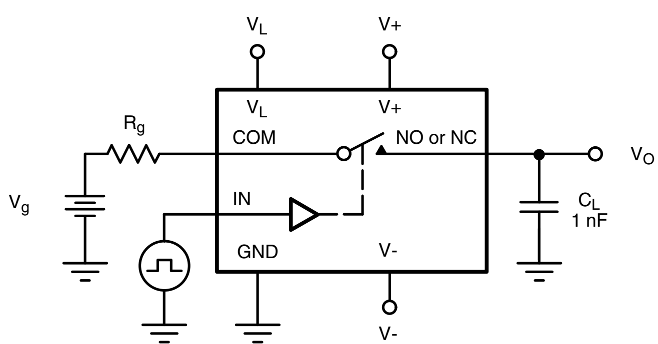




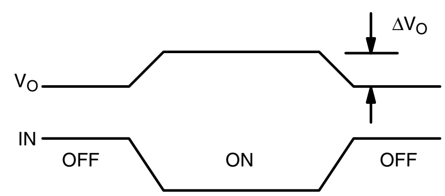
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + R_{ON}}$$

Figure 4. Transition Time (DG419L)



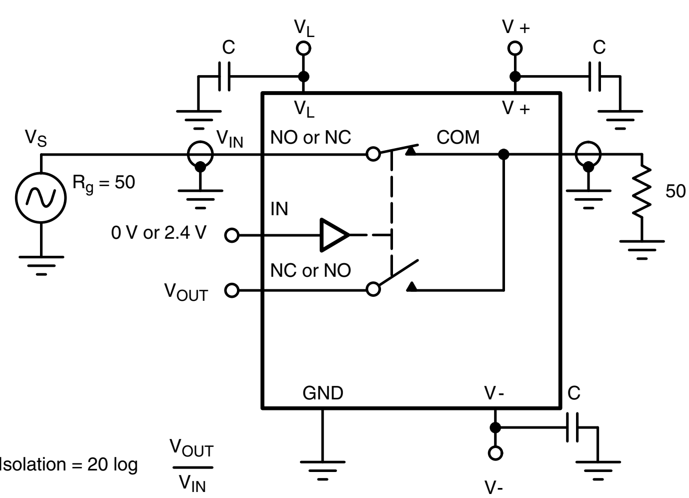
$V_{IN} = 0 - V+$



$Q = \Delta V_O \times C_L$

IN dependent on switch configuration Input polarity determined by sense of switch.

Figure 5. Charge Injection



$$X_{TALK} \text{ Isolation} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

C = RF bypass

Figure 6. Crosstalk (DG419L)

TEST CIRCUITS

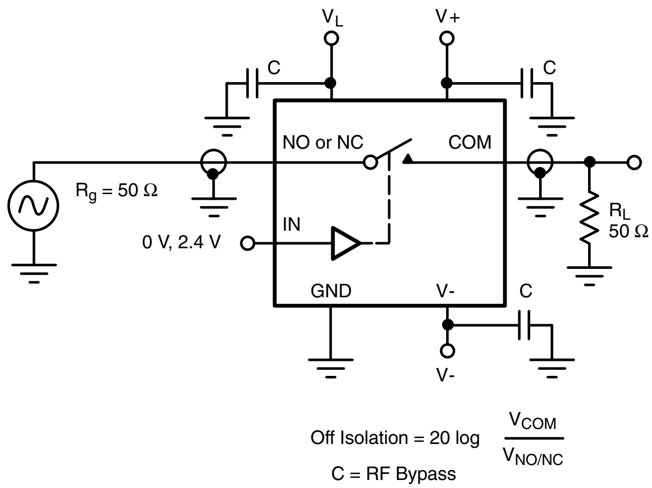


Figure 7. Off Isolation

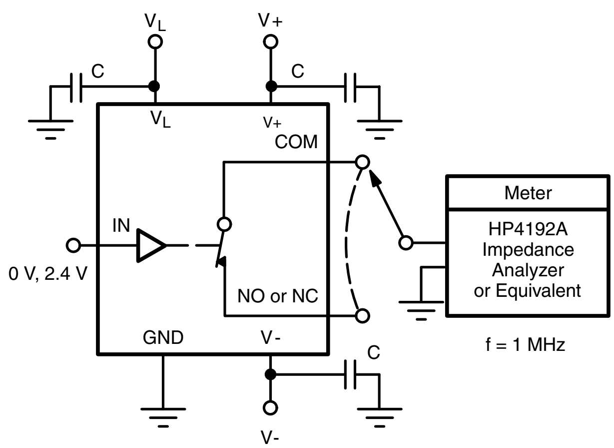
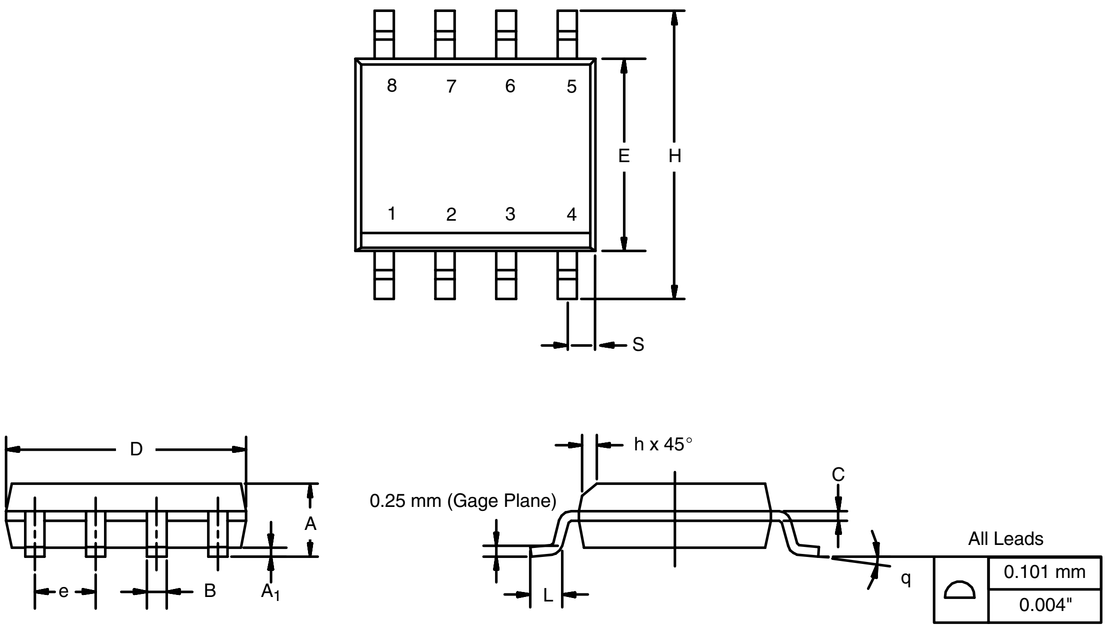


Figure 8. Source/Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71763.

SOIC (NARROW): 8-LEAD

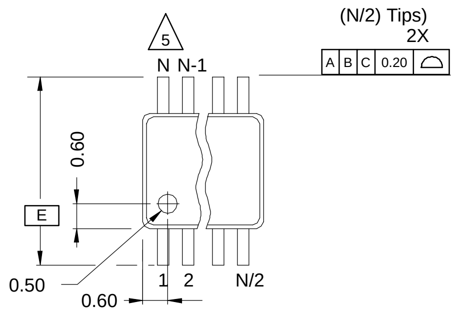
JEDEC Part Number: MS-012



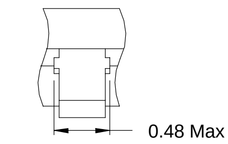
DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

MSOP: 8-LEADS

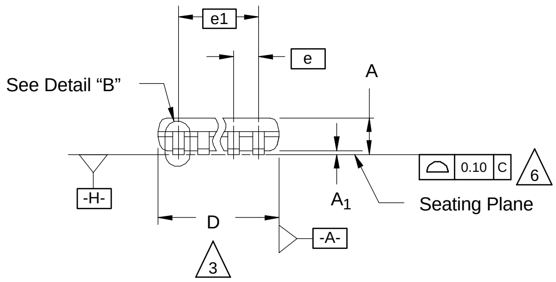
JEDEC Part Number: MO-187, (Variation AA and BA)



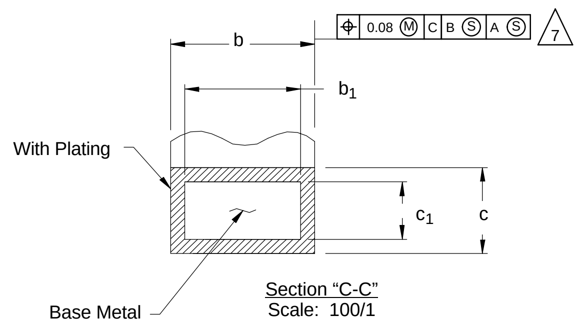
Top View



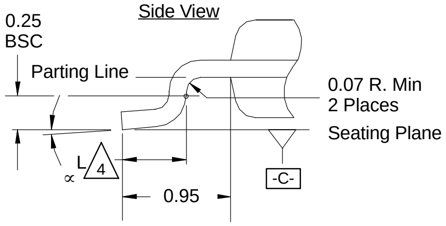
Detail "B"
(Scale: 30/1)
Dambar Protrusion



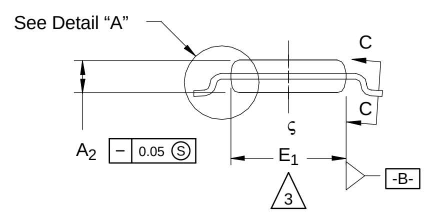
Side View



Section "C-C"
Scale: 100/1
(See Note 8)



Detail "A"
(Scale: 30/1)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 8L

	MILLIMETERS			
Dim	Min	Nom	Max	Note
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.25	-	0.38	8
b_1	0.25	0.30	0.33	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.65 BSC			
e_1	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
∝	0°	4°	6°	
ECN: T-02080—Rev. C, 15-Jul-02 DWG: 5867				

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs,* (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

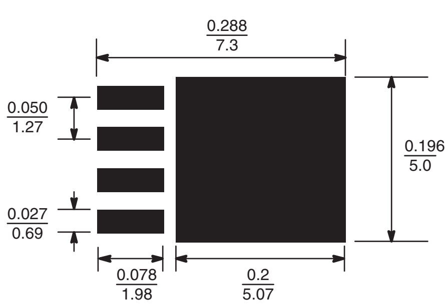


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

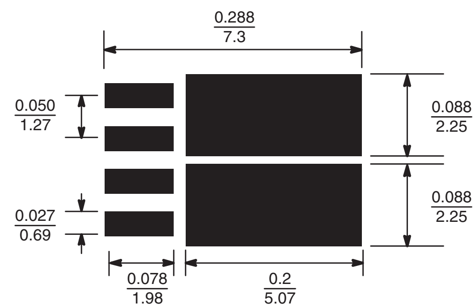


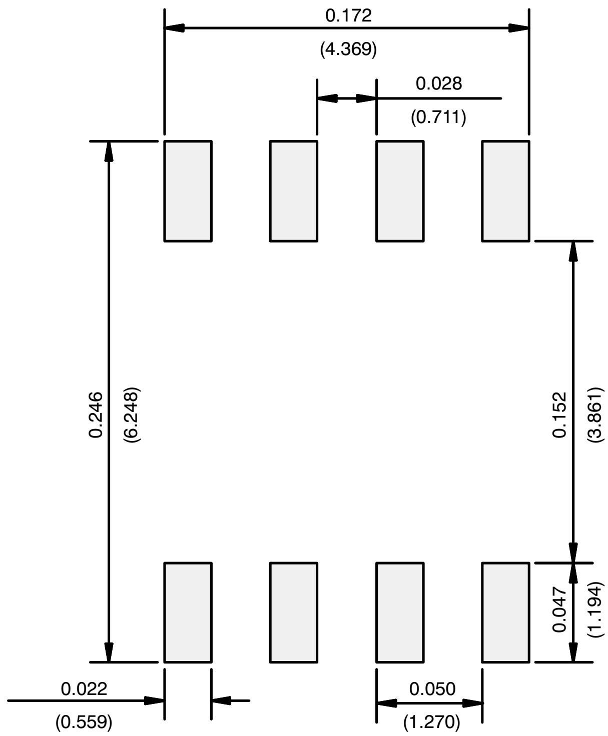
Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.