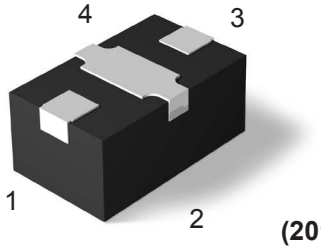
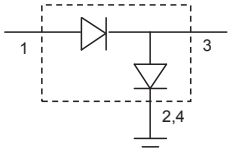
MSWSS-020-40

PIN Diode Series Shunt Integrated Switch Element





(2012)
Laser mark is input

Description

A broadband, high linearity, medium power series shunt integrated switch element in a 1.9 X 1.1 mm QFN package. This device is designed for WiMax, Wibro, WLAN, TD-SCDMA and other wireless infrastructure applications. It is also suited for 0.1 ~ 6 GHz applications with up to 20 watts of power.

Features

- Supports up to 20 watts power when cold switched
- Low insertion loss 0.3 dB typical up to 2.7 GHz
- High Isolation 50 dB typical up to 2.7 GHz

Electrical Specifications, T_A = +25 °C

SYMBOL	TEST CONDITIONS		MIN	TYPICAL	MAX	UNITS
C_J	Series		–	0.05	–	pF
	Shunt		–	0.14	–	pF
V_{BR}	I_R = 10 µA		100	–	–	V
R_s	Series		–	0.98	–	Ω
	Shunt		–	0.50	–	Ω
τ	I_R = 10 mA, I_F = 10 mA measured at 50%		–	450	–	ns
			–	500	–	ns
W	Series		–	15	–	µm
	Shunt		–	15	–	µm
IL	I = -50 mA*	F = 2.3 ~ 2.7 GHz	–	0.3	0.5	dB
		F = 6.0 GHz	–	0.6	0.8	dB
IRL	I = -50 mA*	F = 2.3 ~ 2.7 GHz	15	21	–	dB
		F = 6.0 GHz	10	13	–	dB
ORL	I = -50 mA*	F = 2.3 ~ 2.7 GHz	15	22	–	dB
		F = 6.0 GHz	10	13	–	dB
Iso	I = +50 mA*	F = 2.3 ~ 2.7 GHz	40	50	–	dB
		F = 6.0 GHz	30	35	–	dB

* Positive current is defined as current going into pin 3.

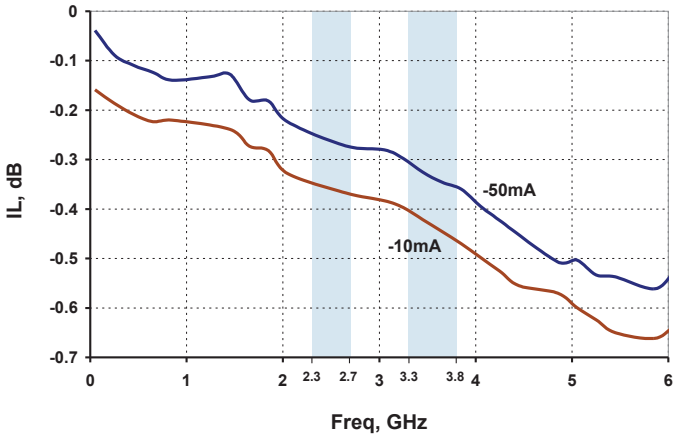
Absolute Maximum Ratings

RATING	LIMITS	UNITS
V_R	100	V
I_F	100	mA
θ_{JC}	30	°C/W
T_J	+175	°C
T_{STG}	-65 to +150	°C
T_{SOLDER}	+260 °C per JEDEC J-STD-20C	

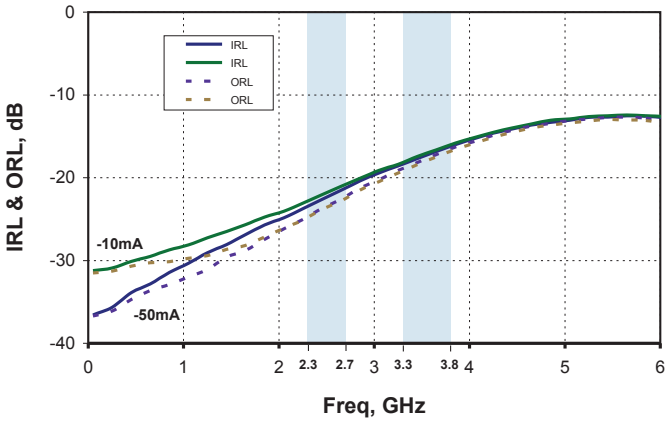
AEROFLEX METELICS

Typical RF Performance at T_A = 25 °C, Zo = 50 Ω, Small Signal
(Unless Otherwise Specified)

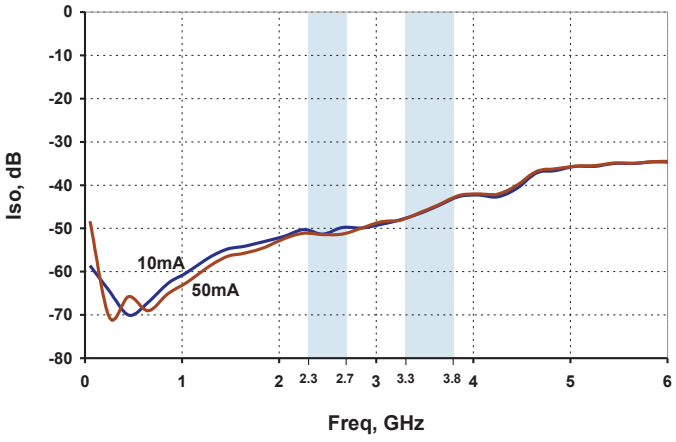
Insertion Loss



Input and Output Return Loss



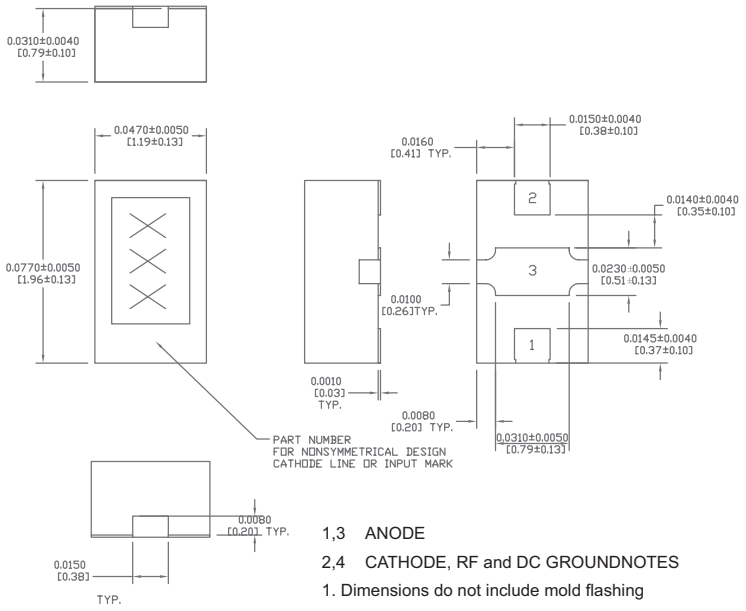
Isolation



Bias Schematic (0.1 to 6 GHz)

NOTE: Contact factory for faster driver circuit!

Package Outline (2012)



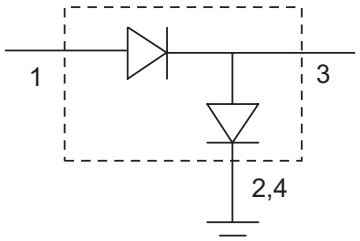
1,3 ANODE

2,4 CATHODE, RF and DC GROUNDNOTES

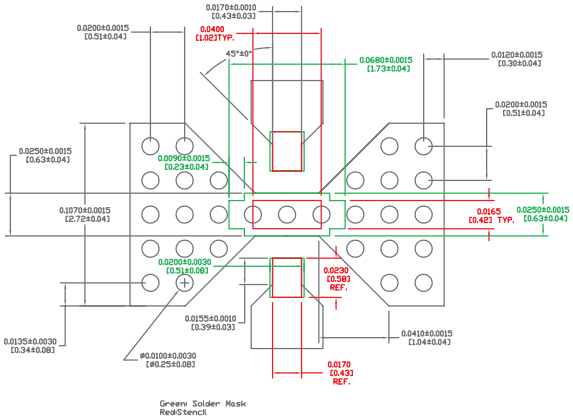
1. Dimensions do not include mold flashing
2. Burrs and dumbar shall not exceed 0.002" per surface.
3. Lead co-planarity is 0.003" max

Dimensions: inches [mm]

Electrical Schematic



PCB Layout



NOTE: If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

Solder mask should provide a 60 um clearance between copper pad and soldermask. Rounded pkg pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that only get 50% to 80% solder paste coverage.

Aeroflex / Metelics Inc.
Aeroflex Microelectronic Solutions
975 Stewart Drive
Sunnyvale, CA 94085
TEL: 408-737-8181

54 Grenier Field Road
Londonderry, NH 03053
TEL: 603-641-3800

Sales
888-641-SEMI (7364)
metelics-sales@aeroflex.com

www.aeroflex.com/Microwave www.aeroflex.com/Metelics

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