

# 74HC423; 74HCT423

Dual retriggerable monostable multivibrator with reset

Rev. 6 — 19 December 2011

Product data sheet

## 1. General description

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74HC423; 74HCT423 are high-speed Si-gate CMOS devices that are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC423; 74HCT423 dual retriggerable monostable multivibrator with reset has two methods of output pulse width control.

1. The minimum pulse width is essentially determined by the selection of an external resistor ( $R_{EXT}$ ) and capacitor ( $C_{EXT}$ ), see [Section 12.1](#).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ( $n\bar{A}$ ) or the active HIGH-going edge input ( $nB$ ). By repeating this process, the output pulse period ( $nQ = \text{HIGH}$ ,  $n\bar{Q} = \text{LOW}$ ) can be made as long as desired. When  $n\bar{RD}$  is LOW, it forces the  $nQ$  output LOW, the  $n\bar{Q}$  output HIGH and also inhibits the triggering. [Figure 10](#) and [Figure 11](#) illustrate pulse control by reset.

The  $n\bar{A}$  and  $nB$  inputs' Schmitt trigger action makes them highly tolerant to slower input rise and fall times.

The 74HC423; 74HCT423 are identical to the 74HC123; 74HCT123 except that they cannot be triggered via the reset input.

## 2. Features and benefits

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- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$



### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC423N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT423N				
74HC423D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT423D				
74HC423BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT423BQ				
74HCT423DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT423PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 4. Functional diagram

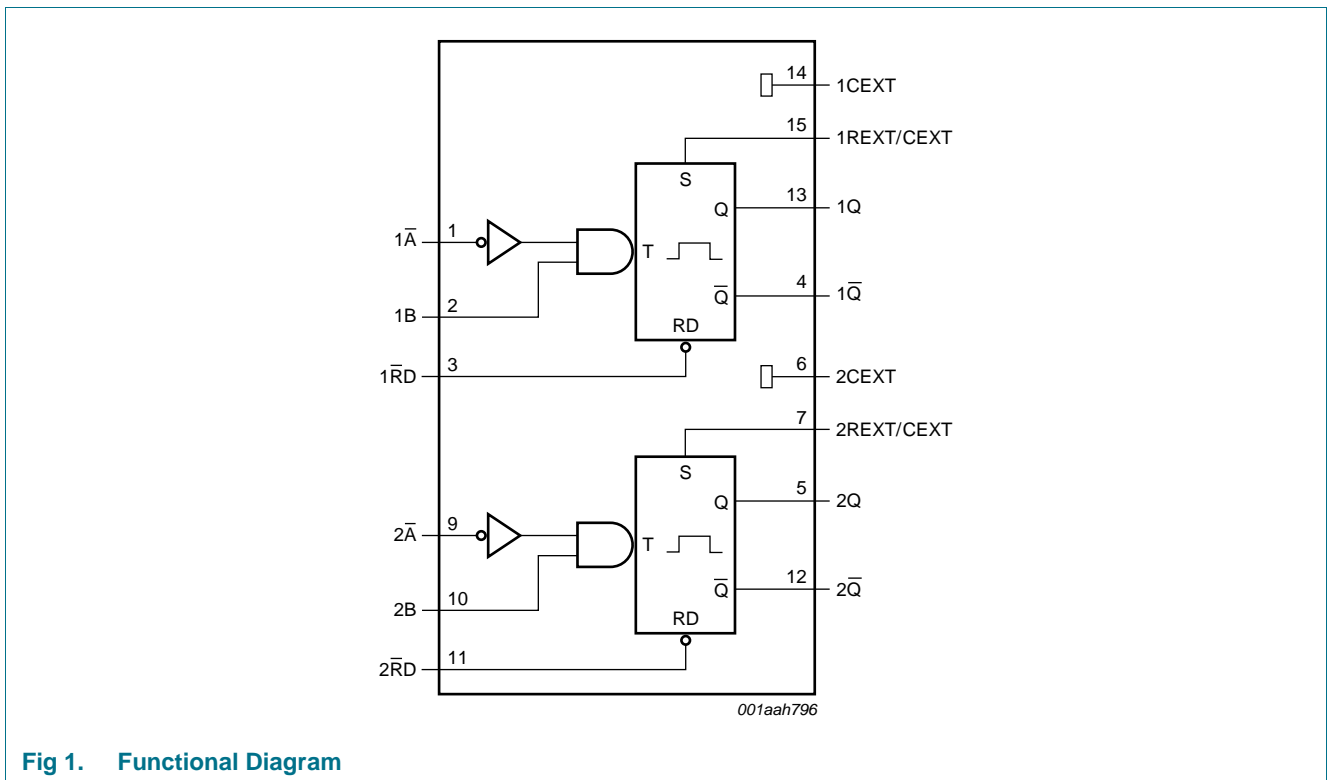


Fig 1. Functional Diagram

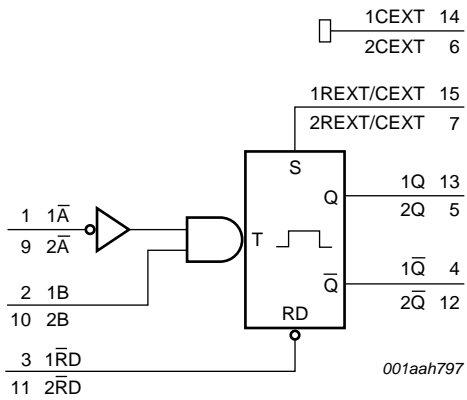


Fig 2. Logic symbol

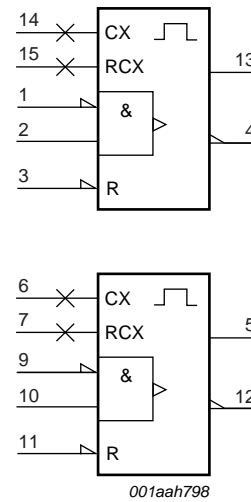


Fig 3. IEC Logic symbol

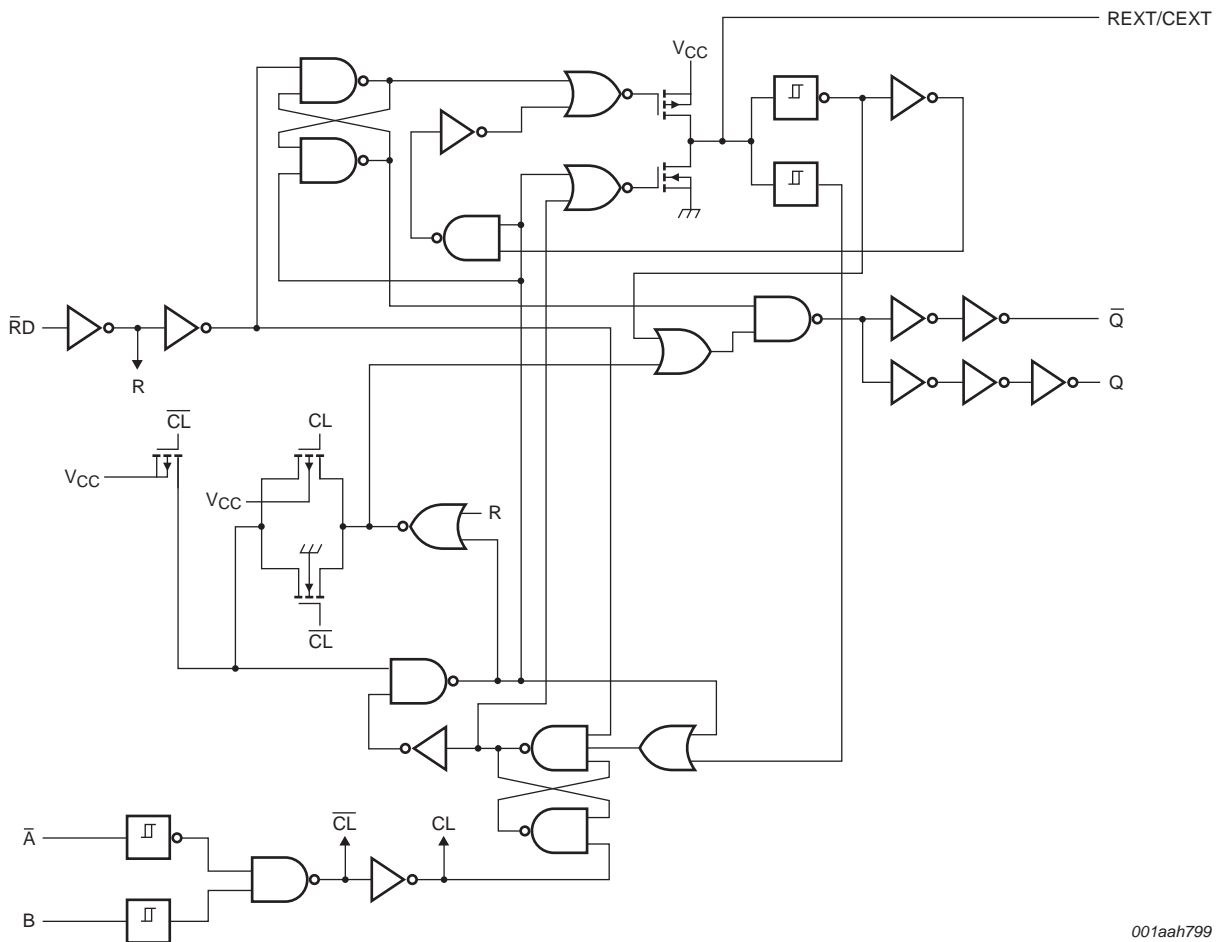
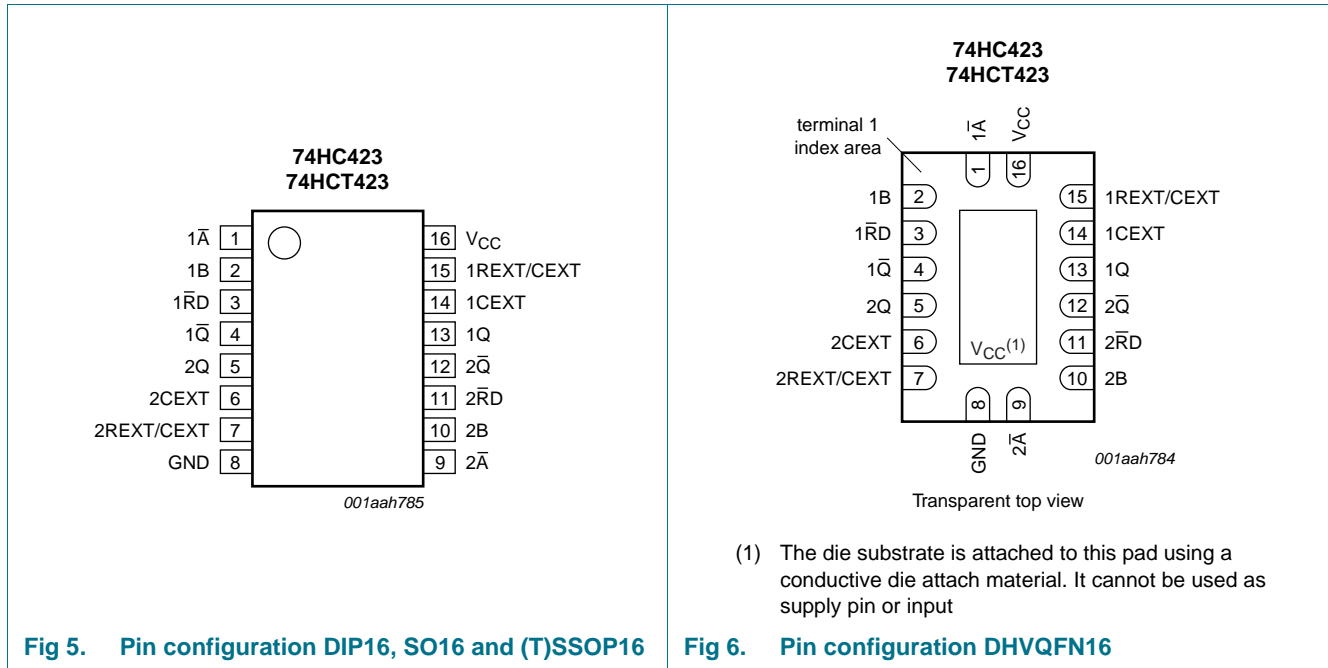


Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning







### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1 $\bar{A}$ , 2 $\bar{A}$	1, 9	trigger input (negative edge triggered)
1B, 2B	2, 10	trigger input (positive edge triggered)
1 $\bar{R}D$ , 2 $\bar{R}D$	3, 11	direct reset (active LOW)
1 $\bar{Q}$ , 2 $\bar{Q}$	4, 12	output (active LOW)
GND	8	ground (0 V)
1Q, 2Q	13, 5	output (active HIGH)
1CEXT, 2CEXT	14, 6	external capacitor connection
1REXT/CEXT, 2REXT/CEXT	15, 7	external resistor/capacitor connection
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input			Output	
nRD	nA	nB	nQ	nQ
L	X	X	L	H
X	H	X	L <sup>[2]</sup>	H <sup>[2]</sup>
X	X	L	L <sup>[2]</sup>	H <sup>[2]</sup>
H	L	↑		
H	↓	H		

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 ↑ = LOW-to-HIGH transition;  
 ↓ = HIGH-to-LOW transition;

 = one HIGH level output pulse;

 = one LOW level output pulse.

- [2] If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	<sup>[1]</sup> -	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	<sup>[1]</sup> -	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	DIP16 package	<sup>[2]</sup> -	750	mW
		SO16, SSOP16, TSSOP16 and DHVQFN16 packages	<sup>[3]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] For DIP16 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 12 mW/K.

- [3] For SO16 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 8 mW/K;  
 For SSOP16 and TSSOP16 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K;  
 For DHVQFN16 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC423			74HCT423			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC423</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT423</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}; V_{CC} = 4.5\text{ V}$								
		$I_O = -20\ \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}; V_{CC} = 4.5\text{ V}$								
		$I_O = 20\ \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$	-	0.15	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}$	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}; I_O = 0\text{ A}$	-	-	8.0	-	80	-	160	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V};$ other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}; I_O = 0\text{ A}$								
		nA, nB inputs	-	35	126	-	158	-	172	$\mu\text{A}$
		nRD input	-	50	180	-	225	-	245	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND = 0 V; test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC423</b>										
t <sub>pd</sub>	propagation delay	n $\bar{A}$ or nB to nQ or n $\bar{Q}$ ; R <sub>EXT</sub> = 5 k $\Omega$ ; C <sub>EXT</sub> = 0 pF; see <a href="#">Figure 7</a>	[1]							
		V <sub>CC</sub> = 2.0 V	-	80	255	-	320	-	385	ns
		V <sub>CC</sub> = 4.5 V	-	29	51	-	64	-	77	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	25	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	23	43	-	54	-	65	ns
		n $\bar{RD}$ to nQ or n $\bar{Q}$ ; see <a href="#">Figure 7</a>	[1]							
		V <sub>CC</sub> = 2.0 V	-	66	215	-	270	-	325	ns
		V <sub>CC</sub> = 4.5 V	-	24	43	-	54	-	65	ns
t <sub>t</sub>	transition time	see <a href="#">Figure 7</a>	[2]							
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
t <sub>w</sub>	pulse width	V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
		n $\bar{A}$ input LOW; see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 2.0 V	100	11	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	4	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	3	-	21	-	26	-	ns
		nB input HIGH; see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 2.0 V	100	17	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	6	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	5	-	21	-	26	-	ns
		n $\bar{RD}$ input LOW; see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 2.0 V	100	14	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	5	-	25	-	30	-	ns
V <sub>CC</sub> = 6.0 V	17	4	-	21	-	26	-	ns		
t <sub>trig</sub>	retrigger time	nQ HIGH or n $\bar{Q}$ LOW; V <sub>CC</sub> = 5.0 V; R <sub>EXT</sub> = 10 k $\Omega$ ; C <sub>EXT</sub> = 100 nF; see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>			450	-	-	-	-	$\mu$ s
		nQ HIGH or n $\bar{Q}$ LOW; V <sub>CC</sub> = 5.0 V; R <sub>EXT</sub> = 5 k $\Omega$ ; C <sub>EXT</sub> = 0 pF; V <sub>I</sub> = GND to V <sub>CC</sub> ; see <a href="#">Figure 7</a> and <a href="#">Figure 8</a>	[3]							
		-	-	75	-	-	-	-	-	ns
		n $\bar{A}$ or nB input; V <sub>CC</sub> = 5.0 V; R <sub>EXT</sub> = 5 k $\Omega$ ; C <sub>EXT</sub> = 0 pF; see <a href="#">Figure 10</a>	[4]							
		-	-	110	-	-	-	-	-	ns



**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V; test circuit see [Figure 12](#).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
R <sub>EXT</sub>	external timing resistor	V <sub>CC</sub> = 2.0 V; see <a href="#">Figure 8</a>	10	-	1000	-	-	-	-	kΩ
		V <sub>CC</sub> = 5.0 V	2	-	1000	-	-	-	-	kΩ
C <sub>EXT</sub>	external timing capacitor	V <sub>CC</sub> = 5.0 V; see <a href="#">Figure 8</a>	no limits						pF	
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub>	-	54	-	-	-	-	-	pF

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t <sub>pd</sub>	propagation delay	n $\bar{A}$ or nB to nQ or n $\bar{Q}$ ; R <sub>EXT</sub> = 5 kΩ; C <sub>EXT</sub> = 0 pF; see <a href="#">Figure 7</a>									
		V <sub>CC</sub> = 4.5 V	[1]	-	30	51	-	64	-	77	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	[1]	-	26	-	-	-	-	-	ns
		n $\bar{RD}$ to nQ or n $\bar{Q}$ ; R <sub>EXT</sub> = 5 kΩ; C <sub>EXT</sub> = 0 pF; see <a href="#">Figure 7</a>	[1]	-	26	48	-	60	-	72	ns
		V <sub>CC</sub> = 4.5 V	[1]	-	26	48	-	60	-	72	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	[1]	-	22	-	-	-	-	ns	
t <sub>t</sub>	transition time	V <sub>CC</sub> = 4.5 V; <a href="#">Figure 7</a>	[2]	-	7	15	-	19	-	22	ns
t <sub>w</sub>	pulse width	trigger pulse; n $\bar{A}$ input LOW; V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a>	20	5	-	25	-	30	-	ns	
		trigger pulse; nB input HIGH; V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 7</a> and <a href="#">Figure 10</a>	20	5	-	25	-	30	-	ns	
		reset pulse; n $\bar{RD}$ input LOW; V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 7</a> and <a href="#">Figure 11</a>	20	7	-	25	-	30	-	ns	
		output pulse; nQ HIGH or n $\bar{Q}$ LOW; V <sub>CC</sub> = 5.0 V; R <sub>EXT</sub> = 10 kΩ; C <sub>EXT</sub> = 100 nF; see <a href="#">Figure 7</a> , <a href="#">Figure 10</a> and <a href="#">Figure 11</a>	-	450	-	-	-	-	-	-	μs
		output pulse; nQ HIGH or n $\bar{Q}$ LOW; V <sub>CC</sub> = 5.0 V; R <sub>EXT</sub> = 5 kΩ; C <sub>EXT</sub> = 0 pF; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V; see <a href="#">Figure 7</a> , <a href="#">Figure 10</a> and <a href="#">Figure 11</a>	[3]	-	75	-	-	-	-	-	ns
t <sub>rtrig</sub>	retrigger time	n $\bar{A}$ or nB input; V <sub>CC</sub> = 5.0 V; R <sub>EXT</sub> = 5 kΩ; C <sub>EXT</sub> = 0 pF; see <a href="#">Figure 10</a>	-	110	-	-	-	-	-	ns	
R <sub>EXT</sub>	external timing resistor	V <sub>CC</sub> = 5.0 V; see <a href="#">Figure 8</a>	2	-	1000	-	-	-	-	kΩ	
C <sub>EXT</sub>	external timing capacitor	V <sub>CC</sub> = 5.0 V; see <a href="#">Figure 8</a>	no limits						pF		

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V; test circuit see [Figure 12](#).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V <a href="#">[6]</a>	-	56	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.

[2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

[3] For other R<sub>EXT</sub> and C<sub>EXT</sub> combinations see [Figure 8](#). If C<sub>EXT</sub> > 10 pF, the next formula is valid:

t<sub>W</sub> = K × R<sub>EXT</sub> × C<sub>EXT</sub> (typ.), where:

t<sub>W</sub> = output pulse width in ns;

R<sub>EXT</sub> = external resistor in kΩ;

C<sub>EXT</sub> = external capacitor in pF;

K = 0.55 for V<sub>CC</sub> = 2.0 V and 0.45 for V<sub>CC</sub> = 5.0 V; see [Figure 9](#).

Inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[4] The time to retrigger the monostable multivibrator depends on the values of R<sub>EXT</sub> and C<sub>EXT</sub>. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

If C<sub>EXT</sub> > 10 pF, the next formula (at V<sub>CC</sub> = 5.0 V) for the set-up time of a retrigger pulse is valid:

t<sub>trig</sub> = 30 + 0.19 × R<sub>EXT</sub> × C<sub>EXT</sub><sup>0.9</sup> + 13 × R<sub>EXT</sub><sup>1.05</sup> (typ.); where:

t<sub>trig</sub> = retrigger time in ns;

C<sub>EXT</sub> = external capacitor in pF;

R<sub>EXT</sub> = external resistor in kΩ.

Inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[5] When the device is powered-up, initiate the device via a reset pulse, when C<sub>EXT</sub> < 50 pF.

[6] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>); where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

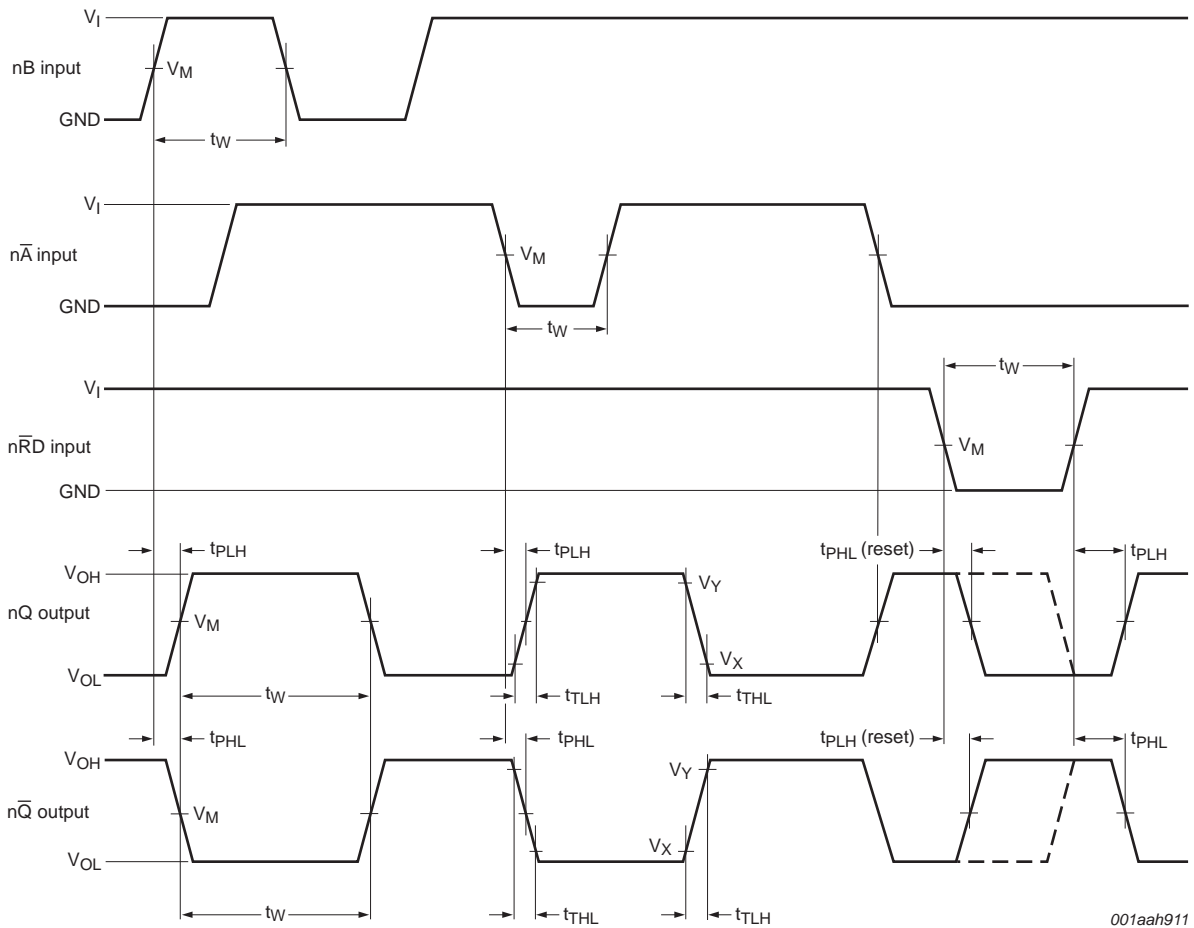
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

11. Waveforms



001aah911

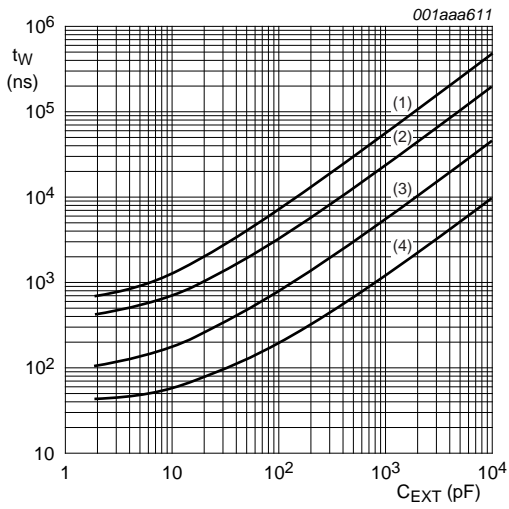
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Pulse widths, propagation delays from inputs (nA, nB, nRD) to outputs (nQ, nQ) and output transition times**

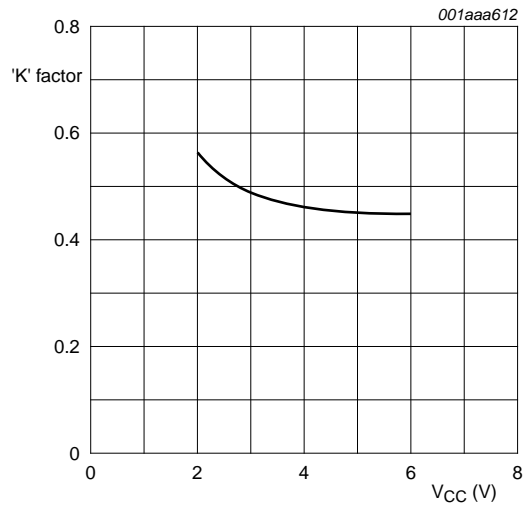
**Table 8. Measurement points**

Type	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
74HC423	$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT423	3 V	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



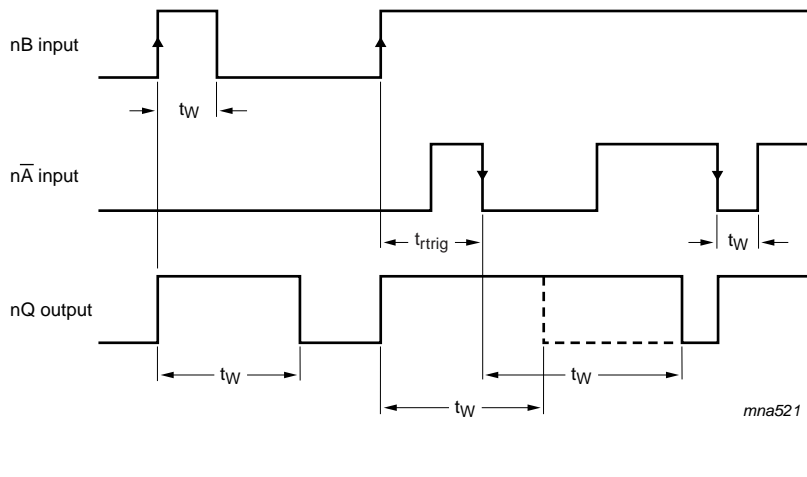
$V_{CC} = 5.0\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .  
 (1)  $R_{EXT} = 100\text{ k}\Omega$ .  
 (2)  $R_{EXT} = 50\text{ k}\Omega$ .  
 (3)  $R_{EXT} = 10\text{ k}\Omega$ .  
 (4)  $R_{EXT} = 2\text{ k}\Omega$ .

**Fig 8. Typical output pulse width as a function of the external capacitor values**



External capacitance = 10 nF,  
 external resistance = 10 kΩ to 100 kΩ and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

**Fig 9. Typical 'K' factor**



**Fig 10. Output pulse control using retrigger pulse ( $t_{rtrig}$ )**

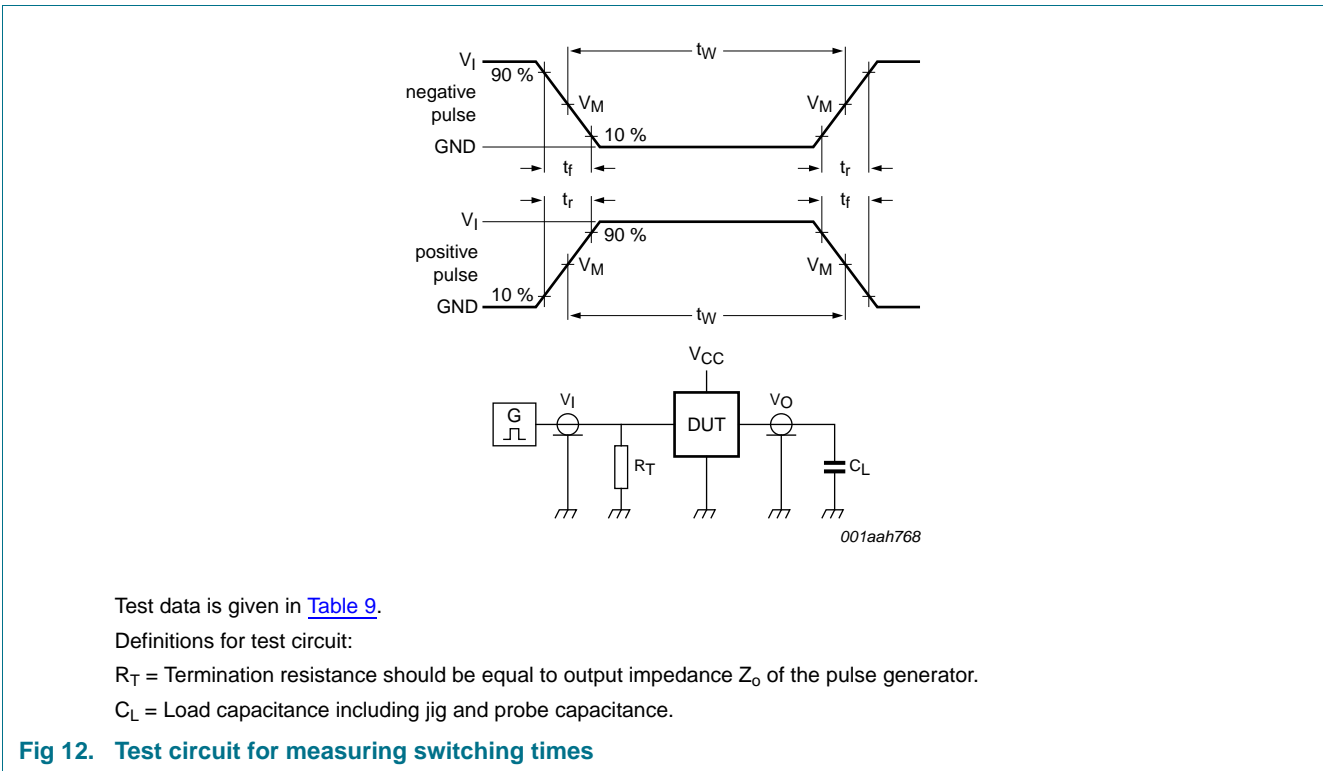
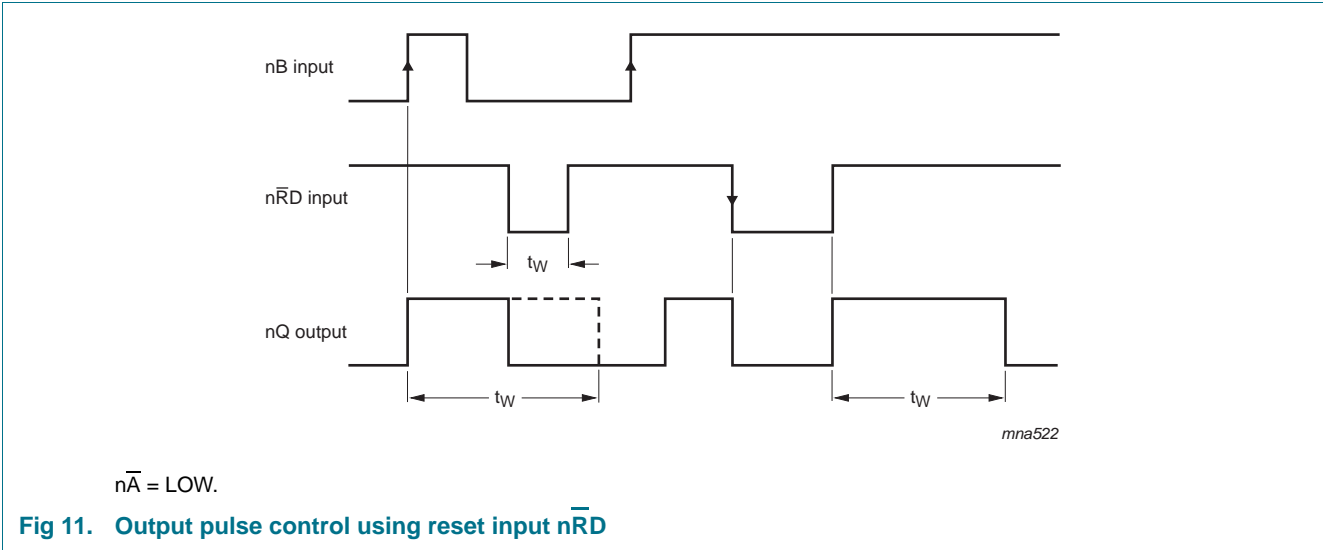


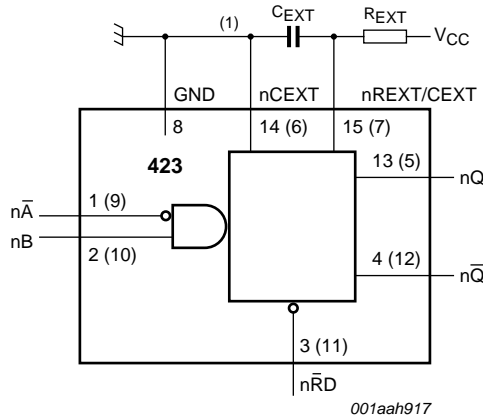
Table 9. Test data

Supply	Input	Load
$V_{CC}$	$V_I$	$C_L$
2.0 V to 6.0 V	$V_{CC}$	15 pF, 50 pF
		$t_r, t_f$
		6 ns

## 12. Application information

### 12.1 Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components  $R_{EXT}$  and  $C_{EXT}$ .



- (1) For minimum noise generation it is recommended that the nCEXT pins (6, 14) are connected to ground externally to the GND pin (8).

Fig 13. Timing component connections

#### 12.1.1 Minimum monostable pulse width

To set the minimum pulse width, when  $C_{EXT} < 10$  nF, see [Figure 8](#) and when  $C_{EXT} > 10$  nF, the output pulse width is defined as:

$$t_W = 0.45 \times R_{EXT} \times C_{EXT} \text{ (typ.)}, \text{ where:}$$

$t_W$  = pulse width in  $\mu\text{s}$ ;

$R_{EXT}$  = external resistor in  $\text{k}\Omega$ ;

$C_{EXT}$  = external capacitor in nF.

#### 12.2 Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of  $R_{EXT}$  and  $C_{EXT}$ , this output pulse can be eliminated using the circuit shown in [Figure 14](#).

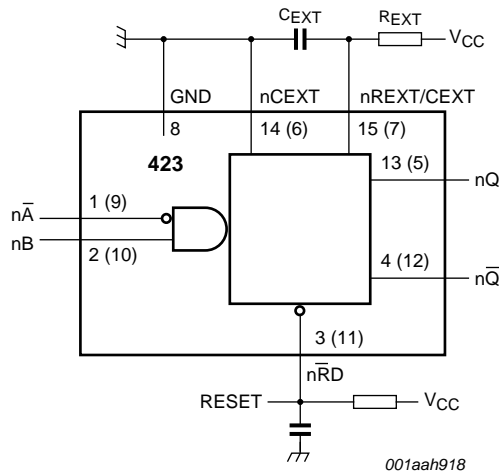


Fig 14. Power-up output pulse elimination circuit

### 12.3 Power-down considerations

A large capacitor  $C_{EXT}$  may cause problems when powering-down the monostable due to the capacitor's stored energy. When a system containing this device is powered-down or a rapid decrease of  $V_{CC}$  to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode  $D_{EXT}$  preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Figure 15](#).

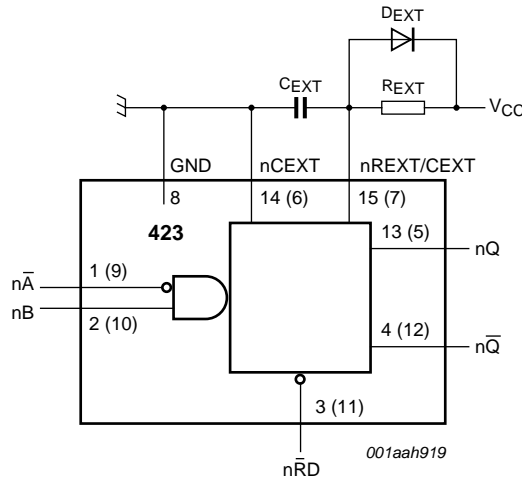


Fig 15. Power-down protection circuit

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

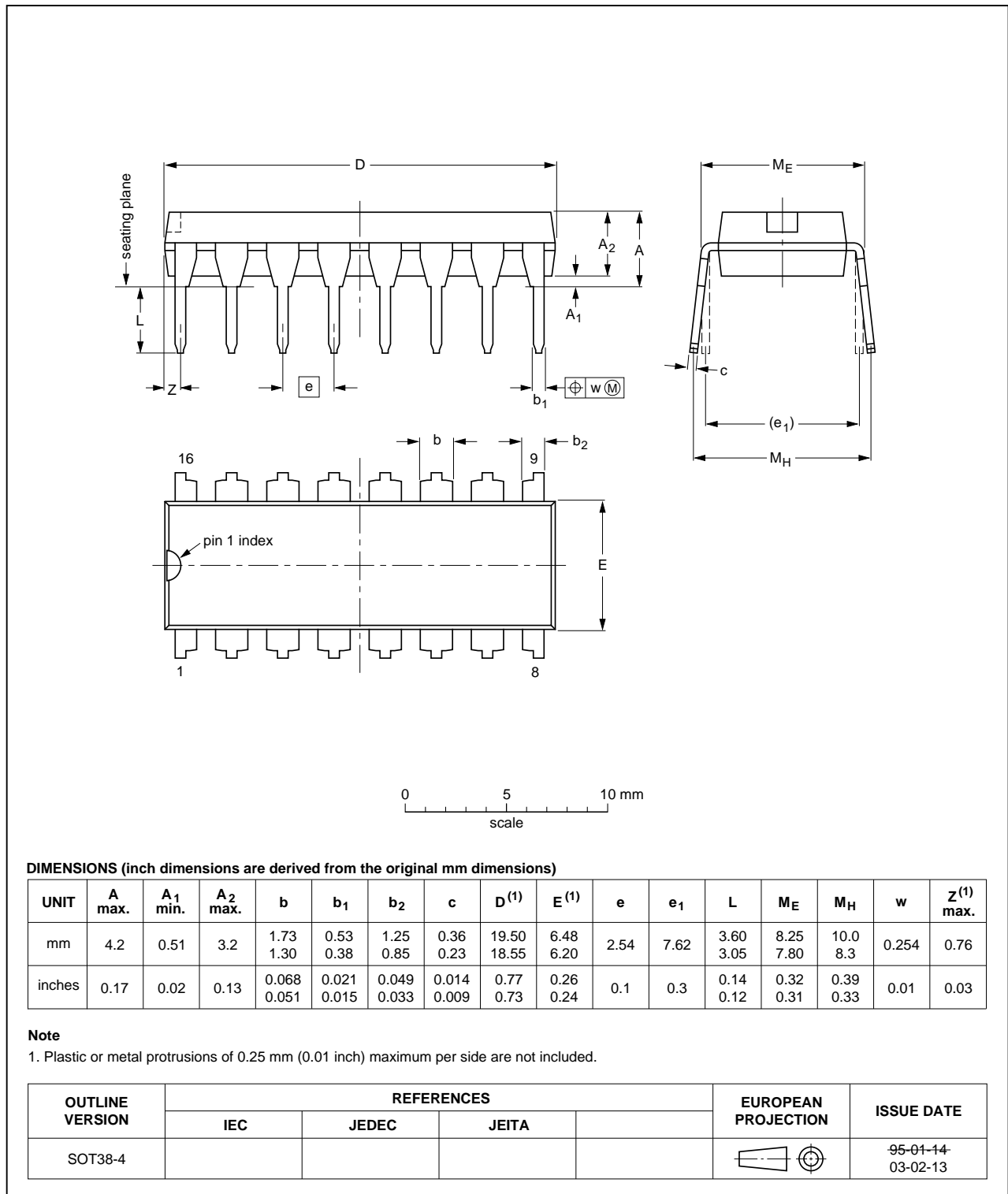


Fig 16. Package outline SOT38-4 (DIP16)



SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

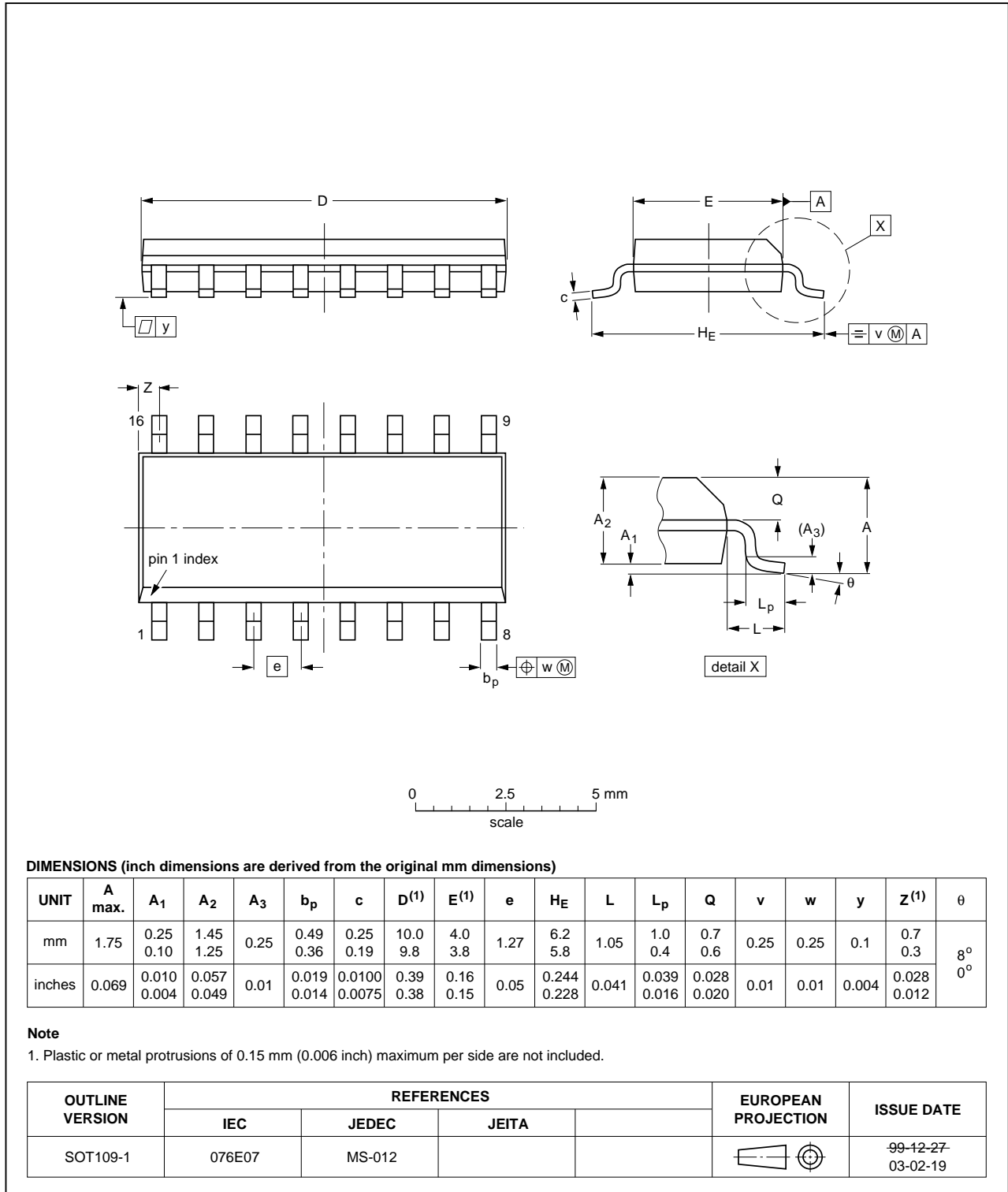
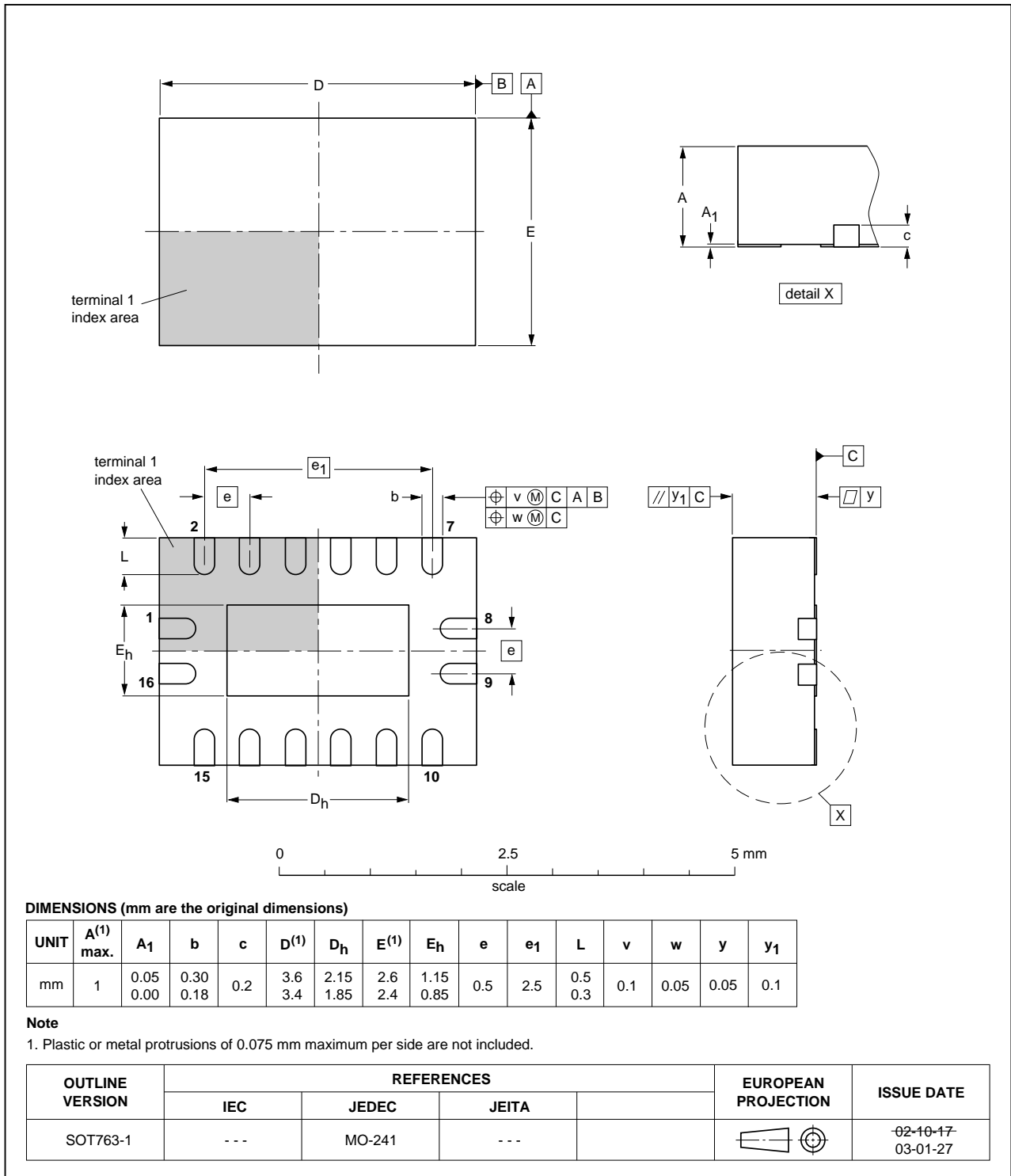


Fig 17. Package outline SOT109-1 (SO16)

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm**

**SOT763-1**



**Fig 18. Package outline SOT763-1 (DHVQFN16)**

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

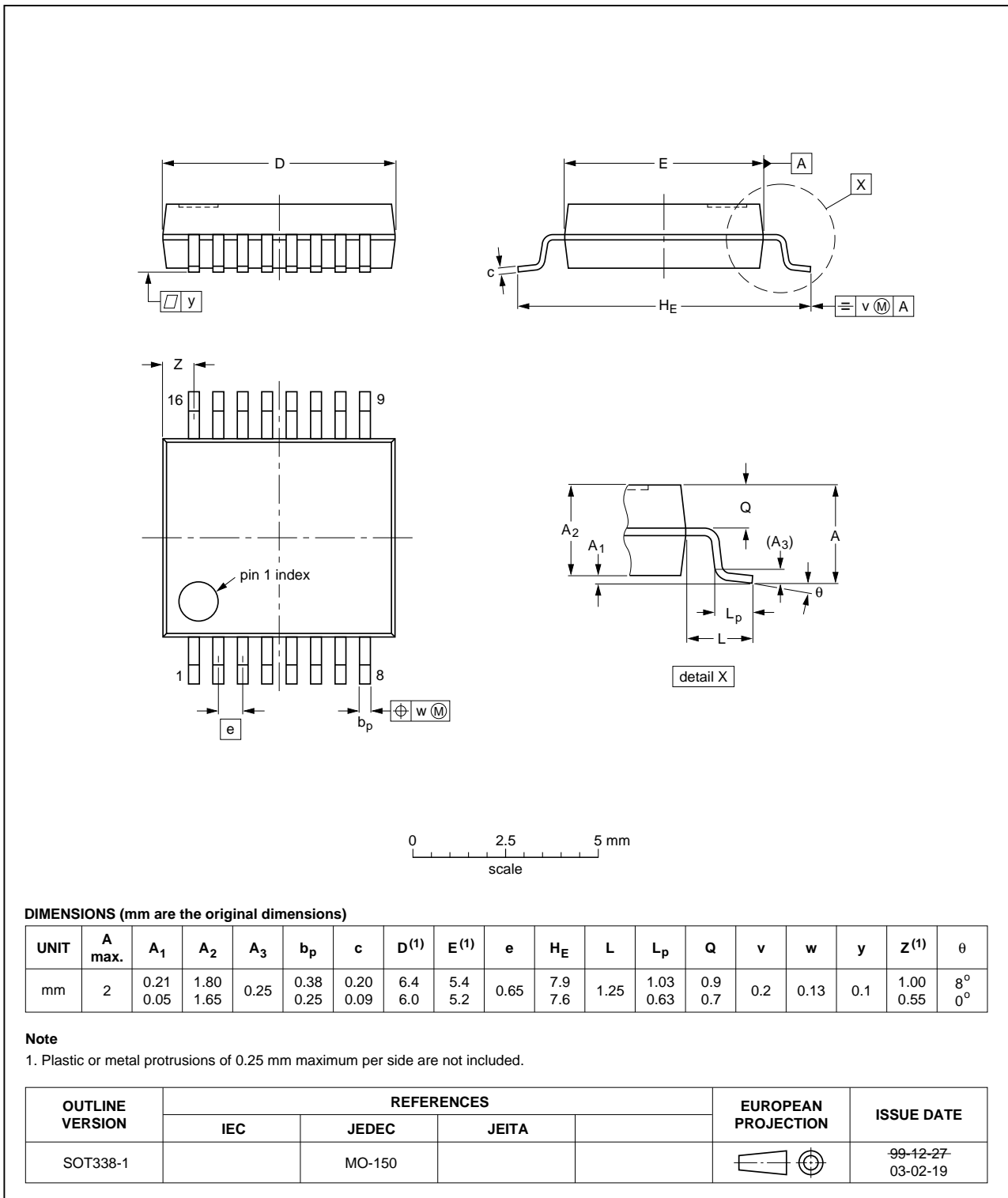


Fig 19. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

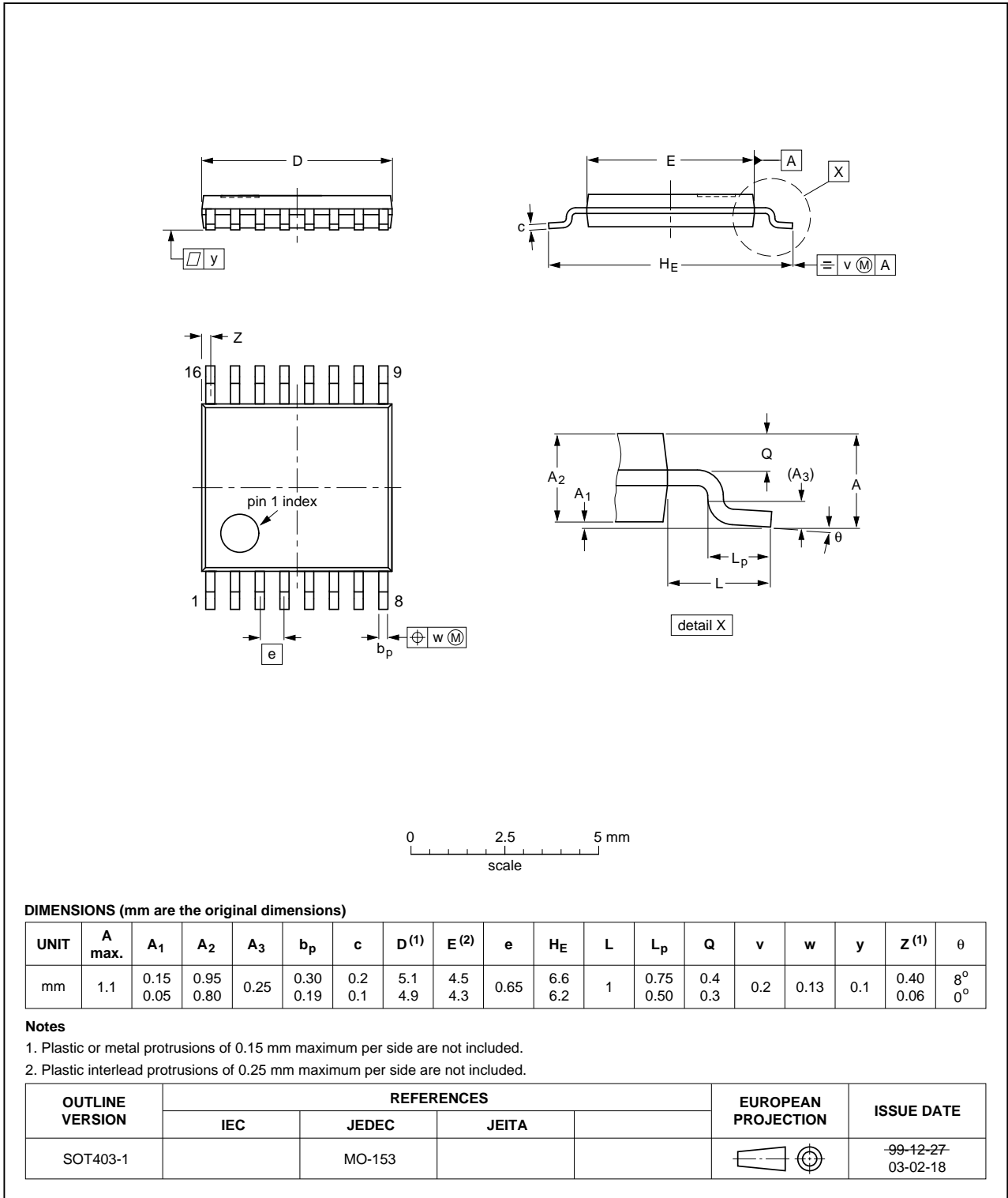


Fig 20. Package outline SOT403-1 (TSSOP16)

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT423 v.6	20111219	Product data sheet	-	74HC_HCT423 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74HC_HCT423 v.5	20110825	Product data sheet	-	74HC_HCT423 v.4
74HC_HCT423 v.4	20110318	Product data sheet	-	74HC_HCT423 v.3
74HC_HCT423 v.3	20080724	Product data sheet	-	74HC_HCT423_CNV v.2
74HC_HCT423_CNV v.2	19980708	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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