

# DATA SHEET

## **74LVC373A**

**Octal D-type transparent latch with  
5 V tolerant inputs/outputs; 3-state**

Product specification  
Supersedes data of 1998 Jul 29

2003 May 19

## Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

### 74LVC373A

#### FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance outputs when  $V_{CC} = 0$  V
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

#### DESCRIPTION

The 74LVC373A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay Dn to Qn LE to Qn	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.0 3.1	ns ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per latch	$V_{CC} = 3.3$ V; notes 1 and 2	14	pF

#### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

The 74LVC373A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus-oriented applications. A latch enable input (pin LE) and an output enable input (pin  $\overline{OE}$ ) are common to all internal latches.

The 74LVC373A consists of eight D-type transparent latches with 3-state true outputs. When pin LE is HIGH, data at the D-inputs (pins D0 to D7) enters the latches. In this condition, the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When pin LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of pin LE. When pin  $\overline{OE}$  is LOW, the contents of the eight latches are available at the Q-outputs (pins Q0 to Q7). When pin  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of input pin  $\overline{OE}$  does not affect the state of the latches.

The 74LVC373A is functionally identical to the 74LVC573A, but the 74LVC573A has a different pin arrangement.

# Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

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**FUNCTION TABLE**

See note 1.

OPERATING MODES	INPUT			INTERNAL LATCHES	OUTPUT
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	X	X	X	Z

**Note**

- H = HIGH voltage level;  
h = HIGH voltage level one setup time prior to the HIGH-to-LOW LE transition;  
L = LOW voltage level;  
l = LOW voltage level one setup time prior to the HIGH-to-LOW LE transition;  
X = don't care;  
Z = high-impedance OFF-state.

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC373AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC373ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC373APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC373ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

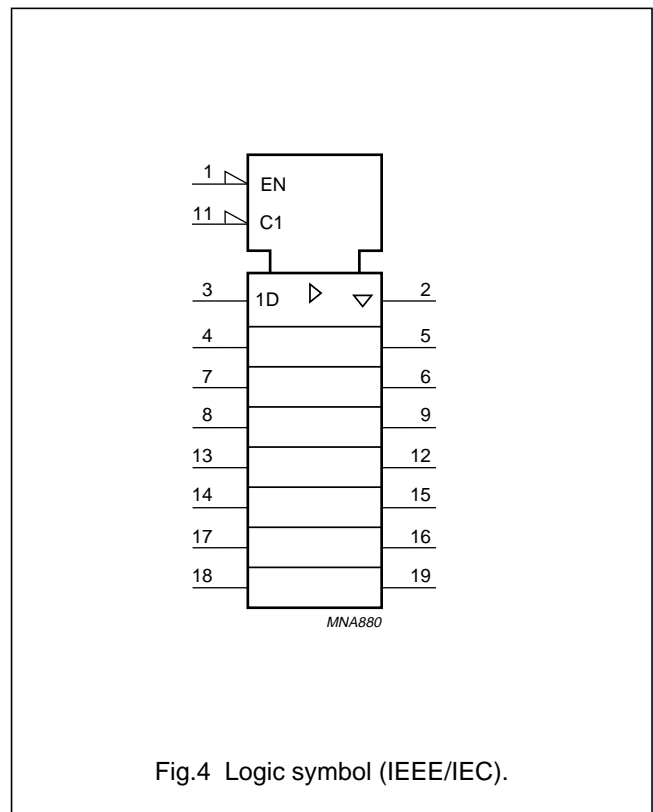
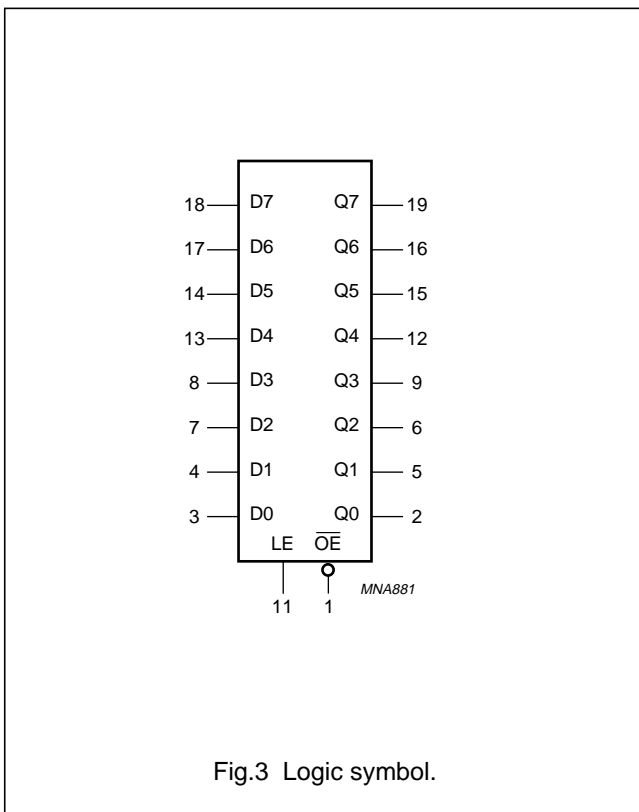
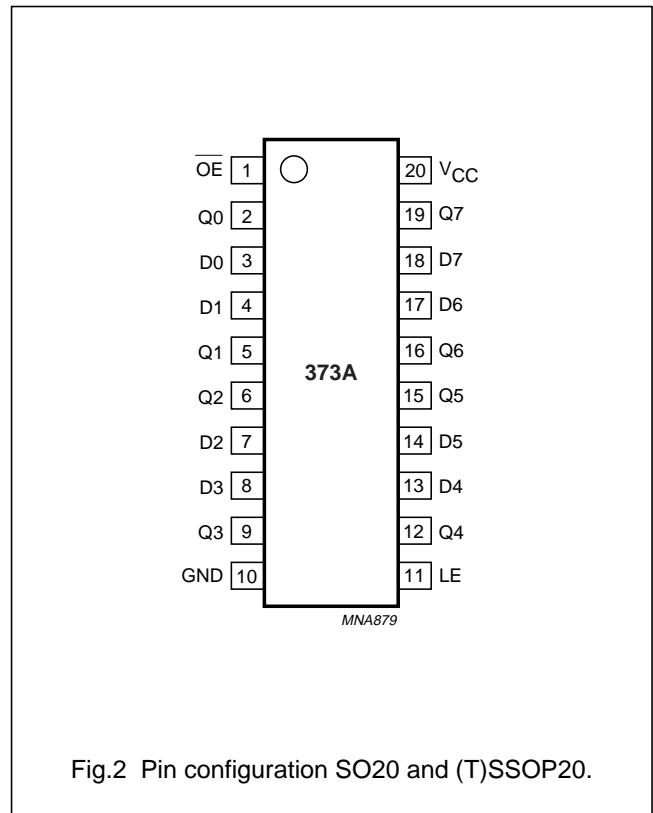
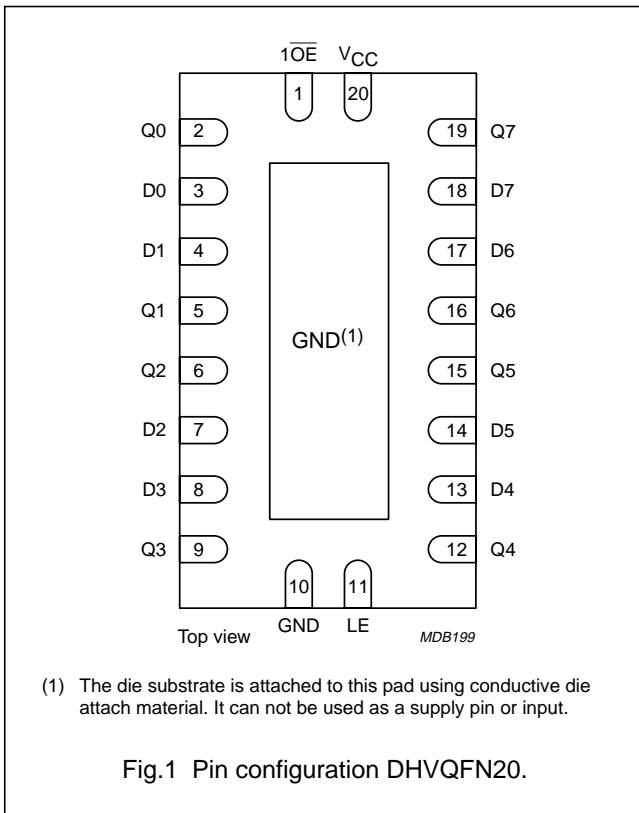
**PINNING**

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	output enable input (active LOW)
2	Q0	latch output
3	D0	data input
4	D1	data input
5	Q1	latch output
6	Q2	latch output
7	D2	data input
8	D3	data input
9	Q3	latch output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	LE	latch enable input (active HIGH)
12	Q4	latch output
13	D4	data input
14	D5	data input
15	Q5	latch output
16	Q6	latch output
17	D6	data input
18	D7	data input
19	Q7	latch output
20	V <sub>CC</sub>	supply voltage

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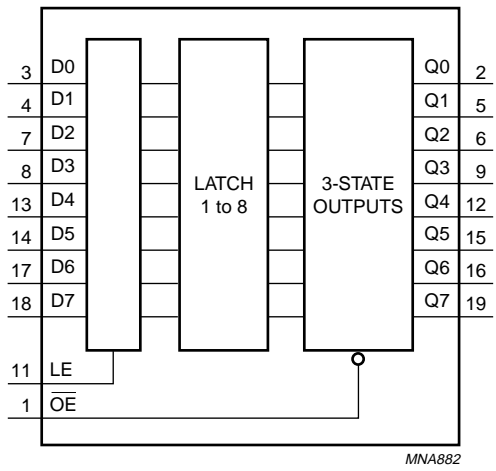


Fig.5 Functional diagram.

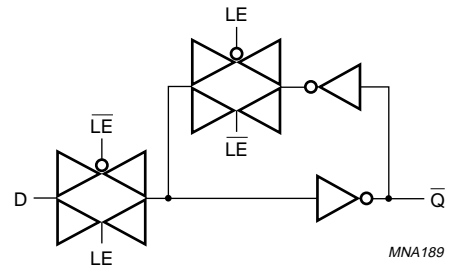


Fig.6 Logic diagram (one latch).

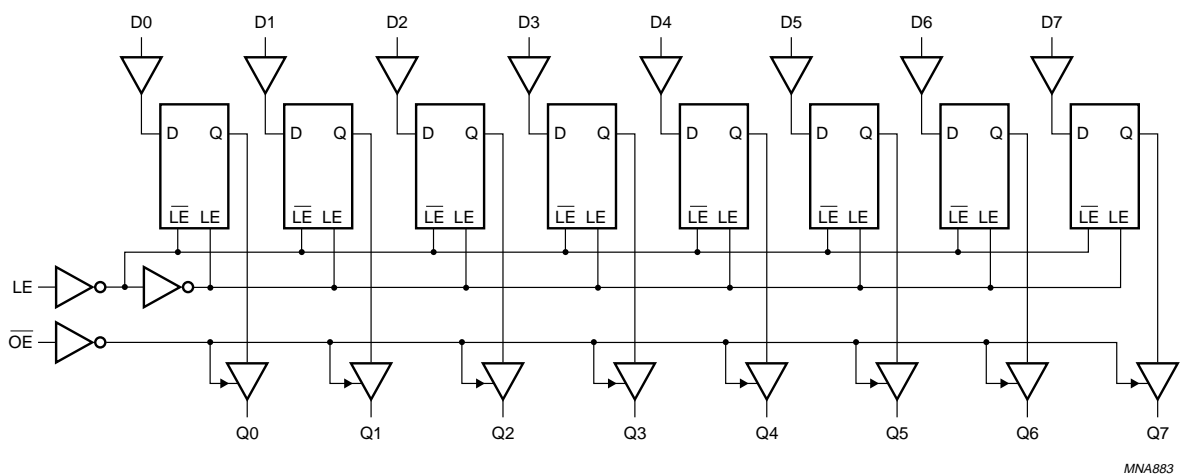


Fig.7 Logic diagram.

# Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	HIGH or LOW state	0	V <sub>CC</sub>	V
		3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		3-state; note 1	-0.5	+6.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA	2.7 to 3.6	V <sub>CC</sub> - 0.2	-	-	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA	2.7 to 3.6	-	-	0.2	V
		I <sub>O</sub> = 12 mA	2.7	-	-	0.4	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	±0.1	±5	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	±0.1	±5	µA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	±0.1	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	5	500	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -100 µA	2.7	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 0.75	-	-	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 1.0	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	-	-	0.3	V
		I <sub>O</sub> = 100 µA	2.7	-	-	0.6	V
		I <sub>O</sub> = 12 mA	3.0	-	-	0.8	V
		I <sub>O</sub> = 24 mA					
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	-	±20	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	-	±20	µA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	-	±20	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	-	40	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	-	5000	µA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.



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**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ .

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay Dn to Qn	see Figs 8 and 12	1.2	–	14	–	ns
			2.7	1.5	3.5	7.8	ns
			3.0 to 3.6	1.5	3.0 <sup>(1)</sup>	6.8	ns
	propagation delay LE to Qn	see Figs 9 and 12	1.2	–	16	–	ns
			2.7	1.5	3.4	8.2	ns
			3.0 to 3.6	1.5	3.1 <sup>(1)</sup>	7.2	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Figs 10 and 12	1.2	–	17	–	ns
			2.7	1.5	4.2	8.7	ns
			3.0 to 3.6	1.5	3.4 <sup>(1)</sup>	7.7	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Figs 10 and 12	1.2	–	8.0	–	ns
			2.7	1.5	3.3	7.1	ns
			3.0 to 3.6	1.5	2.9 <sup>(1)</sup>	6.1	ns
t <sub>w</sub>	LE pulse width HIGH	see Fig.9	2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	1.5 <sup>(1)</sup>	–	ns
t <sub>su</sub>	set-up time Dn to LE	see Fig.11	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0 <sup>(1)</sup>	–	ns
t <sub>h</sub>	hold time Dn to LE	see Fig.11	2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	0.3 <sup>(1)</sup>	–	ns
t <sub>sk(0)</sub>	skew	note 2	–	–	–	1.0	ns

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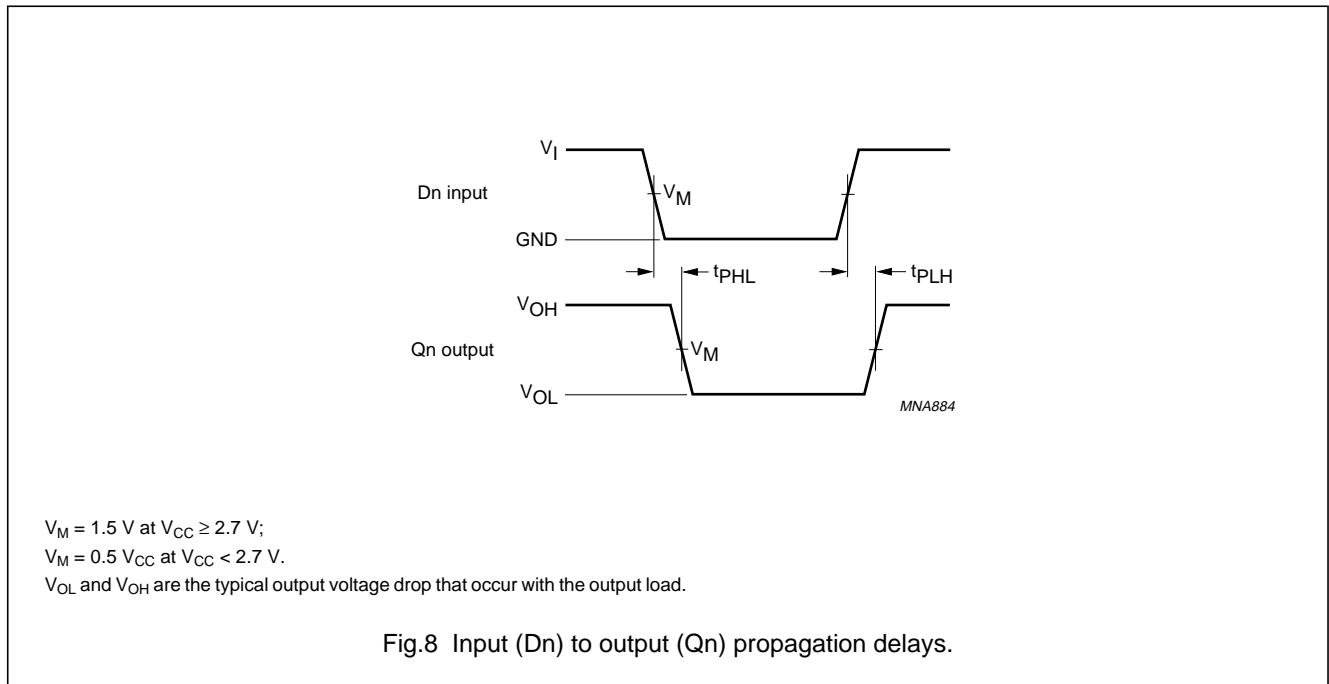
74LVC373A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay Dn to Qn	see Figs 8 and 12	2.7	1.5	–	10.0	ns
			3.0 to 3.6	1.5	–	8.5	ns
	propagation delay LE to Qn	see Figs 9 and 12	2.7	1.5	–	10.5	ns
			3.0 to 3.6	1.5	–	9.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Figs 10 and 12	2.7	1.5	–	11.0	ns
			3.0 to 3.6	1.5	–	10.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Figs 10 and 12	2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.5	–	8.0	ns
t <sub>W</sub>	LE pulse width HIGH	see Fig.9	2.7	4.5	–	–	ns
			3.0 to 3.6	4.5	–	–	ns
t <sub>su</sub>	set-up time Dn to LE	see Fig.11	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	–	–	ns
t <sub>h</sub>	hold time Dn to LE	see Fig.11	2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	–	–	ns
t <sub>sk(0)</sub>	skew	note 2	–	–	–	1.5	ns

**Notes**

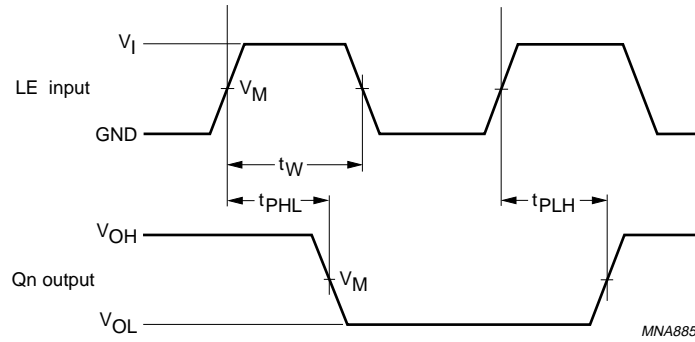
1. Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

**AC WAVEFORMS**



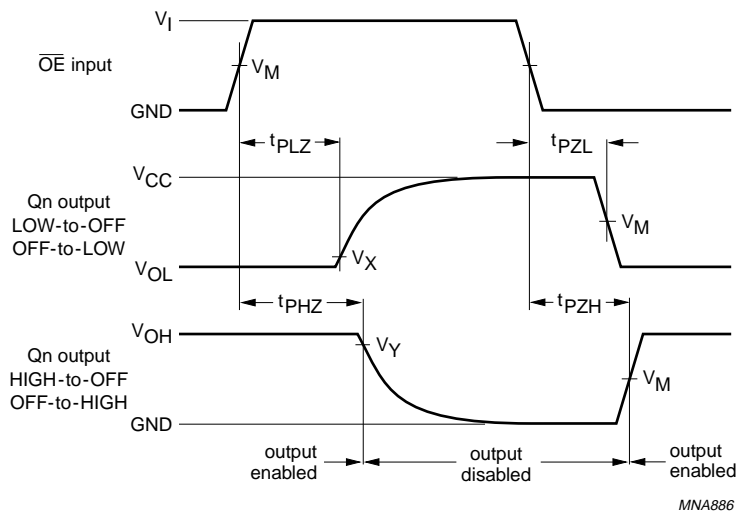
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$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

Fig.9 Latch Enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays.

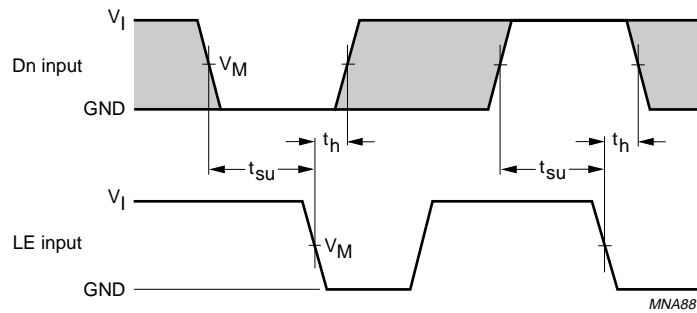


$V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_Y = V_{OH} - 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

Fig.10 3-state enable and disable times.

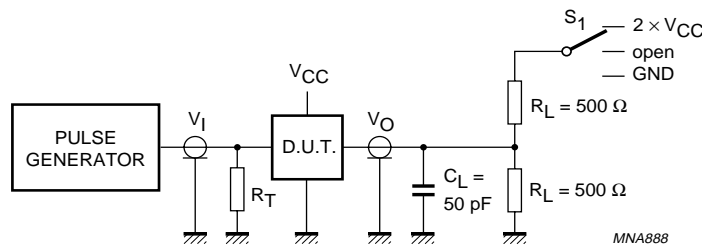
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$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.11 Data set-up and hold times for the Dn input to the LE input.



TEST	S <sub>1</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 × V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V <sub>CC</sub>	V <sub>I</sub>
<2.7 V	V <sub>CC</sub>
2.7 to 3.6 V	2.7 V

Definitions for test circuit:  
 R<sub>L</sub> = Load resistor.  
 C<sub>L</sub> = Load capacitance including jig and probe capacitance.  
 R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.12 Load circuitry for switching times.

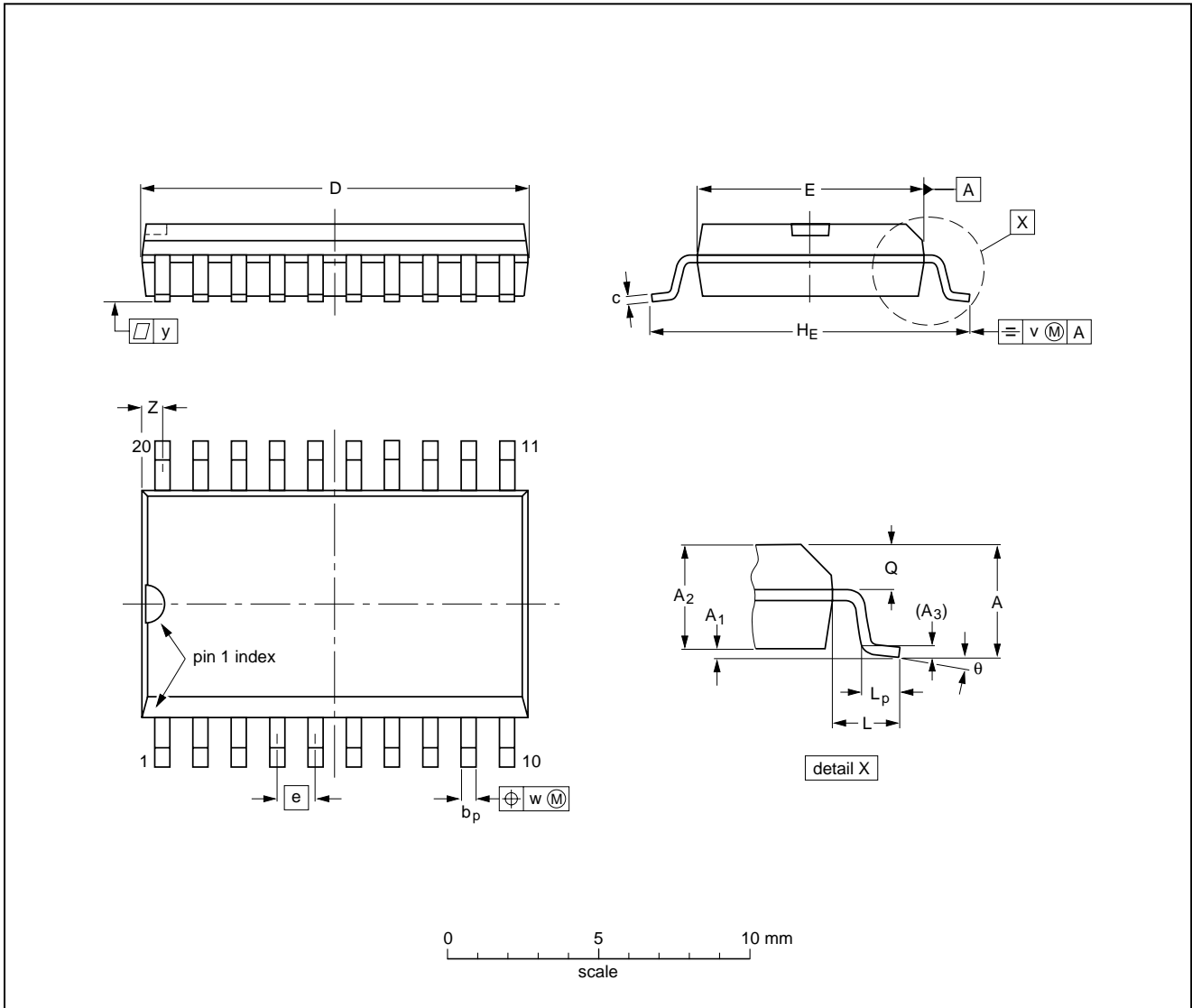
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## PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

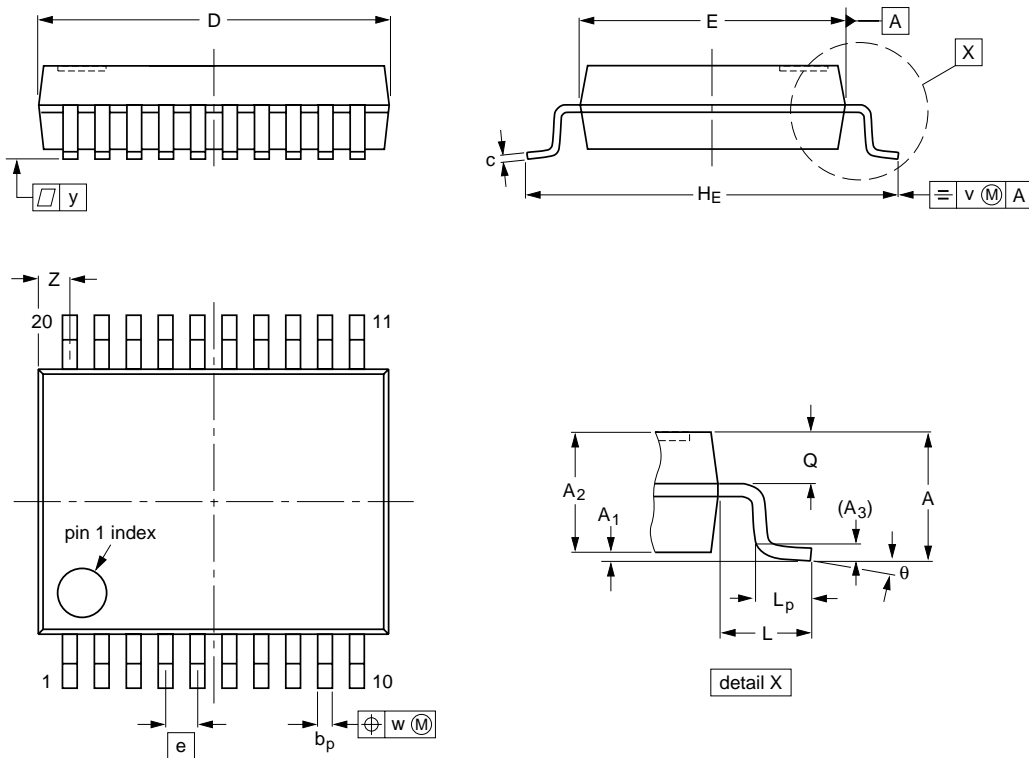
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Octal D-type transparent latch with  
5 V tolerant inputs/outputs; 3-state

74LVC373A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

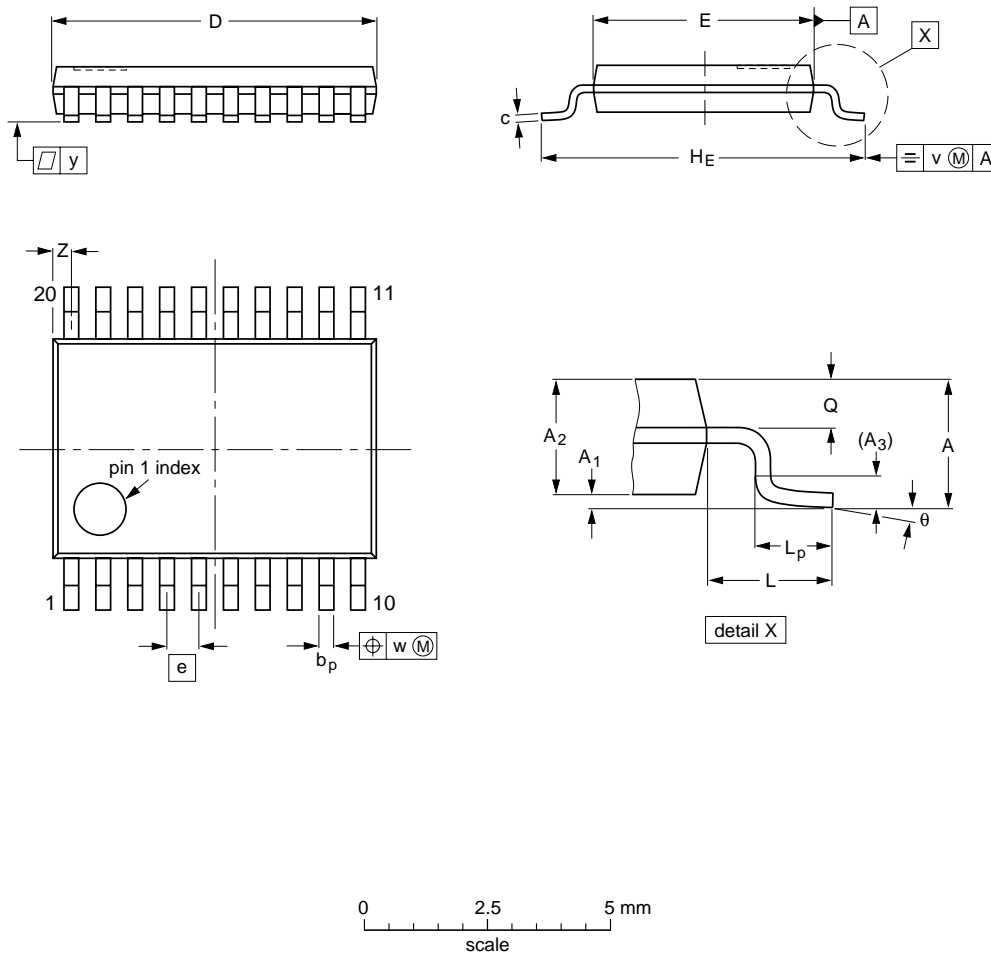
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

Octal D-type transparent latch with  
5 V tolerant inputs/outputs; 3-state

74LVC373A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

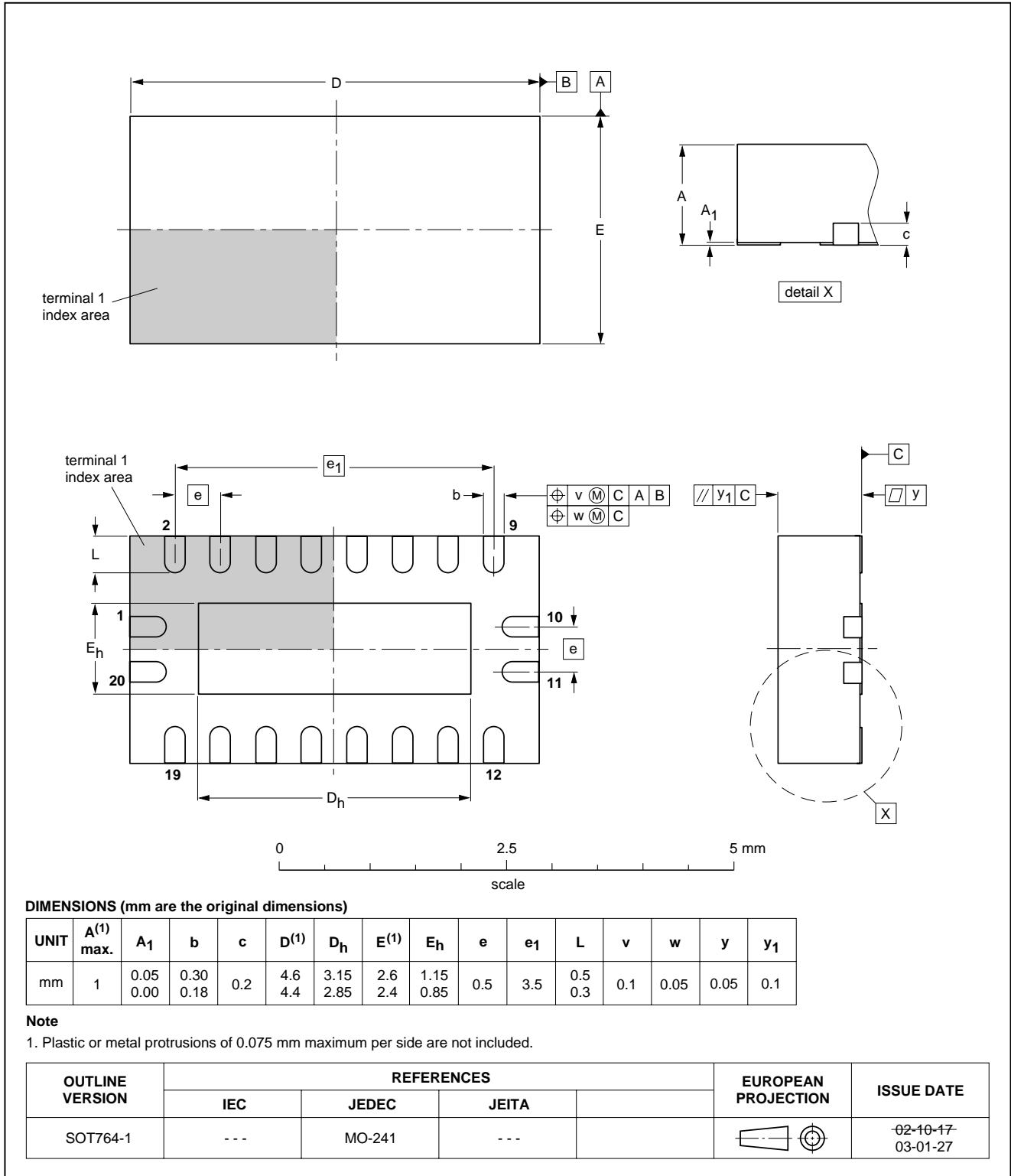
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				99-12-27 03-02-19

Octal D-type transparent latch with  
5 V tolerant inputs/outputs; 3-state

74LVC373A

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1





## Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

### Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(3)</sup>	suitable
PLCC <sup>(4)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(4)(5)</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(6)</sup>	suitable

#### Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

# Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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