INCH-POUND
MIL-M-38510/101K
14 December 2005
SUPERSEDING
MIL-M-38510/101J
07 February 2003

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

Inactive for new design after 13 July 1995.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, operational amplifiers. Two product assurance classes and a choice of case outlines and lead finish are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.1.2 Part or identifying number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	Single operational amplifier - internally compensated
02	Dual operational amplifier - internally compensated
03	Single operational amplifier - externally compensated
04	Single operational amplifier - externally compensated
05	Dual operational amplifier - externally compensated 1/
06	Dual operational amplifier - externally compensated 1/
07	Single operational amplifier, high speed
08	Dual operational amplifier - internally compensated

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1/ Device types 05 and 06 may be monolithic, or they may consist of two separate, independent die.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43218-3990, or emailed to linear@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A 2/	GDFP5-F14 or CDFP6-F14	14	Flat pack
B 2/	GDFP4-14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
G	MACY1-X8	8	Can
H	GDFP1-F10 or CDFP2-F10	10	Flat pack
I	MACY1-X10	10	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
Z	GDFP1-G10	10	Flat pack with gullwing leads
2	CQCC1-N20	20	Square leadless chip carrier

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) ..... ±22 V dc 3/
Input voltage range ..... ±20 V dc 4/
Differential input voltage range ..... ±30 V dc 5/
Input current range ..... -0.1 mA to +10 mA
Storage temperature range ..... -65°C to +150°C
Output short-circuit duration ..... Unlimited 6/
Lead temperature (soldering, 60 seconds) ..... +300°C
Junction temperature (T_J) ..... +175°C 7/

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... ±5 V dc to ±20 V dc
Ambient temperature range (T_A) ..... -55°C to +125°C

2/ Inactive package case outline.
3/ Voltages in excess of these may be applied for short-term tests if voltage difference does not exceed 44 volts.
4/ For supply voltages less than ±20 V dc, the absolute maximum input voltage is equal to the supply voltage.
5/ For device types 04, 06, and 07 only, this rating is ±1.0 V unless resistances of 2 kΩ or greater are inserted in series with the inputs to limit current in the input shunt diodes to the maximum allowable value.
6/ Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
7/ For short term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum) T_J = +275°C.

1.5 Power and thermal characteristics.

Case outlines	Maximum allowable power dissipation	Maximum θ_{JC}	Maximum θ_{JA}
A,B,D	350 mW at T_A = +125°C	60°C/W	140°C/W
C,E,P	400 mW at T_A = +125°C	35°C/W	120°C/W
G	330 mW at T_A = +125°C	40°C/W	150°C/W
I	350 mW at T_A = +125°C	40°C/W	140°C/W
H	330 mW at T_A = +125°C	60°C/W	150°C/W
F	400 mW at T_A = +125°C	35°C/W	120°C/W
Z	330 mW at T_A = +125°C	21°C/W	225°C/W still air
			142°C/W 500 LFPM
2	8/ at T_A = +125°C	60°C/W	120°C/W

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

8/ P_D = 102 mW for device type 01. P_D = 75 mW for device type 03. P_D = 149 mW for device type 04.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VAS) upon request.

3.3.3 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. Lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The following electrical performance characteristics apply over the full operating ambient temperature range of -55°C to +125°C and for supply voltages ±5 V dc to ±20 V dc, unless otherwise specified (see table I).

3.5.1 Offset null circuits. Each amplifier having nulling inputs (device types 01, 02, 03, 05, and 07) shall be capable of being nulled 1 mV beyond the specified offset voltage limits for $-55°C \leq T_A \leq +125°C$ using the circuits of figure 2.

3.5.2 Frequency compensation. Device types 01, 02, 07, and 08 shall be free of oscillation when operated in a unity gain non-inverting mode with no external compensation and a source resistance of ≤ 10 kΩ, and when operated in any test condition specified herein. Device types 03, 04, 05, and 06 shall be free from oscillation when compensated with a 30 pF capacitor for all gain configurations or a 3 pF capacitor when used with a gain of 10.

3.6 Rebonding. Rebonding shall be in accordance with MIL-PRF-38535.

3.7 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.8 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 49 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	$R_S = 50\ \Omega$ 2/	1	01,02, 08	-3	+3	mV
				03,05	-2	+2	
				04,06	-0.5	+0.5	
				07	-4	+4	
			2,3	01,02, 08	-4	+4	
				03,05	-3	+3	
				04,06	-1	+1	
				07	-6	+6	
Input offset voltage temperature sensitivity	$\Delta V_{IO} / \Delta T$		2	01,02, 08	-15	+15	µV/°C
				03,05	-18	+18	
				04,06	-5	+5	
				07	-50	+50	
			3	01,02, 03,05	-15	+15	
				04,06	-5	+5	
				07	-50	+50	
				08	-20	20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Input offset current	I_{IO}	2/	1	01,02,08	-30	+30	nA	
				03,05	-10	+10		
				04,06	-0.2	+0.2		
				07	-40	+40		
			2	01	-30	+30		*
			2,3	02,08	-70	+70		
				03,05	-20	+20		
				04,06	-0.4	+0.4		
				07	-80	+80		
			3	01	-70	+70		*
Input offset current temperature sensitivity	$\Delta I_{IO} / \Delta T$		2	01,02,08	-500	+500	pA/°C	
				03,05	-200	+200		
				04,06	-2.5	+2.5		
				07	-1000	+1000		
			3	01,02,08	-200	+200		
				03,05	-100	+100		
				04,06	-2.5	+2.5		
				07	-1000	+1000		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input bias current	$+I_{IB}$	2/	1,2	01,02, 08	-0.1	+110	nA
				03,05	-0.1	+75	
				07	-0.1	+250	
			1	04,06	-0.1	+2.0	
			2		-1.0	+2.0	
			3	01,02, 08	-0.1	+265	
				03,05	-0.1	+100	
				04,06	-0.1	+3.0	
				07	-0.1	+400	
	$-I_{IB}$		1,2	01,02, 08	-0.1	+110	
				03,05	-0.1	+75	
				07	-0.1	+250	
			1	04,06	-0.1	+2.0	
			2		-1.0	+2.0	
			3	01,02, 08	-0.1	+265	
				03,05	-0.1	+100	
				04,06	-0.1	+3.0	
				07	-0.1	+400	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio	+PSRR	$+V_{CC}$ = 10 V, R_S = 50 Ω, $-V_{CC}$ = -20 V	1	01,02, 03,05, 08	-50	+50	µV/V
				04,06	-16	+16	
				07	-100	+100	
			2,3	01,02, 03,05, 08	-100	+100	
				04,06	-16	+16	
				07	-150	+150	
	-PSRR	$+V_{CC}$ = 20 V, R_S = 50 Ω, $-V_{CC}$ = -10 V	1	01,02, 03,05, 08	-50	+50	
				04,06	-16	+16	
				07	-100	+100	
			2,3	01,02, 03,05, 08	-100	+100	
				04,06	-16	+16	
				07	-150	+150	
Input voltage common mode rejection	CMR	$\pm V_{CC}$ = 20 V, V_{IN} = ±15 V, R_S = 50 Ω	1,2,3	01,02, 03,05, 07,08	80		dB
				04,06	96		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Adjustment for input offset voltage 3/	V_{IO} ADJ(+)	$\pm V_{CC}$ = 20 V	1,2,3	01,02, 08	+5		mV	
				03,05	+4			
				04,06	No external ADJ			
				07	+7			
Adjustment for input offset voltage 3/	V_{IO} ADJ(-)	$\pm V_{CC}$ = 20 V	1,2,3	01,02, 08		-5	mV	
				03,05		-4		
				04,06		No extern al ADJ		
				07		-7		
Output short-circuit current (for positive output)	I_{OS}(+)	$\pm V_{CC}$ = 15 V, t ≤ 25 ms 4/	1,2,3	01,02, 03,05, 08	-60		mA	
				04	-20			*
				06	-20			*
				07	-65			
Output short-circuit current (for negative output)	I_{OS}(-)	$\pm V_{CC}$ = 15 V, t ≤ 25 ms 4/	1,2,3	01,02, 03,05, 08		+60	mA	
				04		+20		*
				06		+20		*
			1,2	07		+65		
			3			+80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current	I_{CC}	$\pm V_{CC} = \pm 15$ V 5/	1	01,02, 08		+3.8	mA
				03,05		+3	
				04,06		+0.6	
				07		+8	
			2	01,02, 08		+3.4	
				03,05		+2.5	
				04,06		+0.6	
				07		+7	
			3	01,02, 08		+4.2	
				03,05		+3.5	
				04,06		+0.8	
				07		+9	
Output voltage swing (maximum)	V_{OP}	$\pm V_{CC} = 20$ V, $R_L = 10$ kΩ	4,5,6	01-06, 08	±16		V
				07	±17		
		$\pm V_{CC} = 20$ V, $R_L = 2$ kΩ		01,02, 03,05, 08	±15		
				04,06	Not speci-fied		
				07	±16		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Open loop voltage gain 6/ (single ended)	$A_{VS}(\pm)$	$\pm V_{CC}$ = 20 V, 7/ R_L = 2 kΩ, 10 kΩ V_{OUT} = ±15 V	4	01,02, 03,05, 07,08	50		V/mV
				04,06	80		
			5,6	01,02, 03,05, 08	25		
				04,06	40		
				07	32		
Open loop voltage gain 6/ (single ended)	A_{VS}	$\pm V_{CC}$ = 5 V, 7/ R_L = 2 kΩ, 10 kΩ V_{OUT} = ±2 V	4,5,6	01,02, 03,05, 07,08	10		V/mV
				04,06	20		
Transient response rise time	$TR_{(tr)}$	See figure 4 8/	7,8A,8B	01,02, 03,05, 08		+800	ns
				04,06		+1000	
				07		+40	
Transient response overshoot	$TR_{(OS)}$	See figure 4 8/	7,8A,8B	01,02, 03,05, 08		+25	%
				04,06, 07		+50	
Slew rate 9/	SR(+)	V_{IN} = ±5 V, A_V = 1, see figure 4	7,8B	01,02, 08	+0.3		V/µs
				03,05	10/		
				04,06	+0.05		
				07	+40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Slew rate 9/	SR(+)	$V_{IN} = \pm 5$ V, $A_V = 1$, see figure 4	8A	01,02, 03,05, 08	+0.3		V/µs
				04,06	+0.05		
				07	+30		
Slew rate 9/	SR(-)	$V_{IN} = \pm 5$ V, $A_V = 1$, see figure 4	7,8B	01,02, 08	+0.3		V/µs
				03,05	10/		
				04,06	+0.05		
				07	+40		
			8A	01,02, 03,05, 08	+0.3		
				04,06	+0.05		
				07	+30		
Settling time 11/	$t_S(+)$	See figure 4	12	07		800	ns
			13A,13B			1200	
	$t_S(-)$		12			800	
			13A,13B			1200	
Channel separation	CS	$\pm V_{CC} = \pm 20$ V, see figure 5, $T_A = +25°C$	7	02,05, 06,08	80		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ see figure 3 unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Noise (referred to input) broadband	NI(BB)	$\pm V_{CC}$ = 20 V, T_A = +25°C, bandwidth = 5 kHz	7	01-06, 08		15	µVrms
				07		25	
Noise (referred to input) popcorn	NI(PC)	$\pm V_{CC}$ = 20 V, T_A = +25°C, bandwidth = 5 kHz	7	01,02, 04,06, 08		40	µVpk
				03,05, 07		80	

1/ For devices marked with the "Q" certification mark, the parameters listed herein maybe guaranteed if not tested to the limits specified herein in accordance with the manufacturer's QM plan.

2/ Tests at common mode V_{CM} = 0 V, V_{CM} = -15 V, and V_{CM} = +15 V.

3/ $V_{IO(ADJ)}$ is not performed on device type 02, case I only, or on device type 08 for either case G or P.

4/ Continuous short circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \le +75°C$ will cause T_J to exceed the maximum of +175°C. For dual devices, I_{OS} is measured one channel at a time.

5/ Value shown is for single devices (01, 03, 04) only. For dual devices (02, 05, 06, and 08) this limit is for single devices.

6/ Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed loop applications (closed loop gain less than 1,000), the open loop tests (AVS) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open loop gain or open loop gain linearity), they should be specified in the individual procurement document as additional requirements.

7/ R_L = 10 kΩ only for device types 04 and 06.

8/ For transient response tests, C_F = 10 pF for device types 01, 02, 03, 04, 05, 06, and 08. Device type 07, C_F = 47 pF. C_F includes the effects of stray capacitance.

9/ Minimum limit for device 08 is 0.4 V/µs at all temperatures.

10/ Minimum limits for device types 03 and 05 are 0.2 V/µs at -55°C and 0.3 V/µs at both +25°C and +125°C.

11/ Settling time is waived for method 5004, MIL-STD-883 except for device type 07.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters 1/	1,2,3,4	1,2,3,4
Group A test requirements	1,2,3,4,5,6, 7,8A,8B,12, 13A,13B	1,2,3,4,5,6,7
Group C end point electrical parameters	1,2,3, and table IV delta limits	1 and table IV delta limits
Additional electrical subgroups For group C periodic inspections	Not applicable	8A,8B,12, 13A,13B
Group D end point electrical parameters	1,2,3	1

1/ PDA applies to subgroup 1.

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

Device type	01			
Case outlines	A,B,C,D	G and P	H	2
Terminal number	Terminal symbol			
1	NC	OFFSET NULL	NC	NC
2	NC	-INPUT	OFFSET NULL	OFFSET NULL (-)
3	OFFSET NULL	+INPUT	-INPUT	NC
4	-INPUT	$-V_{CC}$	+INPUT	NC
5	+INPUT	OFFSET NULL	$-V_{CC}$	-INPUT
6	$-V_{CC}$	OUTPUT	OFFSET NULL	NC
7	NC	$+V_{CC}$	OUTPUT	+INPUT
8	NC	NC	$+V_{CC}$	NC
9	OFFSET NULL	---	NC	NC
10	OUTPUT	---	NC	$-V_{CC}$
11	$+V_{CC}$	---	---	NC
12	NC	---	---	OFFSET NULL (+)
13	NC	---	---	NC
14	NC	---	---	NC
15	---	---	---	OUTPUT
16	---	---	---	NC
17	---	---	---	$+V_{CC}$
18	---	---	---	NC
19	---	---	---	NC
20	---	---	---	NC

NC = No connection

FIGURE 1. Terminal connections.

Device type	02		03		
Case outlines	A,B,C,D	I	C	G and P	H
Terminal number	Terminal symbol				
1	-INPUT A	OUTPUT A	NC	OFFSET NULL / COMP	NC
2	+INPUT A	$+V_{CC}$ (A) SEE NOTE 2	NC	-INPUT	OFFSET NULL / COMP
3	OFFSET NULL A	-INPUT A	OFFSET NULL / COMP	+INPUT	-INPUT
4	$-V_{CC}$	+INPUT A	-INPUT	$-V_{CC}$	+INPUT
5	OFFSET NULL B	$-V_{CC}$	+INPUT	OFFSET NULL	$-V_{CC}$
6	+INPUT B	+INPUT B	$-V_{CC}$	OUTPUT	OFFSET NULL
7	-INPUT B	-INPUT B	NC	$+V_{CC}$	OUTPUT
8	OFFSET NULL B	$+V_{CC}$ (B) SEE NOTE 2	NC	COMP	$+V_{CC}$
9	$+V_{CC}$ (B) SEE NOTE 2	OUTPUT B	OFFSET NULL	---	COMP
10	OUTPUT B	NC	OUTPUT	---	NC
11	NC	---	$+V_{CC}$	---	---
12	OUTPUT A	---	COMP	---	---
13	$+V_{CC}$ (A) SEE NOTE 2	---	NC	---	---
14	OFFSET NULL A	---	NC	---	---
15	---	---	---	---	---
16	---	---	---	---	---
17	---	---	---	---	---
18	---	---	---	---	---
19	---	---	---	---	---
20	---	---	---	---	---

NC = No connection

FIGURE 1. Terminal connections – Continued.

Device type	03	04			
Case outlines	2	C	G and P	H	2
Terminal number	Terminal symbol				
1	NC	NC	INPUT COMP	NC	NC
2	OFFSET NULL (-)	INPUT COMP	-INPUT	GUARD	INPUT COMP
3	NC	GUARD	+INPUT	-INPUT	NC
4	NC	-INPUT	$-V_{CC}$	+INPUT	NC
5	-INPUT	+INPUT	NC	GUARD	-INPUT
6	NC	GUARD	OUTPUT	$-V_{CC}$	NC
7	+INPUT	$-V_{CC}$	$+V_{CC}$	OUTPUT	+INPUT
8	NC	NC	OUTPUT COMP	$+V_{CC}$	NC
9	NC	NC	---	OUTPUT COMP	NC
10	$-V_{CC}$	OUTPUT	---	INPUT COMP	$-V_{CC}$
11	NC	$+V_{CC}$	---	---	NC
12	OFFSET NULL (+)	OUTPUT COMP	---	---	NC
13	NC	NC	---	---	NC
14	NC	NC	---	---	NC
15	OUTPUT	---	---	---	OUTPUT
16	NC	---	---	---	NC
17	$+V_{CC}$	---	---	---	$+V_{CC}$
18	NC	---	---	---	NC
19	NC	---	---	---	NC
20	FREQ COMP	---	---	---	OUTPUT COMP

NC = No connection

FIGURE 1. Terminal connections – Continued.

Device type	05	06	07	
Case outlines	E and F	E and F	C	G and P
Terminal number	Terminal symbol			
1	$+V_{CC}$ (A) SEE NOTE 5	$+V_{CC}$ (A) SEE NOTE 5	NC	COMP A / OFFSET NULL
2	COMP A	OUTPUT COMP A	NC	-INPUT
3	OFFSET NULL / COMP	INPUT COMP A	COMP A / OFFSET NULL	+INPUT
4	-INPUT A	-INPUT A	-INPUT	$-V_{CC}$
5	+INPUT A	+INPUT A	+INPUT	COMP B / OFFSET NULL
6	$-V_{CC}$	$-V_{CC}$	$-V_{CC}$	OUTPUT
7	OFFSET NULL B	NC	NC	$+V_{CC}$
8	OUTPUT B	OUTPUT B	NC	COMP C
9	$+V_{CC}$ (B) SEE NOTE 5	$+V_{CC}$ (B) SEE NOTE 5	COMP B / OFFSET NULL	---
10	COMP B	OUTPUT COMP B	OUTPUT	---
11	OFFSET NULL / COMP B	INPUT COMP B	$+V_{CC}$	---
12	-INPUT B	-INPUT B	COMP C	---
13	+INPUT B	+INPUT B	NC	---
14	OFFSET NULL A	NC	NC	---
15	NC	NC	---	---
16	OUTPUT A	OUTPUT A	---	---

NC = No connection

FIGURE 1. Terminal connections – Continued.

Device types	07	08
Case outlines	H	G and P
Terminal number	Terminal symbol	
1	NC	OUTPUT A
2	COMP A / OFFSET NULL	-INPUT A
3	-INPUT	+INPUT A
4	+INPUT	$-V_{CC}$
5	$-V_{CC}$	+INPUT B
6	COMP B / OFFSET NULL	-INPUT B
7	OUTPUT	OUTPUT B
8	$+V_{CC}$	$+V_{CC}$
9	COMP C	---
10	NC	---

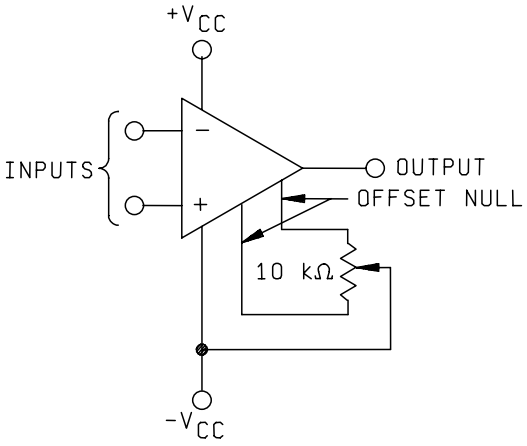
NC = No connection

NOTES:

1. $-V_{CC}$ shall be connected to case of metal packages.
2. For device type 02 only, $+V_{CC}$ (A) and $+V_{CC}$ (B) shall be internally connected.
3. +Input is non-inverting input.
4. -Input is inverting input.
5. For device types 05 and 06 only, $+V_{CC}$ (A) and $+V_{CC}$ (B) shall not be internally connected. (External connection to the same supply voltage recommended).

FIGURE 1. Terminal connections – Continued.

DEVICE TYPES 01 AND 02



DEVICE TYPES 03 AND 05

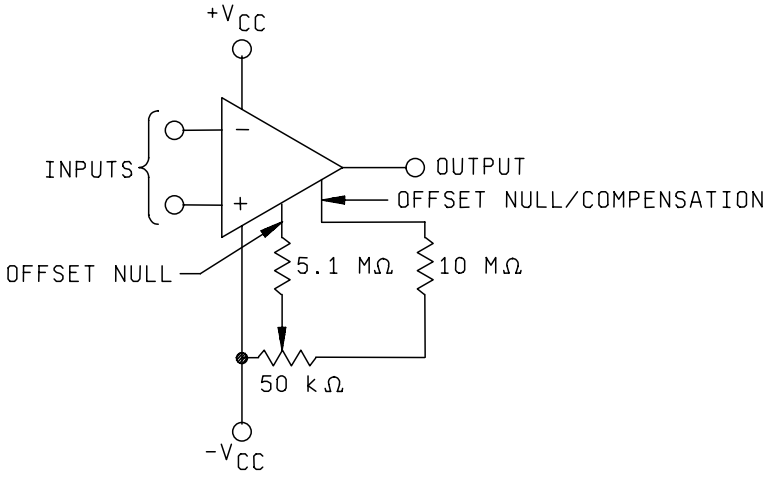


FIGURE 2. Offset null circuits.

Device type 07

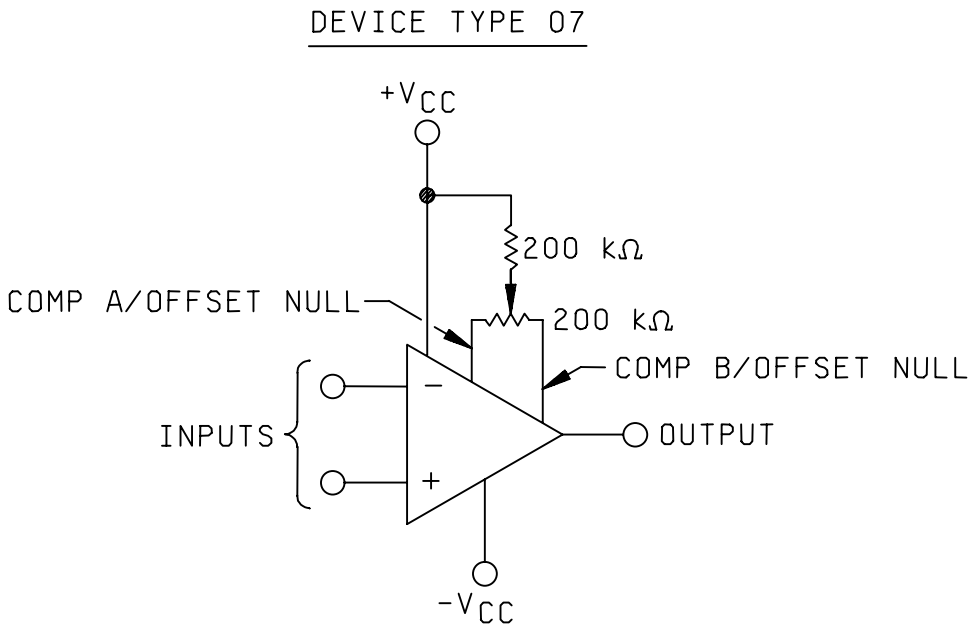


FIGURE 2. Offset null circuits - Continued.

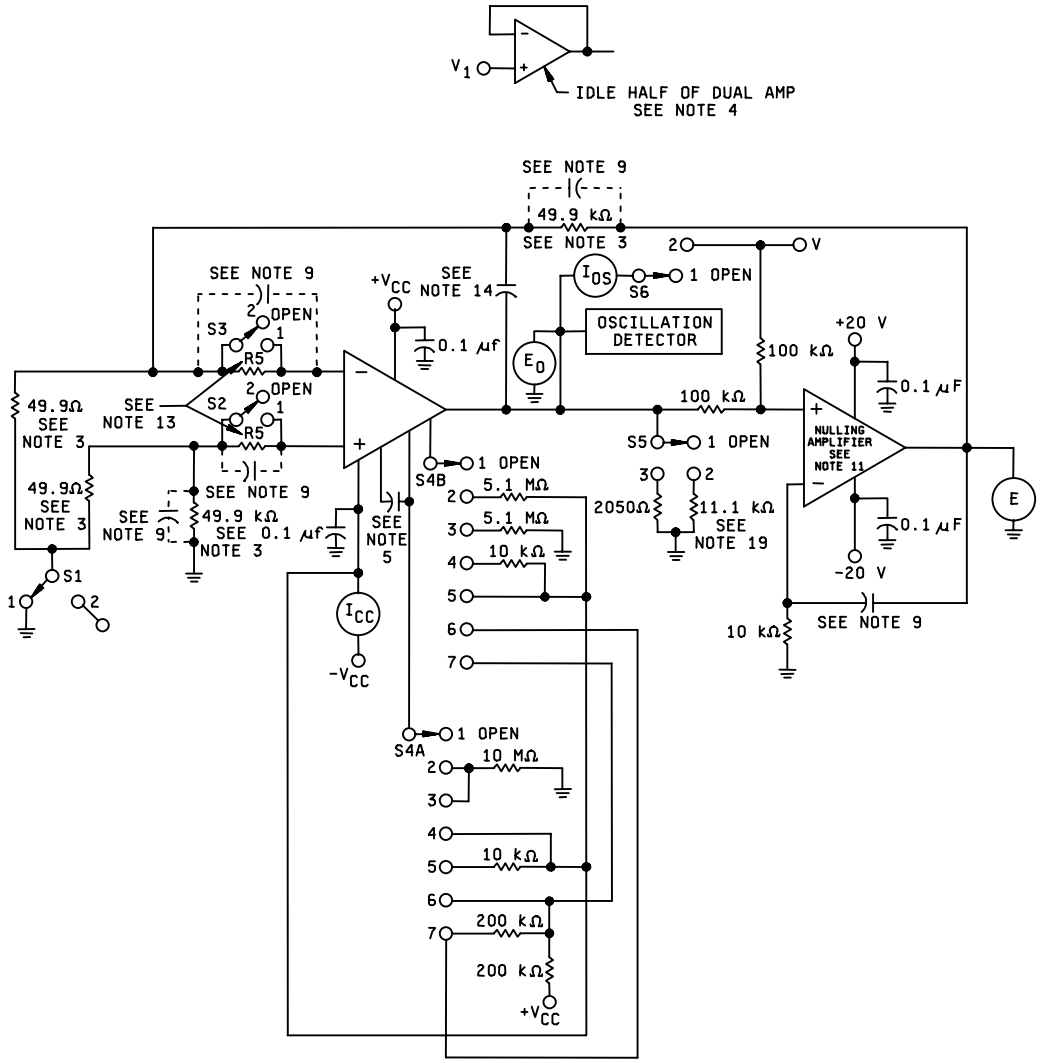


FIGURE 3. Test circuit for static and dynamic tests.

FIGURE 3. Test circuit for static and dynamic tests- Continued.

Parameter	Apply (in volts)			Switch position						Measure		Measured parameter 20/	Units
	$+V_{CC}$	$-V_{CC}$	V	S_1	S_2	S_3	S_4	S_5	S_6	Value	Units	Equation	
V_{IO}	35 5 20 5	-5 -35 -20 -5	-15 15 0 0	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	E1 E2 E3 E4	V	V_{IO} = E1, E2, E3, E4	mV
I_{IO}	35 5 20 5	-5 -35 -20 -5	-15 15 0 0	1 1 1 1	2 2 2 2	2 2 2 2	1 1 1 1	1 1 1 1	1 1 1 1	E5 E6 E7 E8	V	I_{IO} = ((E1 - E5) X 10^6) / R_S, ((E2 - E6) X 10^6) / R_S, 13/ ((E3 - E7) X 10^6) / R_S, ((E4 - E8) X 10^6) / R_S	nA
$+I_{IB}$	35 5 20 5	-5 -35 -20 -5	-15 15 0 0	1 1 1 1	2 2 2 2	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	E9 E10 E11 E12	V	$+I_{IB}$ = ((E1 - E9) X 10^6) / R_S, ((E2 – E10) X 10^6) / R_S, 13/ ((E3 - E11) X 10^6) / R_S, ((E4 - E12) X 10^6) / R_S	nA
$-I_{IB}$	35 5 20 5	-5 -35 -20 -5	-15 15 0 0	1 1 1 1	1 1 1 1	2 2 2 2	1 1 1 1	1 1 1 1	1 1 1 1	E13 E14 E15 E16	V	$-I_{IB}$ = ((E13 - E1) X 10^6) / R_S, ((E14 - E2) X 10^6) / R_S, 13/ ((E15 - E31) X 10^6) / R_S, ((E16 - E4) X 10^6) / R_S	nA
+PSRR	10	-20	5	1	1	1	1	1	1	E18 1/	V	+PSRR = (E3 - E18) X 10^2	µV/V
-PSRR	20	-10	-5	1	1	1	1	1	1	E19 1/	V	-PSRR = (E3 - E19) X 10^2	µV/V
CMR	35 5	-5 -35	-15 +15	1 1	1 1	1 1	1 1	1 1	1 1	E1 1/ E2 1/	V V	CMR = 20 LOG |(30 X 10^3) / (E1 - E2)|	dB
V_{IO} 7/ ADJ(+)	20	-20	0	1	1	1	2	1	1	E20	V	V_{IO} ADJ (+) = (E3 - E20)	mV
V_{IO} 7/ ADJ(-)	20	-20	0	1	1	1	3	1	1	E21	V	V_{IO} ADJ (-) = (E3 - E21)	mV
V_{IO} 6/ ADJ(+)	20	-20	0	1	1	1	4	1	1	E22	V	V_{IO} ADJ (+) = (E3 - E22)	mV
V_{IO} 6/ ADJ(-)	20	-20	0	1	1	1	5	1	1	E23	V	V_{IO} ADJ (-) = (E3 - E23)	mV
V_{IO} 15/ ADJ(+)	20	-20	0	1	1	1	6	1	1	E34	V	V_{IO} ADJ (+) = (E3 - E34)	mV
V_{IO} 15/ ADJ(-)	20	-20	0	1	1	1	7	1	1	E35	V	V_{IO} ADJ (-) = (E3 - E35)	mV

Parameter	Apply (in volts)			Switch position						Measure		Measured parameter 20/	Units
	+VCC	-VCC	V	S1	S2	S3	S4	S5	S6	Value	Units	Equation	
$+I_{OS}$ (output)	15	-15	-15	1	1	1	1	1	2	I_{OS1}	mA	$+I_{OS} = -IOS1$	mA
$-I_{OS}$ (output)	15	-15	+15	1	1	1	1	1	2	I_{OS2}	mA	$-I_{OS} = IOS2$	mA
I_{CC}	15	-15	0	1	1	1	1	1	1	I_{CC}	mA	$I_{CC} = I_{CC}$	mA
$+V_{OP}$ R_L = 10 kΩ	20	-20	-20	1	1	1	1	2	1	(E0)1	V	$+V_{OP} = (E0)1$	V
$-V_{OP}$ R_L = 10 kΩ	20	-20	+20	1	1	1	1	2	1	(E0)2	V	$-V_{OP} = (E0)2$	V
$+V_{OP}$ R_L = 2 kΩ	20	-20	-20	1	1	1	1	3	1	(E0)3	V	$+V_{OP} = (E0)3$	V
$-V_{OP}$ R_L = 2 kΩ	20	-20	+20	1	1	1	1	3	1	(E0)4	V	$-V_{OP} = (E0)4$	V
$+A_{VS}$ 16/ R_L = 2 kΩ	20	-20	-15	1	1	1	1	3	1	E24	V	$+A_{VS} = 15 / (E3 - E24)$	V/mV
$-A_{VS}$ 16/ R_L = 2 kΩ	20	-20	+15	1	1	1	1	3	1	E25	V	$-A_{VS} = 15 / (E25 - E3)$	V/mV
A_{VS} 16/ R_L = 2 kΩ	5 5	-5 -5	-2 +2	1 1	1 1	1 1	1 1	3 3	1 1	E26 E27	V	$A_{VS} = 4 / (E27 - E26)$	V/mV
$+A_{VS}$ 16/ R_L = 10 kΩ	20	-20	-15	1	1	1	1	2	1	E30	V	$+A_{VS} = 15 / (E3 - E30)$	V/mV
$-A_{VS}$ 16/ R_L = 10 kΩ	20	-20	+15	1	1	1	1	2	1	E31	V	$-A_{VS} = 15 / (E31 - E3)$	V/mV
A_{VS} 16/ R_L = 10 kΩ	5 5	-5 -5	-2 +2	1 1	1 1	1 1	1 1	2 2	1 1	E32 E33	V	$A_{VS} = 4 / (E33 - E32)$	V/mV
CMR 3/	20 20	-20 -20	+15 -15	2 2	1 1	1 1	1 1	1 1	1 1	E28 1/ E29 1/	V	CMR = 20 log $\lvert(30 \times 10^3) / (E28 - E29)\rvert$	

FIGURE 3. Test circuit for static and dynamic tests- Continued.

NOTES:

1/ These voltages in mV shall be measured to four place accuracy to provide required resolution in PSRR and CMR.

2/ Precautions shall be taken to prevent damage to the device under test during insertion into socket and change of switch positions (example, disable voltage supplies, current limit $\pm V_{CC}$, etc.).

3/ If this alternate CMR test is used, these resistors shall be of .01 percent tolerances matched to .001 percent.

4/ Device types 02, 05, and 06 only, test both halves for all tests. The idle half of the dual amplifiers shall be maintained in this configuration where V1 is midway between $+V_{CC}$ and $-V_{CC}$, or the manufacturer has the option to connect the idle half in a V_{IO} configuration such that the inputs are maintained at the same common mode voltage as the device under test.

5/ Compensation: for device types 03, 04, 05, and 06 only, equals 30 pF; for device type 07 only, equals 330 pF (optional).

6/ Device types 01, all case types, and device type 02, case outlines A, B, C, and D only.

7/ Device types 03 and 05 only.

8/ See figure 6. Noise test circuit.

9/ As required, if needed to prevent oscillation. Also, proper wiring procedures shall be followed to prevent oscillation. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least five loop time constants before the value is measured.

10/ Adequate settling time shall be allowed such that each parameter has settled to within five percent of its final value.

11/ The nulling amplifier is an M38510/10101XXX. Saturation of the nulling amplifier is not allowed on test where the "E" value is measured.

12/ All resistors 0.1 percent tolerance except as noted (note 3).

13/ For device types 01, 02, 07, and 08: R_S = 20 kΩ. For device types 03 and 05: R_S = 100 kΩ. For device types 04 and 06: R_S = 5.0 MΩ.

14/ Device type 07 only, this capacitor = 1,000 pF maximum to prevent oscillations.

15/ Device type 07 only.

16/ To minimize thermal drift, the reference voltages for gain measurements (E3 and E4) shall be taken immediately prior to or after the reading corresponding to device gain (E24, E25, E26, E27, E30, E31, E32, and E33). The gain at R_L = 10 kΩ is essentially the gain at R_L = 2 kΩ is influenced by thermal gradients on the die resulting from power dissipation in the output stage. Hence, it is not linear and may not even be a true approximation of the gain between other than the specified operation points.

17/ Any oscillation greater that 300 mV in amplitude (pk - pk) shall be cause for device failure.

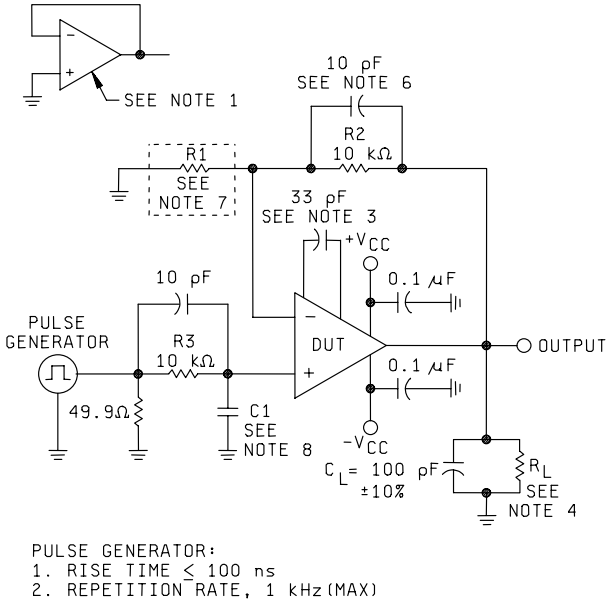
18/ Although switches are depicted as toggle switches, any switching mechanism may be used provided the switching action is achieved without adversely affecting the measurement.

19/ The load resistors (2,050 Ω and 11.1 kΩ) yield effective load resistances of 2 kΩ and 10 kΩ, respectively.

20/ The equations take into account both the loop gain of 1,000 and the scale factor multiplier, so that the calculated value is in table III units. Therefore, use measured value / units in the equations, example E1 (volts).

FIGURE 3. Test circuit for static and dynamic tests- Continued.

DEVICE TYPES 01,02,03,04,05,06, AND 08



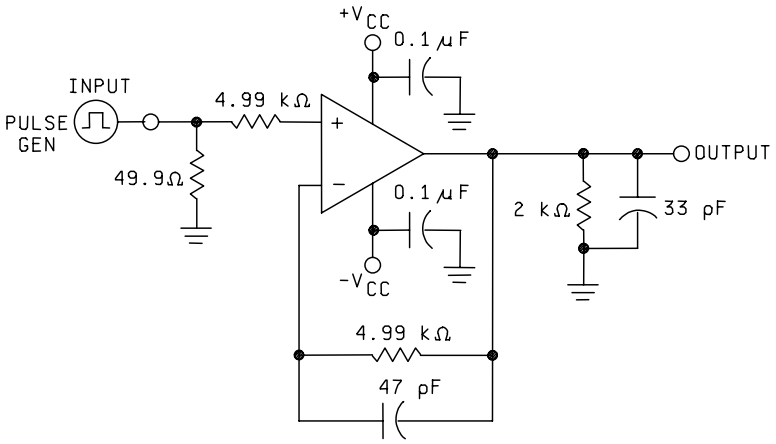
PULSE GENERATOR:
1. RISE TIME ≤ 100 ns
2. REPETITION RATE, 1 kHz(MAX)

See notes on page 29

Parameter	Pulse generator	Measure	Equation	Units
Rise time (tr) A_V = 1	+50 mV amplitude	t (µs), see waveform 1	$t_r = t$	µs
Overshoot (OS) A_V = 1	+50 mV amplitude	ΔV (mV), see waveform 1	OS = (ΔV / 50) x 100	%
Bandwidth (BW) A_V = 1	+50 mV amplitude	Calculate	BW = 0.35 / tr (µs)	MHz
Slew rate (+SR) A_V = 1	-5 V to +5 V step	ΔV_O (volts), Δt (µs) see waveform 2	+SR = $\lvert\Delta V_O(+) / \Delta t(+)\rvert$	V/µs
Slew rate (-SR) A_V = 1	+5 V to -5 V step	ΔV_O (volts), Δt (µs) see waveform 3	-SR = $\lvert\Delta V_O(-) / \Delta t(-)\rvert$	V/µs

FIGURE 4. Transient response test circuit.

DEVICE TYPE 07

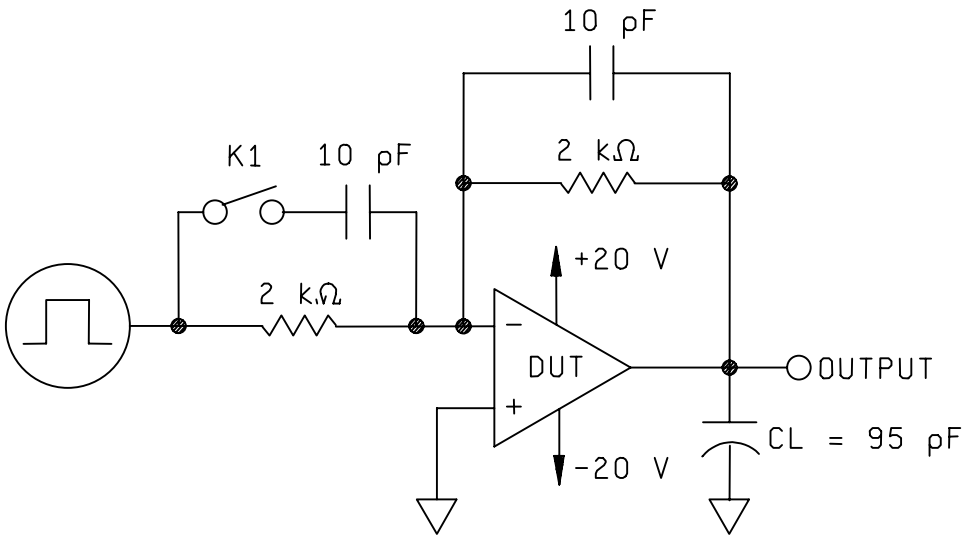


PULSE GENERATOR:
1. RISE TIME ≤ 10 ns
2. REPETITION RATE, 1 kHz(MAX)

See notes on page 30

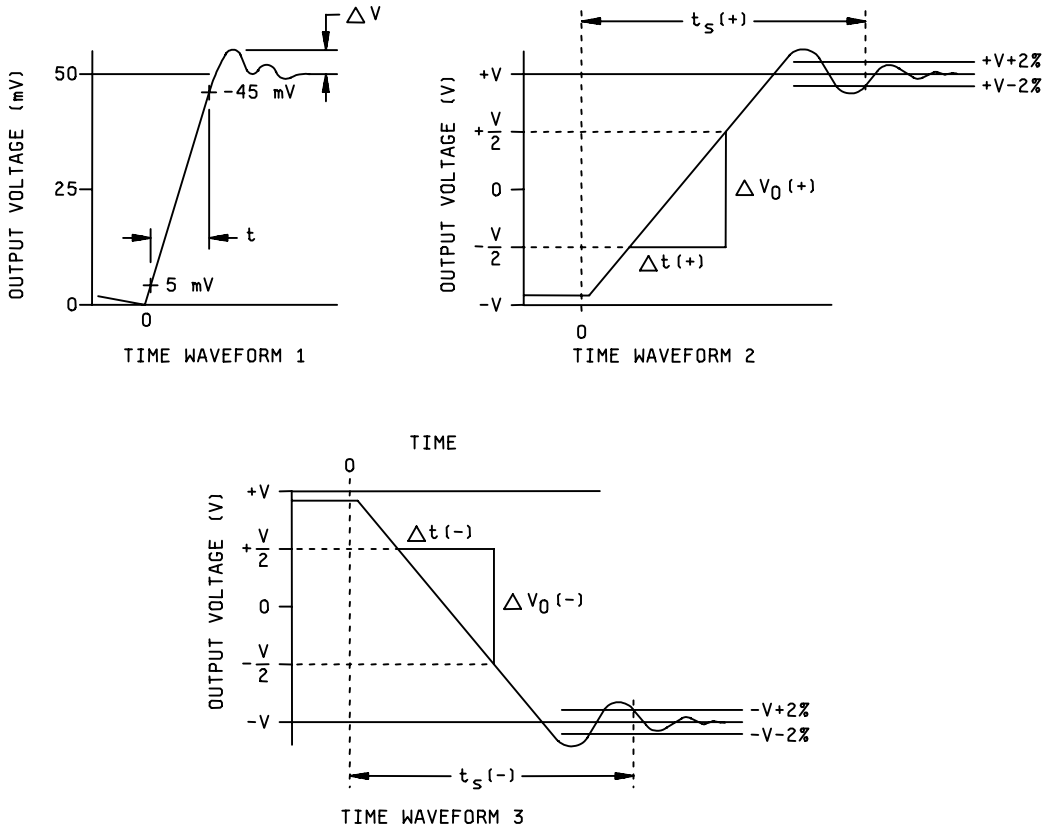
Parameter	Pulse generator	Measure	Equation	Units
Rise time (tr)	+50 mV amplitude	t (ns), see waveform 1	$t_r = t$	ns
Overshoot (OS)	+50 mV amplitude	ΔV (mV), see waveform 1	OS = (ΔV / 50) x 100	%
Bandwidth (BW)	+50 mV amplitude	Calculate	BW = (0.35 x 10^3) / tr (ns)	MHz
Slew rate (+SR)	-5 V to +5 V step	ΔV_O (+) (volts), Δt (+) (ns) see waveform 2	+SR = $\lvert \Delta V_O(+) / \Delta t(+) \times 10^{-3} \rvert$	V/µs
Slew rate (-SR)	+5 V to -5 V step	ΔV_O (-) (volts), Δt (-) (ns) see waveform 3	-SR = $\lvert \Delta V_O(-) / \Delta t(-) \times 10^{-3} \rvert$	V/µs
Settling time $t_S(+)$ 5/	-5 V to +5 V step	$t_S(+)$, see waveform 2	$t_S(+) = t_S(+)$	ns
Settling time $t_S(-)$ 5/	+5 V to -5 V step	$t_S(-)$, see waveform 3	$t_S(-) = t_S(-)$	ns

FIGURE 4. Transient response test circuit - Continued.



NOTES:
1. K1 is closed for small tests (Tr and P.O.) and is open for large signal tests (±slew rate, ±Ts).
2. Input signal is a -50 mV to 0 mV pulse train for small signal tests and -5 V to +5 V pulse train for large signal tests.
3. Tr of the input signal is < 10 ns for the small signal tests.

FIGURE 4. Transient response test circuit - Continued.

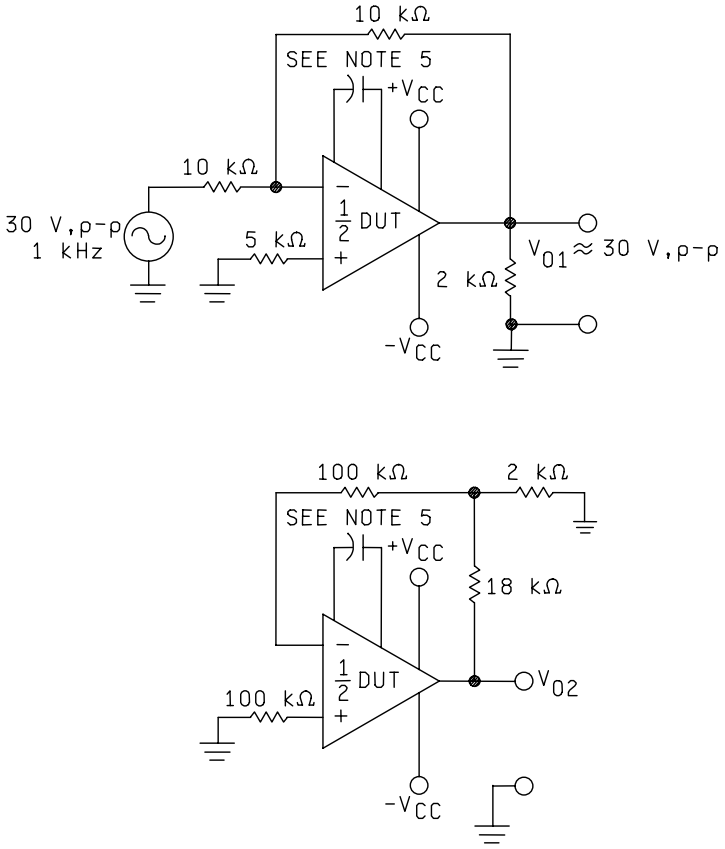


NOTES:

1. Idle half of dual amplifier shall be connected during test of other half.
2. All resistor tolerances are 1 percent, capacitor tolerances are 10 percent and $\pm V_{CC} = \pm 20$ V.
3. This compensation capacitor is used for device types 03, 04, 05, and 06.
4. For device types 01, 02, 03, 05, and 08, $R_L = 2$ kΩ; for device types 04 and 06, $R_L = 10$ kΩ.
5. Settling time is the interval from the beginning of the output response to the point where the output remains within the error band, in this case ±2 percent.
6. CF = 10 pF ±10 percent includes stray capacitance.
7. R1 may be added to the circuit. When R1 is added, its value shall be 10 kΩ. When using R1, the unity gain will increase to 2. To accommodate this change in gain, the pulse generator input shall be halved.
8. C1 may be added to the circuit. When added, it shall be within the range of 0 pF to 2 pF.
9. C_L capacitance specified includes stray, jig, and probe capacitance.

FIGURE 4. Transient response test circuit - Continued.

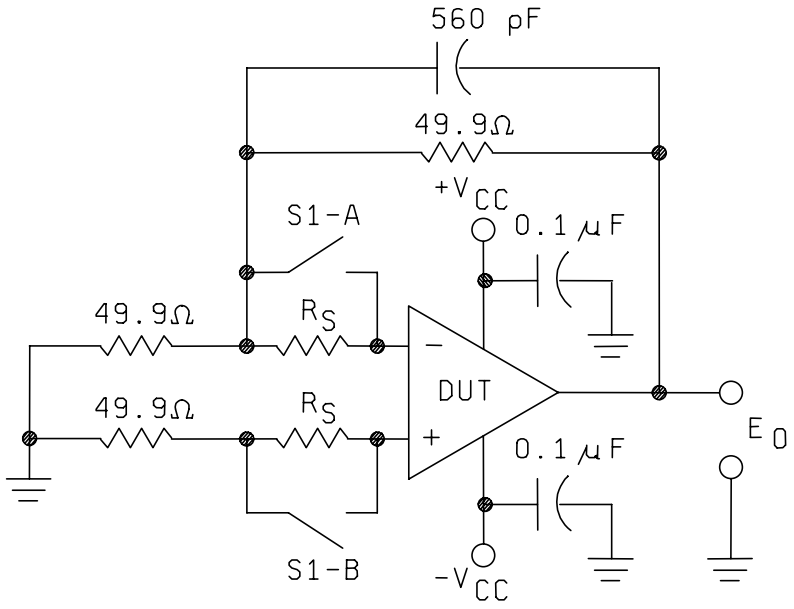
Device types 02, 05, 06, and 08 only.



NOTES:

1. $\pm V_{CC}$ = 20 V.
2. Measure: V_{02} (volts, p-p) at 1 kHz to accuracy of 0.1 mV or better.
3. Channel separation (dB) referred to input of second channel = 20 log [V_{01} / (0.1 x V_{02})].
4. All resistor tolerances ≤ 1 percent.
5. A 30 pF compensation capacitor is required for device types 05 and 06.

FIGURE 5. Test circuit for channel separation.



Noise (Referred to input)	Symbol	S1	Measure		Measured equation	Parameter units
			Value	Units		
Broadband	N_1(BB)	Closed	E_0	mV rms	E_0 / 1000	µV rms
Popcorn	N_1(PC)	Open	E_0	mV pk	E_0 / 1000	µV pk

NOTES:

1. R_S = 20 kΩ for device types 01, 02, 07, and 08; R_S = 100 kΩ for device types 03, 04, 05, and 06.
2. E_0 is measured using an RMS voltmeter with a bandwidth of 10 Hz to 5 kHz and a peak detector simultaneously. Monitor the peak test for a minimum of 15 seconds. The loop bandwidth shall be at least 5 kHz.

FIGURE 6. Noise test circuit.

TABLE III. Group A inspection.

Subgroup	Symbol	MIL-STD -883 method	Test no.	Conditions $\pm V_{CC}$ = ±20 V dc, figure 3 unless otherwise specified	01, 02, 08 1/ Limits		03, 05 1/ Limits		04, 06 1/ Limits		07 1/ Limits		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
1 T_A = +25°C	V_{IO}	4001	1	V_{CM} = -15 V 2/	-3.0	+3.0	-2.0	+2.0	-0.5	+0.5	-4.0	+4.0	mV
			2	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"
			3	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
			4	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
	I_{IO}		5	V_{CM} = -15 V 2/	-30	+30	-10	+10	-0.2	+0.2	-40	+40	nA
			6	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"
			7	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
			8	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
	$+I_{IB}$		9	V_{CM} = -15 V 2/	-0.1	110	-0.1	75	-0.1	+2.0	-0.1	250	nA
			10	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"
			11	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
			12	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
	$-I_{IB}$		13	V_{CM} = -15 V 2/	-0.1	110	-0.1	75	-0.1	+2.0	-0.1	250	nA
			14	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"
			15	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
			16	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"
	+PSRR	4003	17	$+V_{CC}$ = 10 V, $-V_{CC}$ = -20 V	-50	+50	-50	+50	-16	+16	-100	+100	µV/V
	-PSRR		18	$+V_{CC}$ = 20 V, $-V_{CC}$ = -10 V	-50	+50	-50	+50	-16	+16	-100	+100	µV/V
	CMR		19	V_{CM} = +15 V	80		80		96		80		dB
	V_{IO} ADJ (+)		20	3/	+5		+4				+7		mV
	V_{IO} ADJ (-)		21	3/		-5		-4				-7	mV

TABLE III. Group A inspection - Continued.

* * * *

Subgroup	Symbol	MIL-STD -883 method	Test no.	Conditions $\pm V_{CC}$ = ±20 V dc, figure 3 unless otherwise specified	01, 02, 08 1/		03, 05 1/		04 1/		06 1/		07 1/		Unit
					Limits		Limits		Limits		Limits		Limits		
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1	I_{OS} (+) 4/	3011	22	$\pm V_{CC}$ = ±15 V, t ≤ 25 ms	-60		-60		-20		-20		-65		mA
T_A =	I_{OS} (-) 4/		23	$\pm V_{CC}$ = ±15 V, t ≤ 25 ms		+60		+60		+20		+20		+65	mA
+25°C	I_{CC}	4005	24	$\pm V_{CC}$ = ±15 V 5/		3.8		3.0		0.6		0.6		8	mA
2	V_{IO}	4001	25	V_{CM} = -15 V 2/	-4.0	+4.0	-3.0	+3.0	-1.0	+1.0	-1.0	+1.0	-6.0	+6.0	mV
T_A =			26	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"
+125°C			27	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
			28	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
	ΔV_{IO} / ΔT 6/		29	ΔV_{IO} / ΔT = [V_{IO} (test 27) - V_{IO} (test 3)] x 10	-15	+15	-15	+15	-5.0	+5.0	-5.0	+5.0	-50	+50	µV/°C
	I_{IO}		30	V_{CM} = -15 V 2/	-30	+30	-10	+10	-0.4	+0.4	-0.4	+0.4	-80	+80	nA
			31	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"
			32	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
			33	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
	ΔI_{IO} / ΔT		34	ΔI_{IO} / ΔT = [I_{IO} (test 32) - I_{IO} (test 7)] x 10	-200	+200	-100	+100	-2.5	+2.5	-2.5	+2.5	-1,000	+1,000	pA/°C
	$+I_{IB}$		35	V_{CM} = -15 V 2/	-0.1	110	-0.1	75	-1.0	+2.0	-1.0	+2.0	-0.1	250	nA
			36	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"
			37	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
			38	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
	$-I_{IB}$		39	V_{CM} = -15 V 2/	-0.1	110	-0.1	75	-1.0	+2.0	-1.0	+2.0	-0.1	250	nA
			40	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"
			41	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
			42	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"

See footnotes at end of table III.

TABLE III. Group A inspection - Continued.

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Subgroup	Symbol	MIL-STD -883 method	Test no.	Conditions $\pm V_{CC}$ = ±20 V dc, figure 3 unless otherwise specified	01, 02 1/ Limits		03, 05 1/ Limits		04 1/ Limits		06 1/ Limits		07 1/ Limits		08 1/ Limits		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
2	I_{OS} (+) 4/	3011	43	$\pm V_{CC}$ = ±15 V, t ≤ 25 ms	-60		-60		-20		-20		-65		-60		mA
T_A =	I_{OS} (-) 4/		44	$\pm V_{CC}$ = ±15 V, t ≤ 25 ms		+60		+60		+20		+20		+65		+60	mA
+125°C	I_{CC}	4005	45	$\pm V_{CC}$ = ±15 V		3.4		2.5		0.6		0.6		7		3.4	mA
	+PSRR	4003	46	$+V_{CC}$ = 10 V, $-V_{CC}$ = -20 V	-100	+100	-100	+100	-16	+16	-16	+16	-150	+150	-100	+100"	µV /V
	-PSRR		47	$+V_{CC}$ = 20 V, $-V_{CC}$ = -10 V	"	"	"	"	"	"	"	"	"	"	"		
	CMR	4003	48	V_{CM} = ±15 V	80		80		96		96		80		80		dB
	V_{IO} ADJ(+)		49	3/	+5		+4						+7		+5		mV
	V_{IO} ADJ(-)		50	3/		-5		-4						-7		-5	
3	V_{IO}	4001	51	V_{CM} = -15 V 2/	-4.0	+4.0	-3.0	+3.0	-1.0	+1.0	-1.0	+1.0	-6.0	+6.0	-4.0	+4.0	mV
T_A =			52	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"	"	"
-55°C			53	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"	"	"
			54	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"	"	"
	ΔV_{IO} / ΔT 6/		55	ΔV_{IO} / ΔT = [V_{IO} (test 3) - V_{IO} (test 53)] x 12.5	-15	+15	-18	+18	-5.0	+5.0	-5.0	+5.0	-50	+50	-20	+20	µV /°C
	I_{IO}		56	V_{CM} = -15 V 2/	-70	+70	-20	+20	-0.4	+0.4	-0.4	+0.4	-80	+80	-70	+70	nA
			57	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"	"	"
			58	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"	"	"
			59	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"	"	
	ΔI_{IO} / ΔT 6/		60	ΔI_{IO} / ΔT = [I_{IO} (test 7) - I_{IO} (test 58)] x 12.5	-500	+500	-200	+200	-2.5	+2.5	-2.5	+2.5	-1,000	+1,000	-500	+500	pA/°C

See footnotes at end of table III.

TABLE III. Group A inspection - Continued.

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Subgroup	Symbol	MIL-STD -883 method	Test no.	Conditions $\pm V_{CC}$ = ±20 V dc, figure 3 unless otherwise specified	01, 02, 08 1/		03, 05 1/		04 1/		06 1/		07 1/		Unit
					Limits		Limits		Limits		Limits		Limits		
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3	$+I_{IB}$	4001	61	V_{CM} = -15 V 2/	-0.1	265	-0.1	100	-0.1	3.0	-0.1	3.0	-0.1	400	nA
T_A =			62	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"
-55°C			63	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
			64	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
	$-I_{IB}$		65	V_{CM} = -15 V 2/	-0.1	265	-0.1	100	-0.1	3.0	-0.1	3.0	-0.1	400	nA
			66	V_{CM} = +15 V 2/	"	"	"	"	"	"	"	"	"	"	"
			67	V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
			68	$\pm V_{CC}$ = ±5 V, V_{CM} = 0 V	"	"	"	"	"	"	"	"	"	"	"
	I_{OS} (+) 4/	3011	69	$\pm V_{CC}$ = ±15 V, t ≤ 25 ms	-60		-60		-20		-20		-65		mA
	I_{OS} (-) 4/		70	$\pm V_{CC}$ = ±15 V, t ≤ 25 ms		+60		+60		+20		+20		80	mA
	I_{CC}	4005	71	$\pm V_{CC}$ = ±15 V 5/		4.2		3.5		0.8		0.8		9	mA
	+PSRR	4003	72	$+V_{CC}$ = 10 V, $-V_{CC}$ = -20 V	-100	+100	-100	+100	-16	+16	-16	+16	-150	+150	µV/V
	-PSRR		73	$+V_{CC}$ = 20 V, $-V_{CC}$ = -10 V	-100	+100	-100	+100	-16	+16	-16	+16	-150	+150	µV/V
	CMR		74	V_{CM} = ±15 V	80		80		96		96		80		dB
	V_{IO} ADJ(+)		75	3/	+5		+4						+7		mV
	V_{IO} ADJ(-)		76	3/		-5		-4						-7	mV
4	$+V_{OP}$	4004	77	R_L = 10 kΩ	+16		+16		+16		+16		+17		V
T_A =	$-V_{OP}$		78	R_L = 10 kΩ		-16		-16		-16		-16		-17	"
+25°C	$+V_{OP}$		79	R_L = 2 kΩ	+15		+15						+16		"
	$-V_{OP}$		80	R_L = 2 kΩ		-15		-15						-16	"

See footnotes at end of table III.

TABLE III. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD -883 method	Test no.	Conditions: ±VCC = ±20 V dc, figure 3 unless otherwise specified	01, 02, 08 1/ Limits Min	01, 02, 08 1/ Limits Max	03, 05 1/ Limits Min	03, 05 1/ Limits Max	04, 06 1/ Limits Min	04, 06 1/ Limits Max	07 1/ Limits Min	07 1/ Limits Max	Unit
4 TA = +25°C	+AVS	4004	81	RL = 2 kΩ, VOUT = +15 V	50		50				50		V/mV
	-AVS		82	RL = 2 kΩ, VOUT = -15 V	50		50				50		"
	+AVS		83	RL = 10 kΩ, VOUT = +15 V	50		50		80		50		"
	-AVS		84	RL = 10 kΩ, VOUT = -15 V	50		50		80		50		"
	AVS		85	RL = 2 kΩ, ±VCC = ±5 V, VOUT = ±2 V	10		10				10		"
	AVS		86	RL = 10 kΩ, ±VCC = ±5 V, VOUT = ±2 V	10		10		20		10		"
5 TA = +125°C	+VOP		87	RL = 10 kΩ	+16		+16		+16		+17		V
	-VOP		88	RL = 10 kΩ		-16		-16		-16		-17	"
	+VOP		89	RL = 2 kΩ	+15		+15				+16		"
	-VOP		90	RL = 2 kΩ		-15		-15				-16	"
	+AVS		91	RL = 2 kΩ, VOUT = +15 V	25		25				32		V/mV
	-AVS		92	RL = 2 kΩ, VOUT = -15 V	25		25				32		"
	+AVS		93	RL = 10 kΩ, VOUT = +15 V	25		25		40		32		"
	-AVS		94	RL = 10 kΩ, VOUT = -15 V	25		25		40		32		"
	AVS		95	RL = 2 kΩ, ±VCC = ±5 V, VOUT = ±2 V	10		10				10		"
	AVS		96	RL = 10 kΩ, ±VCC = ±5 V, VOUT = ±2 V	10		10		20		10		"
6 TA = -55°C	+VOP		97	RL = 10 kΩ	+16		+16		+16		+17		V
	-VOP		98	RL = 10 kΩ		-16		-16		-16		-17	"
	+VOP		99	RL = 2 kΩ	+15		+15				+16		"
	-VOP		100	RL = 2 kΩ		-15		-15				-16	"

See footnotes at end of table III.

TABLE III. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD -883 method	Test no.	Conditions $\pm V_{CC}$ = ±20 V dc, figure 3 unless otherwise specified	01, 02, 08 1/		03, 05 1/		04, 06 1/		07 1/		Unit
					Limits		Limits		Limits		Limits		
					Min	Max	Min	Max	Min	Max	Min	Max	
6	$+A_{VS}$		101	R_L = 2 kΩ, V_{OUT} = +15 V	25		25				32		V/mV
T_A =	$-A_{VS}$		102	R_L = 2 kΩ, V_{OUT} = -15 V	25		25				32		"
-55°C	$+A_{VS}$		103	R_L = 10 kΩ, V_{OUT} = +15 V	25		25		40		32		"
	$-A_{VS}$		104	R_L = 10 kΩ, V_{OUT} = -15 V	25		25		40		32		"
	A_{VS}		105	R_L = 2 kΩ, $\pm V_{CC}$ = ±5 V, V_{OUT} = ±2 V	10		10				10		"
	A_{VS}		106	R_L = 10 kΩ, $\pm V_{CC}$ = ±5 V, V_{OUT} = ±2 V	10		10		20		10		"
7	$TR(t_r)$		107	Figure 4		800		800		1,000		40	ns
T_A =	TR(OS)		108	Figure 4		25		25		50		50	%
+25°C	SR(+)	4002	109	Figure 4, A_V = 1, V_{IN} = -5 V to +5 V	0.3		0.3		0.05		40		V/µs
	SR(-)		110	Figure 4, A_V = 1, V_{IN} = +5 V to -5 V	0.3		0.3		0.05		40		V/µs
	CS 7/		111	Figure 5	80		80		80				dB
	$NI_{(BB)}$		112	BW = 5 kHz, figure 6		15		15		15		25	µV rms
	$NI_{(PC)}$		113	BW = 5 kHz, figure 6		40		80		40		80	µV pk
8A	$TR(t_r)$		114	T_A = +125°C, figure 4		800		800		1,000		40	ns
T_A =	TR(OS)		115	T_A = +125°C, figure 4		25		25		50		50	%
+125°C	SR(+)	4002	116	T_A = +125°C, figure 4, A_V = 1, V_{IN} = -5 V to +5 V	0.3		0.3		0.05		30		V/µs
	SR(-)		117	T_A = +125°C, figure 4, A_V = 1, V_{IN} = +5 V to -5 V	0.3		0.3		0.05		30		V/µs
8B	$TR(t_r)$		118	T_A = -55°C, figure 4		800		800		1,000		40	ns
T_A =	TR(OS)		119	T_A = -55°C, figure 4		25		25		50		50	%
-55°C	SR(+)	4002	120	T_A = -55°C, figure 4, A_V = 1, V_{IN} = -5 V to +5 V	0.3		0.2		0.05		40		V/µs
	SR(-)		121	T_A = -55°C, figure 4, A_V = 1, V_{IN} = +5 V to -5 V	0.3		0.2		0.05		40		V/µs

See footnotes at end of table III.

TABLE III. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD -883 method	Test no.	Conditions $\pm V_{CC}$ = ±20 V dc, figure 3 unless otherwise specified	01, 02, 08 1/ Limits		03, 05 1/ Limits		04, 06 1/ Limits		07 1/ Limits		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
12	$t_{S(+)}$	4002	122	T_A = +25°C, figure 4								800	ns
T_A =+25°C	$t_{S(-)}$		123	T_A = +25°C, figure 4								800	ns
13A	$t_{S(+)}$		124	T_A = +125°C, figure 4								1,200	ns
T_A =+125°C	$t_{S(-)}$		125	T_A = +125°C, figure 4								1,200	ns
13B	$t_{S(+)}$		126	T_A = -55°C, figure 4								1,200	ns
T_A =-55°C	$t_{S(-)}$		127	T_A = -55°C, figure 4								1,200	ns

1/ For devices marked with the "Q" certification mark, the parameters listed herein may be guaranteed if not tested to the limits specified herein in accordance with the manufacturer's QM plan. Limits apply to both halves of dual devices (02, 05, 06, and 08) independently, and slew rate limit for device 08 is 0.4 V/µs at all temperatures (tests 109, 110, 116, 117, 120, 121).

2/ V_{CM} is achieved by algebraically subtracting the common mode voltage from each supply and algebraically adding the common mode voltage to V (example, for V_{CM} = -15 V, $+V_{CC}$ = +35 V, $-V_{CC}$ = -5 V, V = -15 V).

3/ V_{IO} (ADJ) is not performed on device type 02, case I only, or on device types 04, 06, and 08 all case types.

4/ Due to the significant power dissipation and associated device heating, these tests shall always be the last tests performed in any given sequence, followed by operational verification (example, such tests as V_{OPP}, A_{VS}, TR, SR).

5/ Limit shown applied to single devices (01, 03, and 04) only. The maximum quiescent I_{CC} for dual devices (02, 05, 06, and 08) is twice that shown for single devices.

6/ Tests 29, 34, 55, and 60 which require a read and record measurement plus a calculation, may be omitted except when subgroups 2 and 3 are being accomplished for group A sampling inspection and group C and D endpoint measurements.

7/ Applies to device types 02, 05, and 06 only.

TABLE IV. Group C end point electrical parameters.

(T_A = +25°C, V_{CC} = ±20 V, V_{CM} = 0 V)

Table III test no.	Test	01, 02, 08				03, 05				Unit
		Limit		Delta		Limit		Delta		
		Min	Max	Min	Max	Min	Max	Min	Max	
3	V_{IO}	-3.0	+3.0	-0.5	+0.5	-2.0	+2.0	-0.5	+0.5	mV
11	$+I_{IB}$	+1.0	+110	-12	+12	+1.0	+75	-7.5	+7.5	nA
15	$-I_{IB}$	+1.0	+110	-12	+12	+1.0	+75	-7.5	+7.5	nA

Table III test no.	Test	04, 06				07				Unit
		Limit		Delta		Limit		Delta		
		Min	Max	Min	Max	Min	Max	Min	Max	
3	V_{IO}	-0.5	+0.5	-0.25	+0.25	-4.0	+4.0	-1.0	+1.0	mV
11	$+I_{IB}$	-0.1	+2.0	-0.5	+0.5	+1.0	250	-25	+25	nA
15	$-I_{IB}$	-0.1	+2.0	-0.5	+0.5	+1.0	250	-25	+25	nA

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Subgroups 9, 10, and 11 shall be omitted.

b. Tests shall be as specified in table II herein.

c. Subgroups 12 and 13 (for device type 07 only) shall be added to table III of MIL-PRF-38535 for class S only. The class S sample size series for subgroup 12 shall be 5 and for subgroup 13 the class S sample size series shall be 7.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. Subgroups shall be added to group C inspection and shall consist of subgroups 8, 12, and 13 respectively as specified in table III herein. The sample size series for subgroup 12 shall be 5, and subgroup 13 shall be 7 for class B devices (see MIL-PRF-38535, Appendix D).

c. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cooldown procedure. When devices are measured at +25°C following application of the steady state life or burn-in condition, they shall be cooled to within 10°C of their power stable condition at room temperature prior to removal of the bias.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to acquiring activity in addition to notification of the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirements for “JAN” marking.

j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired to Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	741A
02	747A (with common $+V_{CC}$)
03	LM101A
04	LM108A
05	LH2101A
06	LH2108A
07	LM118
08	1558

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army – MI, SM
Navy - AS, CG, MC, SH, TD
Air Force – 03, 19, 99

Preparing activity:
DLA - CC

Project 5962-2005-046

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.