REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Convert to military drawing format. Add vendor CAGE number 50088 to drawing. Changed code identification number to 67268.	87-11-12	R. P. Evans
E	Add vendor CAGE code 3V146. Update boilerplate to MIL-PRF-38535 requirements. Add QD device type criteria. - LTG	03-08-26	Thomas M. Hess
F	Correct marking requirements in 3.5. Update boilerplate in accordance with MIL-PRF-38535 requirements. Editorial change throughout. - PHN	05-02-17	Thomas M. Hess
G	Correct terminal names for terminal number 17 and 18 in case outline Z. - PHN	06-08-16	Thomas M. Hess

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			G	E	F	F	E	E	E	F	G	F	F	F	F	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY

James E. Jamison

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

D. A. Di Cenzo

APPROVED BY

Robert P. Evans

DRAWING APPROVAL DATE

79-03-14

REVISION LEVEL

G

MICROCIRCUIT, DIGITAL, BIPOLAR, MICROPROGRAM CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**78017**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

78017	01	Q	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2910	Microprogram controller
02	2910A	Microprogram controller

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
Z	See figure 2	42	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage to ground potential ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -0.5 V dc to +5.5 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) 1/ ..... 1.9 W
Thermal resistance, junction-to-case (θ_{JC}):
Case Q ..... See MIL-STD-1835
Case Z ..... 25°C/W
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature (T_J) ..... +200°C
Output current, into outputs ..... 30 mA dc
Input current ..... -30 mA dc to +5.0 mA dc

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 4.5 V dc minimum to 5.5 V dc maximum

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Switching and timing waveforms. The switching and timing waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the “Q” or “QML” certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.6 mA V_{IN} = V_{IH} or V_{IL}		All	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	Y_{0-11}, I_{OL} = 12 mA	All	1, 2, 3		0.5	V
			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$, I_{OL} = 8 mA	All				
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		All	1, 2, 3		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.5 V	D_{0-11}	All	1, 2, 3		-0.87	mA
			CI, $\overline{CCEN}$	All			-0.54	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$	All			-0.72	
			$\overline{CC}$	All			-1.31	
			CP	All			-2.14	
High level input current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 2.7 V	D_{0-11}	All	1, 2, 3		80	µA
			CI, $\overline{CCEN}$	All			30	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$	All			40	
			$\overline{CC}$	All			50	
			CP	All			100	
Input current at maximum input voltage	I_I	V_{CC} = 5.5 V, V_{IN} = 5.5 V		All	1, 2, 3		1.0	mA
Output short circuit current 2/	I_{OS}	V_{CC} = 5.5 V		All	1, 2, 3	-30	-85	mA
Off-state output current, low level voltage applied	I_{OZL}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V $\overline{OE}$ = 2.4 V		All	1, 2, 3		-50	µA
Off-state output current, high level voltage applied	I_{OZH}	V_{CC} = 5.5 V, $\overline{OE}$ = V_{OUT} = 2.4 V		All	1, 2, 3		50	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	T_C = +25°C	All	1, 2, 3		340	mA
			T_C = -55°C	All			340	
			T_C = +125°C	All			280	
Functional test		See 4.3.1c		All	7, 8			
Direct input to register/ counter setup time	t_{DR}	C_L = pF 3/		01	9, 10, 11		28	ns
				02			16	
Direct input to microprogram address counter setup time	t_{DPC}			01	9, 10, 11		62	ns
				02			30	
Instruction setup time	t_I			01	9, 10, 11		110	ns
				02			38	
Condition code setup time	$t_{\overline{CCI}}$			01	9, 10, 11		86	ns
				02			35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Condition code enable setup time	$t_{\overline{CCEN1}}$	C_L = 50 pF 3/		01	9, 10, 11		86	ns
				02			35	
Carry-in setup time	t_{CI}			01	9, 10, 11		58	ns
				02			18	
Register load to setup time	$t_{\overline{RLD}}$			01	9, 10, 11		42	ns
				02			20	
Direct input to address output	t_{DY}			All	9, 10, 11		25	ns
Instruction input to address output	t_{IY}			01	9, 10, 11		75	ns
				02			40	
Condition code to any output	$t_{\overline{CC2}}$			01	9, 10, 11		48	ns
				02			36	
Condition code enable to any output	$t_{\overline{CCEN2}}$			01	9, 10, 11		50	ns
				02			36	
Clock pulse to any output	t_{CP}		I = 8, 9, 15 4/	01	9, 10, 11		130 106	ns
				02			46	
			All other I	01			61	
				02			46	
Enable/disable input to any output 5/	t_{OE}		Enable	01	9, 10, 11		40	ns
				02			25	
			Disable	01			30	
				02			30	
Clock LOW time	t_{CLKL}	C_L = 50 pF 6/		01	9, 10, 11	58		ns
				02		25		
Clock HIGH time	t_{CLKH}	C_L = 50 pF 6/		01	9, 10, 11	42		ns
				02		25		
Instruction input to PL, VECT, MAP outputs	t_{IPVM}	C_L = 50 pF 3/		01	9, 10, 11		58	ns
				02			35	
Clock pulse to $\overline{FULL}$ for all instructions	t_{CPF}			01	9, 10, 11		67	ns
				02			35	
Register load to hold time 7/	t_{HRLD}			01	9, 10, 11		6	ns
				02			0	
Direct input to register/ counter hold time 7/	t_{HDR}			01	9, 10, 11		6	ns
				02			0	
Direct input to microprogram address counter hold time 7/	t_{HDPC}			01	9, 10, 11		4	ns
				02			0	

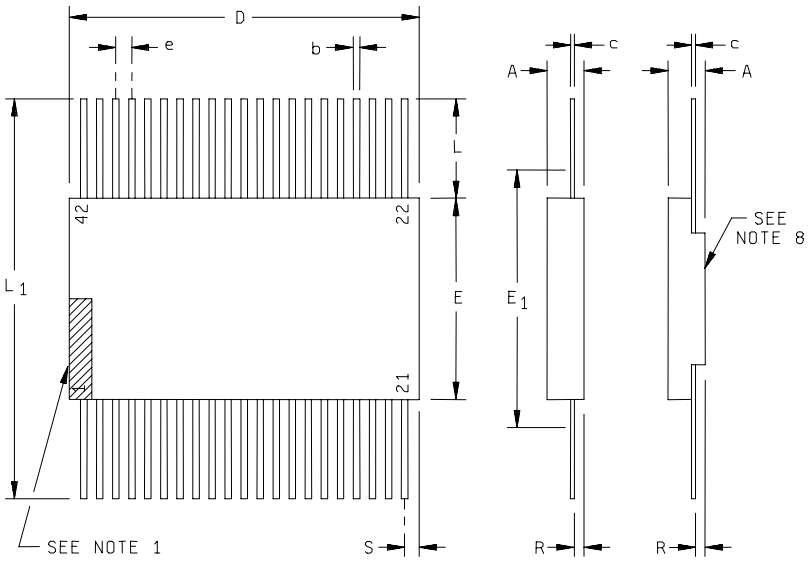
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Instruction hold time 7/	t_{HI}	C_L = 50 pF 3/	01	9, 10, 11		0	ns
			02			0	
Condition code hold time 7/	$t_{\overline{HCCI}}$		01	9, 10, 11		0	ns
			02			0	
Condition code enable hold time 7/	$t_{\overline{HCCEN1}}$		01	9, 10, 11		0	ns
			02			0	
Carry-in hold time 7/	$t_{\overline{HCI}}$		01	9, 10, 11		5	ns
			02			0	

1/ Unless otherwise specified, T_C = -55°C to +125°C and V_{CC} = 4.5 V dc to 5.5 V dc.
2/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3/ See figure 3.
4/ For device type 01 only, these instructions are conditional on the counter. Use the shorter specified delay time if the previous instruction could produce no change in the counter or could only decrement the counter. Use the longer delays from CP to outputs if the instruction prior to the clock was 4 or 12 or RLD was low.
5/ Enable/disable: Disable times measured to 0.5 V change on the output voltage level with C_L = 5.0 pF
6/ Clock periods for other instructions are determined by external conditions.
7/ Guaranteed by design, if not tested.

Case Z



Symbol	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.78	2.92	.070	.115	
b	0.43	0.58	.017	.023	5
c	0.15	0.30	.006	.012	5
D	26.16	27.69	1.030	1.090	
E	15.24	16.76	.600	.660	
E_1		17.53		.690	3
e	1.14	1.40	.045	.055	4, 6
L	6.35	9.40	.250	.370	
L_1	33.02	34.80	1.280	1.370	
R	0.51	1.14	.020	.060	2
S	1.02		.005		7

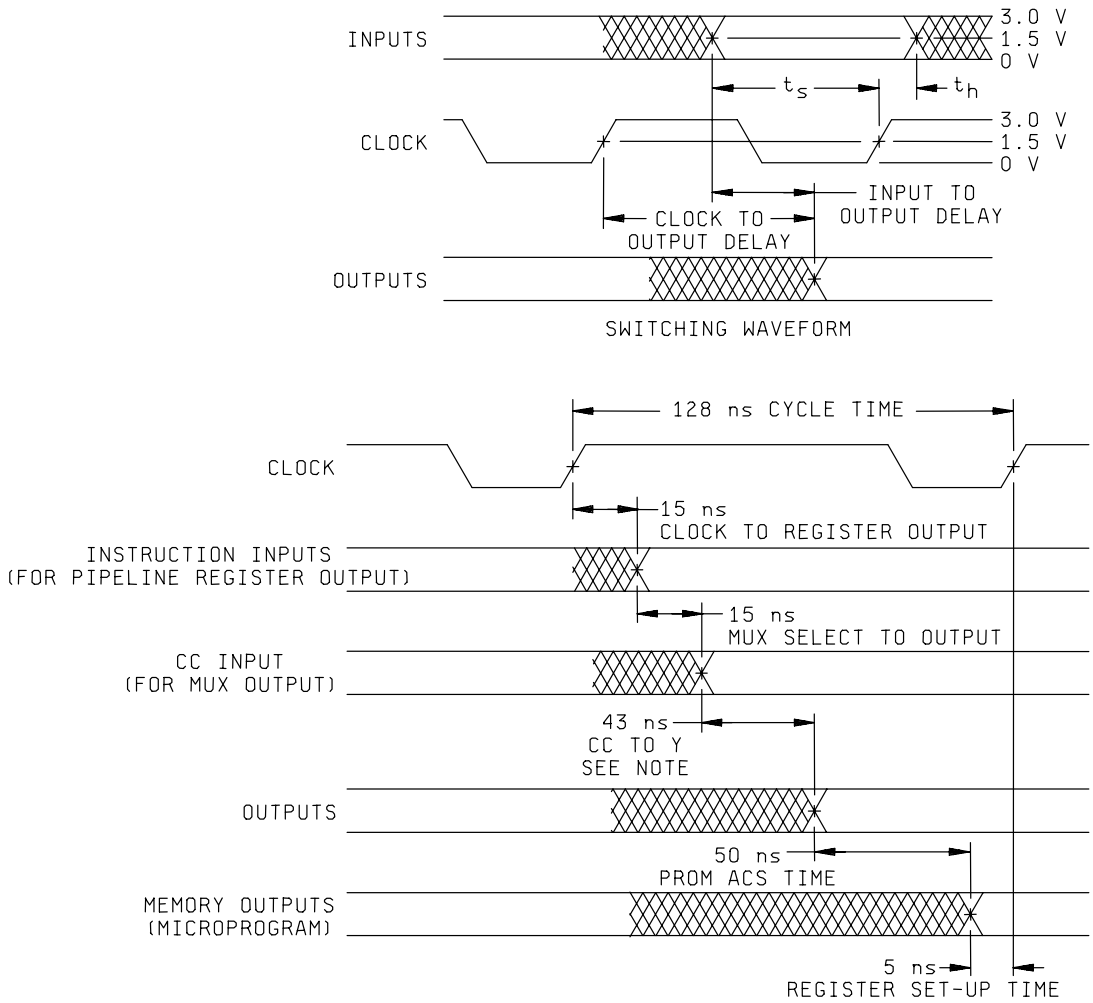
NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension R shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 (0.13 mm) of its exact logitudinal position relative to pins 1 and 42.
5. All leads – increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Forty spaces.
7. Applies to all four corners (leads number 1, 21, 22, and 42).
8. Optional configuration. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

FIGURE 1. Case outline.

Device type	All			Device type	All		
Case outline	Q			Case outline	Z		
Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	Y_4	21	D_8	1	$\overline{VECT}$	22	Y_{10}
2	D_4	22	Y_8	2	$\overline{PL}$	23	NC
3	Y_5	23	D_9	3	$\overline{MAP}$	24	D_{11}
4	D_5	24	Y_9	4	I_3	25	Y_{11}
5	$\overline{VECT}$	25	D_{10}	5	I_2	26	$\overline{OE}$
6	$\overline{PL}$	26	Y_{10}	6	V_{CC}	27	GND
7	$\overline{MAP}$	27	D_{11}	7	I_1	28	CP
8	I_3	28	Y_{11}	8	I_0	29	CI
9	I_2	29	$\overline{OE}$	9	$\overline{CCEN}$	30	Y_0
10	V_{CC}	30	GND	10	$\overline{CC}$	31	D_0
11	I_1	31	CP	11	$\overline{RLD}$	32	NC
12	I_0	32	CI	12	$\overline{FULL}$	33	Y_1
13	$\overline{CCEN}$	33	Y_0	13	D_6	34	D_1
14	$\overline{CC}$	34	D_0	14	Y_6	35	Y_2
15	$\overline{RLD}$	35	Y_1	15	D_7	36	D_2
16	$\overline{FULL}$	36	D_1	16	Y_7	37	Y_3
17	D_6	37	Y_2	17	D_8	38	D_3
18	Y_6	38	D_2	18	Y_8	39	Y_4
19	D_7	39	Y_3	19	D_9	40	D_4
20	Y_7	40	D_3	20	Y_9	41	Y_5
				21	D_{10}	42	D_5

FIGURE 2. Terminal connections.

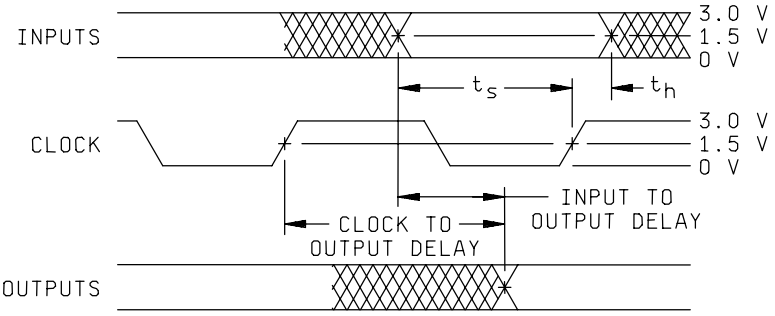
DEVICE TYPE 01



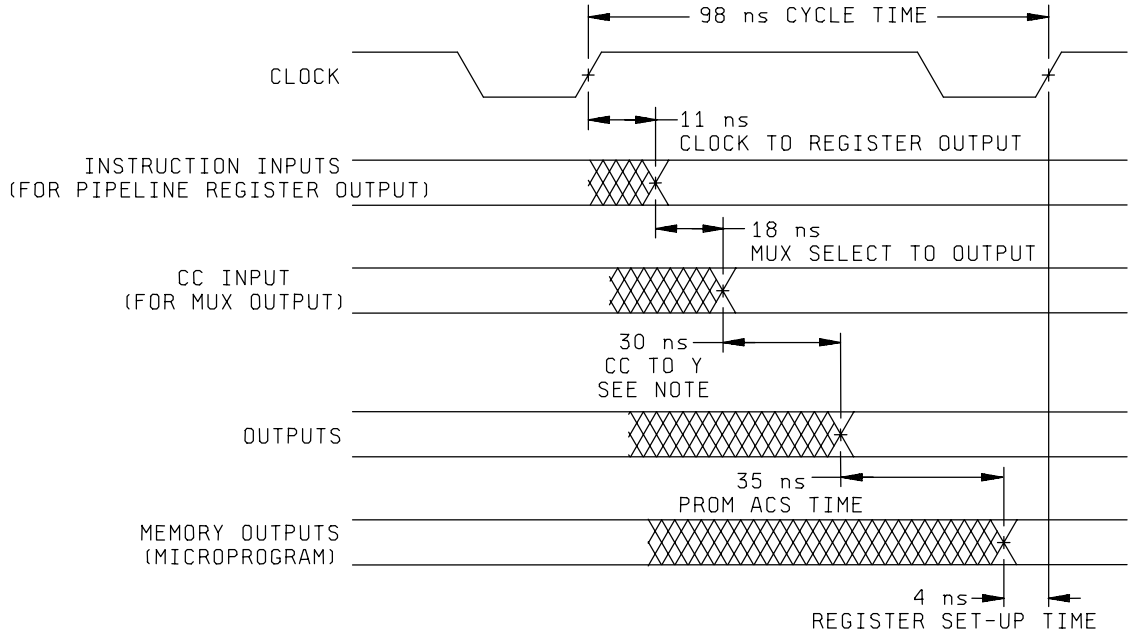
NOTE: 50 ns figure is an estimate of what worst case delay will be for the $\overline{CC}$ to Y path.

FIGURE 3. Switching and timing waveforms.

DEVICE TYPE 02



SWITCHING WAVEFORM



TYPICAL CCU CYCLE TIMING WAVEFORMS

NOTE: 30 ns figure is an estimate of what worst case delay will be for the $\overline{CC}$ to Y path.

FIGURE 3. Switching and timing waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the functionality of the device.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Pin names.

Abbreviation	Name	Abbreviation	Name
D_0 thru D_{11}	Direct input	V_{CC}	+5 Volt
I_0 thru I_3	Instruction	GND	Ground
$\overline{CC}$	Condition code	Y_0 thru Y_{11}	Microprogram address
$\overline{CCEN}$	Condition code enable	$\overline{FULL}$	Full
CI	Carry-in	$\overline{PL}$	Pipeline address enable
$\overline{RLD}$	Register load	$\overline{MAP}$	Map address enable
$\overline{OE}$	Output enable	$\overline{VECT}$	Vector address enable
CP	Clock pulse		

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-08-16

Approved sources of supply for SMD 78017 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
7801701ZX	3/	AM2910FMB
7801701QX	3/	AM2910DMB TS2910MCB/C TS2910MJB/C
7801701QA	3V146	2910/BQA
7801701ZA	3V146	2910/BZA
7801701ZC	3V146	2910/BZC
7801702QA	3V146	2910A/BQA
7801702ZA	3V146	2910A/BZA
7801702ZC	3V146	2910A/BZC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950