REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Change to Military drawing format. Add new vendor CAGE 61394. Add 2 new device types. Editorial changes throughout. Change drawing CAGE to 67268.	87-08-31	N. A. HAUCK
E	Updated boiler plate paragraphs. Added D certification paragraphs. ksr	05-02-10	Raymond Monnin
F	Boilerplate update, part of 5 year review. ksr	10-11-15	Charles F. Saffle

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV	F	F	F	F	F	F	F	F											
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS															
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
26 May 1982

REVISION LEVEL
F

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUITS,MEMORY, DIGITAL, 65,536 (8K X 8), UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**82005**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

82005	01	Y	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access	Program method
01	2764-450	8192 x 8 - Bit UV EPROM	450 ns	A,C
02	2764-250	8192 x 8 - Bit UV EPROM	250 ns	A,C
03	2764A-35	8192 x 8 - Bit UV EPROM	350 ns	B
04	2764A-25	8192 x 8 - Bit UV EPROM	250 ns	B
05	2764A-20	8192 x 8 - Bit UV EPROM	200 ns	B
06	2764-150	8192 x 8 - Bit UV EPROM	150 ns	C
07	2764-200	8192 x 8 - Bit UV EPROM	200 ns	C

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	GDIP1-T28 or CDIP2-T28	28	dual-in-line package 1/
Z	CQCC1-N32	32	rectangular leadless chip carrier 1/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage, V_{CC} .....-0.3 to 7.0 V 2/
Storage temperature range .....-65°C to +150°C
Maximum power dissipation, P_D .....1.0 W
Lead temperature (soldering, 10 seconds) .....300°C.
Thermal resistance, junction-to-case (θ_{JC}).....See MIL-STD-1835
Junction temperature (T_J)
Device types 03 - 05.....+150°C
Device types 01, 02, 06, 07 .....+175°C
All input or output voltages with respect to ground for device types 03 - 05 ...-0.6 V to 6.25 V
Input voltage range for device types 01, 02, 06, 07 .....-0.3 V dc to 7.0 V dc
V_{PP} Supply Voltage (methods A and C).....-0.3 V to 22 V
(method B).....-0.6 V to 13 V

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ All voltages referenced to V_{SS}.

1.4 Recommended operating conditions.

Case operating temperature range ..... -55°C to +125°C
Input low voltage, V_{IL} ..... -0.1 V to 0.8 V
Input high voltage, V_{IH} ..... 2.0 to V_{CC} +1
Supply voltage, V_{CC} ..... 4.5 V to 5.5 V
High level program input voltage $V_{IN(PR)}$ ..... 21.0 V ±.5 V (Program methods A and C)
High level program input voltage $V_{IN(PR)}$ ..... 12.5 V ±0.3 V (Program method B)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2 herein. When required, in screening (see 4.2 herein), or quality conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this document.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535 the “D” certification mark shall be used in place of the "C" certification mark.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \ge 125°C$		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	I_{OH} = -400 µA V_{IL} = 0.8 V, V_{IH} = 2.0 V	V_{CC} = 4.5 V	1, 2, 3	01,02,06, 07	2.4		V
			V_{CC} = 5.25 V		03 - 05	2.4		
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	V_{CC} = 5.5 V	1, 2, 3	01,02,06, 07		0.4	V
			V_{CC} = 5.25 V		03 - 05		0.45	
Low level output leakage current	I_{OL}	V_{CC} = 5.5 1/ V_{OUT} = 0.1 V		1, 2, 3	ALL		10	µA
High level output leakage current 2/	I_{OH}	V_{CC} = 5.5 V 1/ V_{OUT} = 5.5 V		1, 2, 3	ALL		10	µA
High level input current 2/	I_{IH}	V_{CC} = 5.25 V Outputs deselected V_{IN} = 5.25 V		1, 2, 3	ALL		10	µA
Low level input current 2/	I_{IL}	V_{CC} = 5.25 V Outputs deselected V_{IN} = 0.4 V		1, 2, 3	ALL		-10	µA
V_{PP} supply current read	I_{PP}	V_{PP} = 5.5 V		1, 2, 3	ALL		5	mA
Supply current (standby)	I_{SB}	Output open $\overline{CE}$ = V_{IH}	V_{CC} = 5.5 V	1, 2, 3	01, 02, 06, 07		60	mA
			V_{CC} = 5.25 V		03 - 05		40	
Supply current	I_{CC}	Output open $\overline{OE}$ = $\overline{CE}$ = V_{IL}	V_{CC} = 5.5 V	1, 2, 3	01, 02, 06, 07		120	mA
			V_{CC} = 5.25 V		03 - 05		100	
High level input leakage current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V		1, 2, 3	01, 02, 06, 07		1	µA
					03 - 05		10	
Low level input leakage current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.1 V		1, 2, 3	01, 02, 06, 07		1	µA
					03 - 05		-10	
High level input voltage	V_{IH}	V_{CC} = 4.5 V 3/		1, 2, 3	ALL	2.0	6.5	V
Low level input voltage	V_{IL}	V_{CC} = 5.5 V 3/		1, 2, 3	ALL	-0.1	0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \ge 125°C$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V_{PP} read voltage	V_{PP}		1, 2, 3	ALL	V_{CC} -0.7	V_{CC} +1	V
Input capacitance 2/ 4/	C_{IN}	V_{IN} = 0V T_C = +25°C f = 1 MHz See 4.3.1c	4	All		6	pF
Output capacitance 4/	C_{OUT}	V_{OUT} = 0V T_C = +25°C f = 1 MHz See 4.3.1c	4	All		12	pF
Address access time	t_{AA}	V_{CC} = 5.25 V 2/ 5/ See figure 5	9, 10, 11	06		150	ns
				05, 07		200	
				01		450	
				02, 04		250	
				03		350	
Chip enable access time	t_{CE}		9, 10, 11	06		150	ns
				05, 07		200	
				01		450	
				02, 04		250	
				03		350	
Output enable access time	t_{OE}		9, 10, 11	03	15	130	ns
				01	15	200	
				02, 04, 06	10	100	
				05, 07	0	150	
Chip enable or Output enable to high Z	t_{DF} 6/		9, 10, 11	03	0	115	ns
				01	5	150	
				02	0	90	
				04	0	60	
				05, 07	0	150	
				06	0	80	
Output hold from address change	t_{OH} 6/		9, 10, 11	All	0		ns

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OL} and I_{OH} with the output under test connected to V_{OUT}.

2/ Outputs shall be loaded per figure 4.

3/ Tests for all inputs and control pins.

4/ All pins not being tested are to be grounded.

5/ Equivalent ac test conditions (actual load conditions vary by tester): Output load: 1 TTL gate and C_L = 100 pF.
Input rise and fall times $\le$ 20 ns.
Input pulse levels: 0.4 V and 2.4 V.

6/ Tested initially and after any design changes.

Device Types	All	
Case Outlines	Y	Z
Terminal Number	Terminal Symbol	Terminal Symbol
1	V_{PP}	NC
2	A12	V_{PP}
3	A7	A12
4	A6	A7
5	A5	A6
6	A4	A5
7	A3	A4
8	A2	A3
9	A1	A2
10	A0	A1
11	Q0	A0
12	Q1	NC
13	Q2	Q0
14	V_{SS}	Q1
15	Q3	Q2
16	Q4	V_{SS}
17	Q5	NC
18	Q6	Q3
19	Q7	Q4
20	$\overline{CE}$	Q5
21	A10	Q6
22	$\overline{OE}$	Q7
23	A11	$\overline{CE}$
24	A9	A10
25	A8	$\overline{OE}$
26	NC	NC
27	$\overline{PGM}$	A11
28	VCC	A9
29		A8
30		NC
31		$\overline{PGM}$
32		VCC

Pin names	
$A_0 – A_{12}$	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$,	Output enable
$Q_0 – Q_7$	Outputs
$\overline{PGM}$	Program pin

Option A with active terminals on plane 1.

FIGURE 1. Terminal connections.

Device types 01, 02, 06,and 07

Pins Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output enable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon signature * (Intelligent identifier)	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded data

X can be either V_{IL} or V_{IH}.
* For silicon signature (tm) (intelligent identifier) A0 is toggled.
A9 = 12 $\pm$0.5 V, and all other addresses are at a TTL low (V_{IL}).

Device types 03, 04, and 05

Mode/pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs	V_{PP}
Programming method	A, B	A, B	A, B	A	A, B	B
Deselect	V_{IL}	V_{IH}	V_{IH}	V_{CC}	High Z	V_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}	V_{CC}
Standby	V_{IH}	X	X	V_{CC}	High Z	V_{CC}
Program	V_{IL}	V_{IH}	V_{IL}	+21 V	D_{IN}	+21.5 V
Program inhibit	V_{IH}	X	X	+21 V	High Z	+21.5 V
Program verify	V_{IL}	V_{IL}	V_{IH}	+21 V	D_{OUT}	+21.5 V

It is recommended that verification for method A & B devices be performed after the completion of programming all bytes.
X means input is a "don't care".

FIGURE 2. Truth tables.

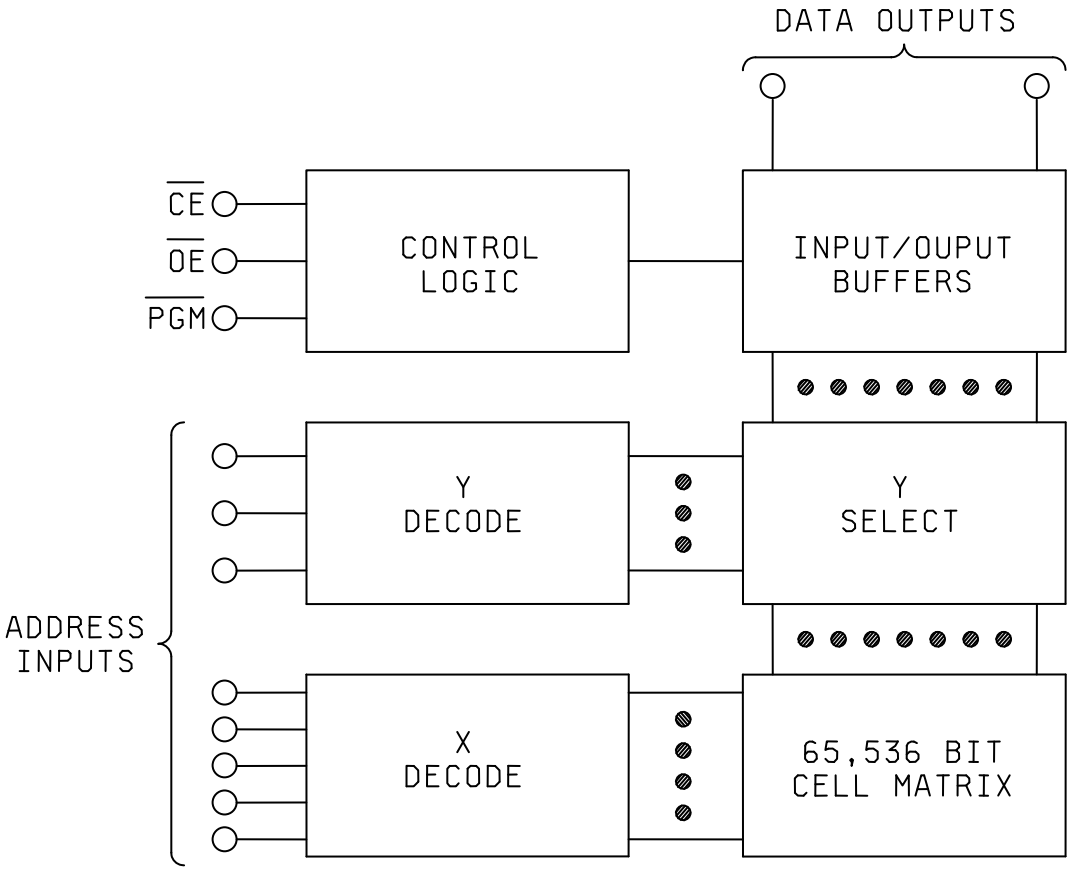


FIGURE 3. Logic diagram.

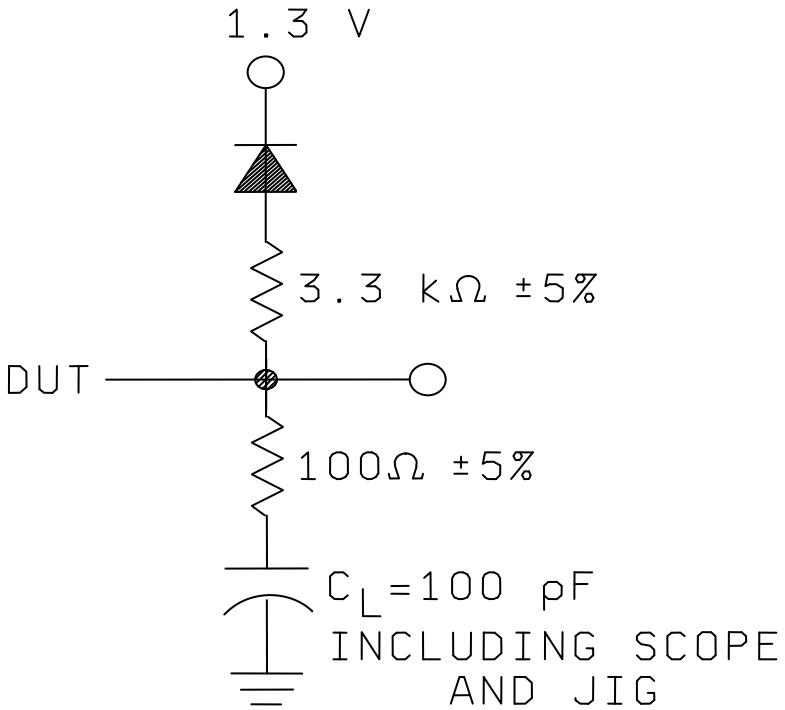
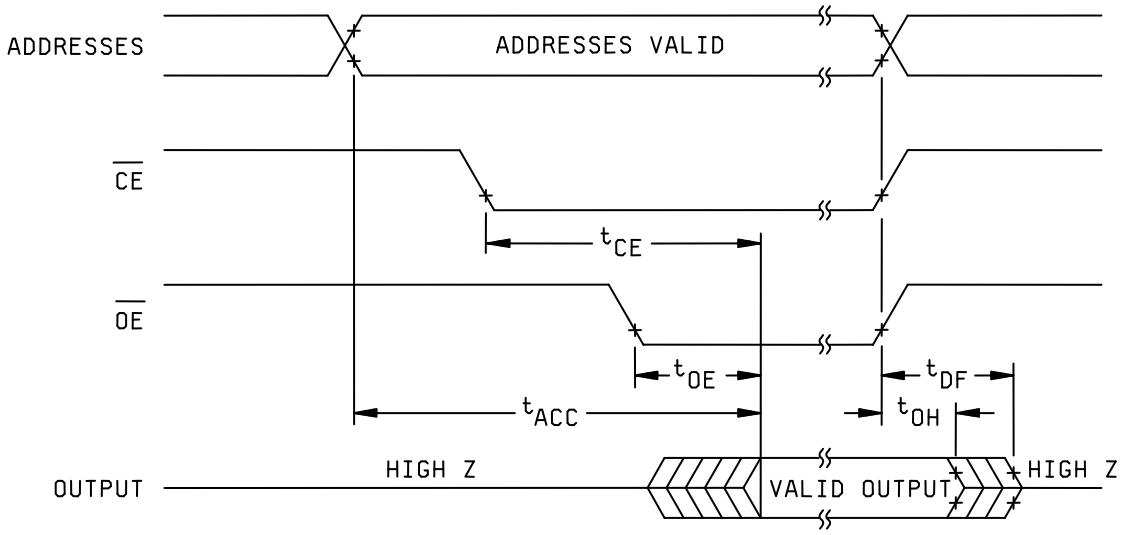


FIGURE 4. Output load. (suggested)

Device types 01, 02, 06, and 07.



NOTES:

1. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
2. OE may be delayed up to t_{ACC} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

FIGURE 5. Read cycle timing diagram.

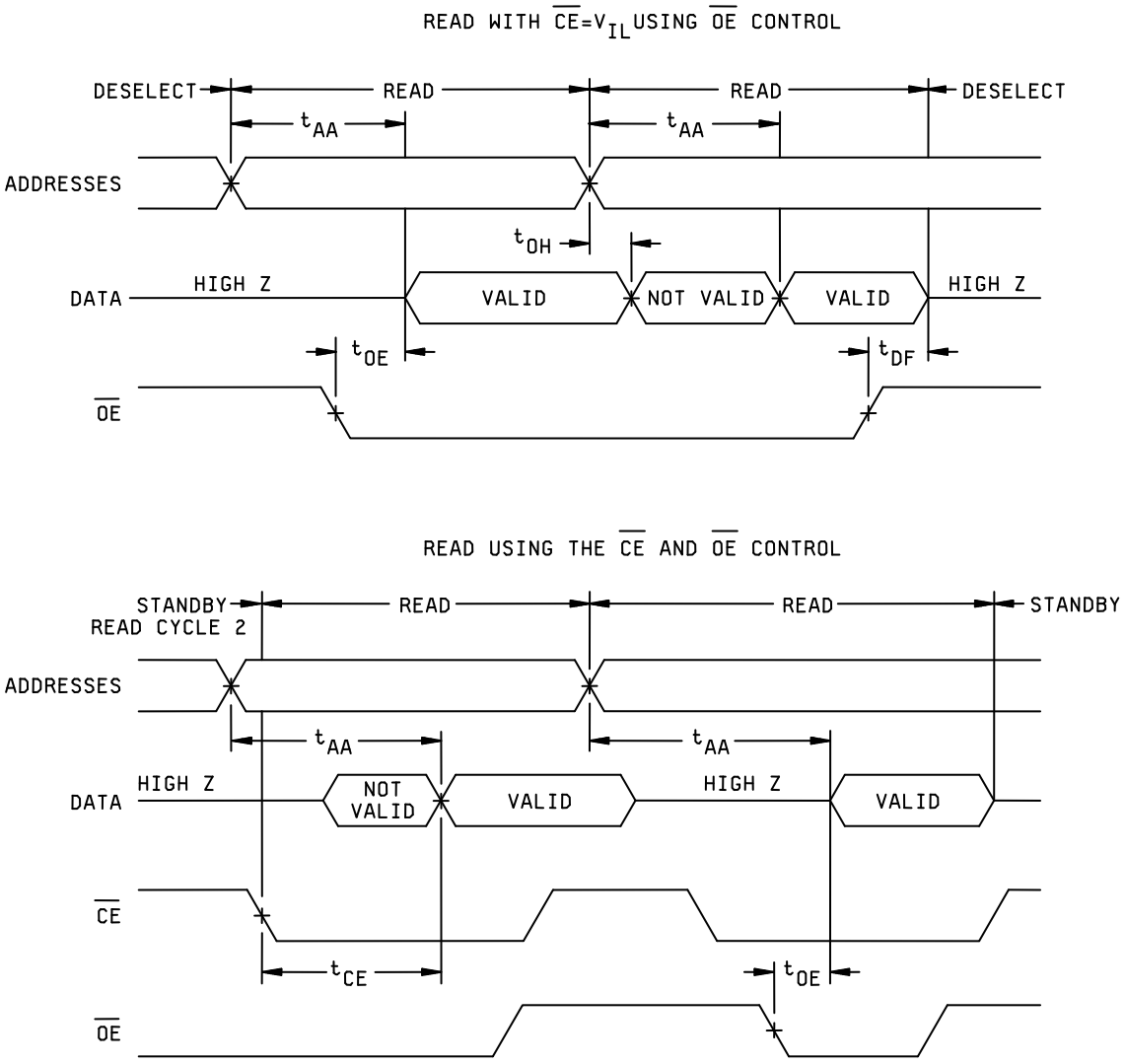


FIGURE 5. Read cycle timing diagram - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps.

Margin test method A.

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.6.2).
2. Bake, unbiased, for 12 hours at 200°C.
3. Perform a margin test using $V_M = V_{CC}$ = 6.0 V at 25°C using loose timing.
4. Erase device, then program 45 percent – 50 percent of the bits to a worst case speed pattern.
5. Perform dynamic burn-in (see 4.2a).
6. Perform a margin test using $V_M = V_{CC}$ = 6.0 V at 25°C.
7. Perform 100 percent electrical testing at +125°C and -55°C. Perform 100 percent ac and dc electricals at 25°C.
8. Erase device (see 3.6.1), except devices submitted for groups A, B, C, and D.
9. Verify erasure (see 3.6.3).

Margin test method B.

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.6.2). The remaining cells shall provide a worst case speed pattern.
2. Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.
3. Perform a margin test using V_M = 5.9 V at 25°C using loose timing. (i.e., t_{ACC} = 1 µs)
4. Perform dynamic burn-in (see 4.2a)
5. Perform a margin test using V_M = 5.9 V.
6. Perform electrical tests (see 4.2).
7. Erase device (see 3.6.1), except devices submitted for groups A, B, C, and D.
8. Verify erasure (see 3.6.3).

Margin test method C

1. Program at 25°C with a greater than 95 percent pattern (ex. diagonal "1's") (see 3.6.2).
2. Unbiased bake for 8 hours at 200°C or 24 hours at 170°C or 72 hours at 150°C.
3. Test at 95°C (see 3.6.3), including a margin test at VM = +6 V and loose timing (i.e. T_{ACC} = 1 µs).
4. Erase (see 3.6.1).
5. Program at 25°C with a 50 percent pattern (ex. checkerboard bar) (see 3.5.2) (Programmed with checkerboard at wafer sort).
6. Test at 125°C (see 3.6.3).
7. Burn-in (see 4.2a).
8. Test at 125°C (see 3.6.3).
9. Test at -55°C (see 3.6.3).
10. Erase (see 3.6.1). Devices may be submitted for groups A, B, C, and D testing at this point.
11. Verify erasure at 25°C (see 3.6.3).

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 9 or 2, 8A, 10
Additional electrical subgroups for group C periodic inspections	- - -

1/ * PDA applies to subgroup 1.
2/ Any or all subgroup may be combined when using a high speed tester.
3/ Subgroup 8 shall consist of verifying the pattern specified.
4/ For all electrical tests, the device shall be programmed to the pattern specified.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} / C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The device is erased by exposure to high intensity shortwave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm2. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 shortwave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about one inch from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedures.

4.5.1 Programming procedures for method A and C. The programming characteristics in table IIIA, IIIC; and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table IIIA and IIIC shall apply

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{PP} is 21.0 ±0.5 V and chip enable and $\overline{PGM}$ is brought low.

4.5.2 Programming procedures for method B. The programming characteristics in table IIIB and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table IIIB shall apply

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{PP} is 12.50 ±0.3 V and chip enable and $\overline{PGM}$ is brought low.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross-referenced in 6.4 herein with the manufacture's symbol or CAGE number.

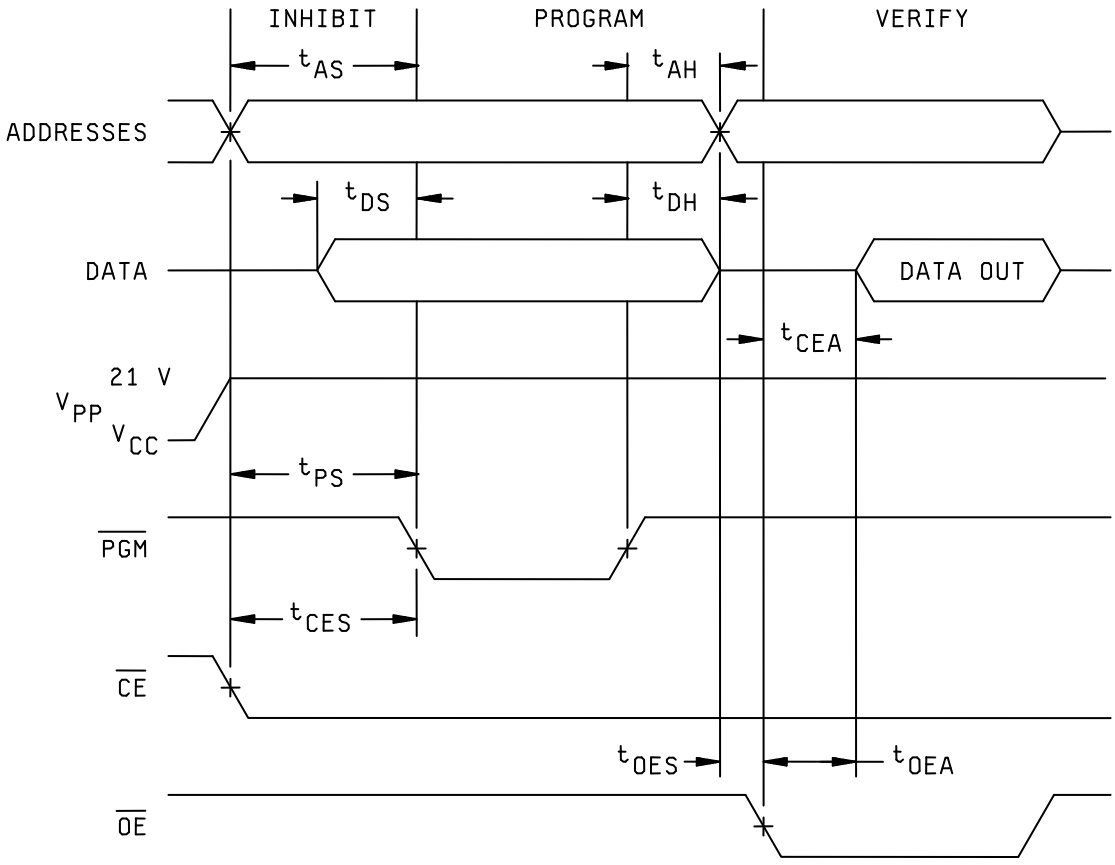
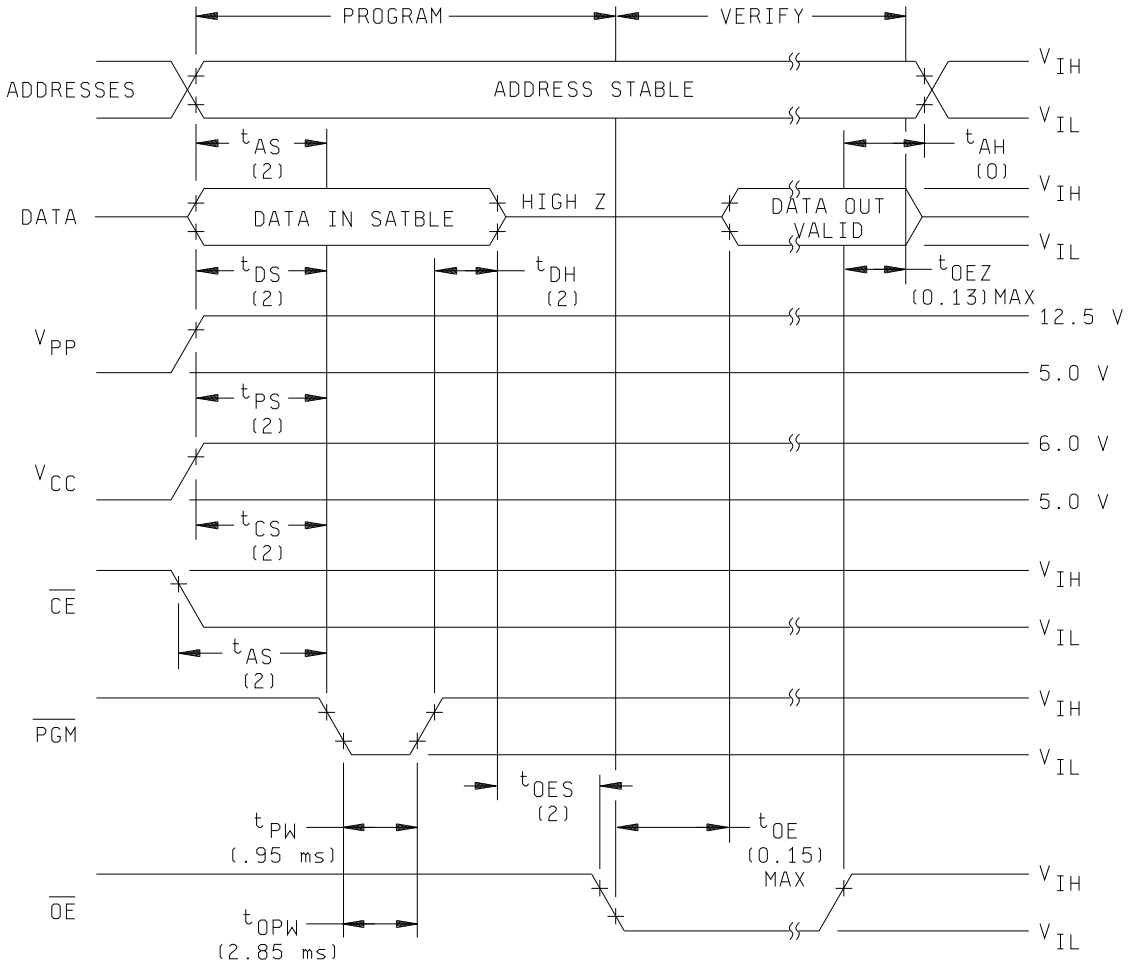


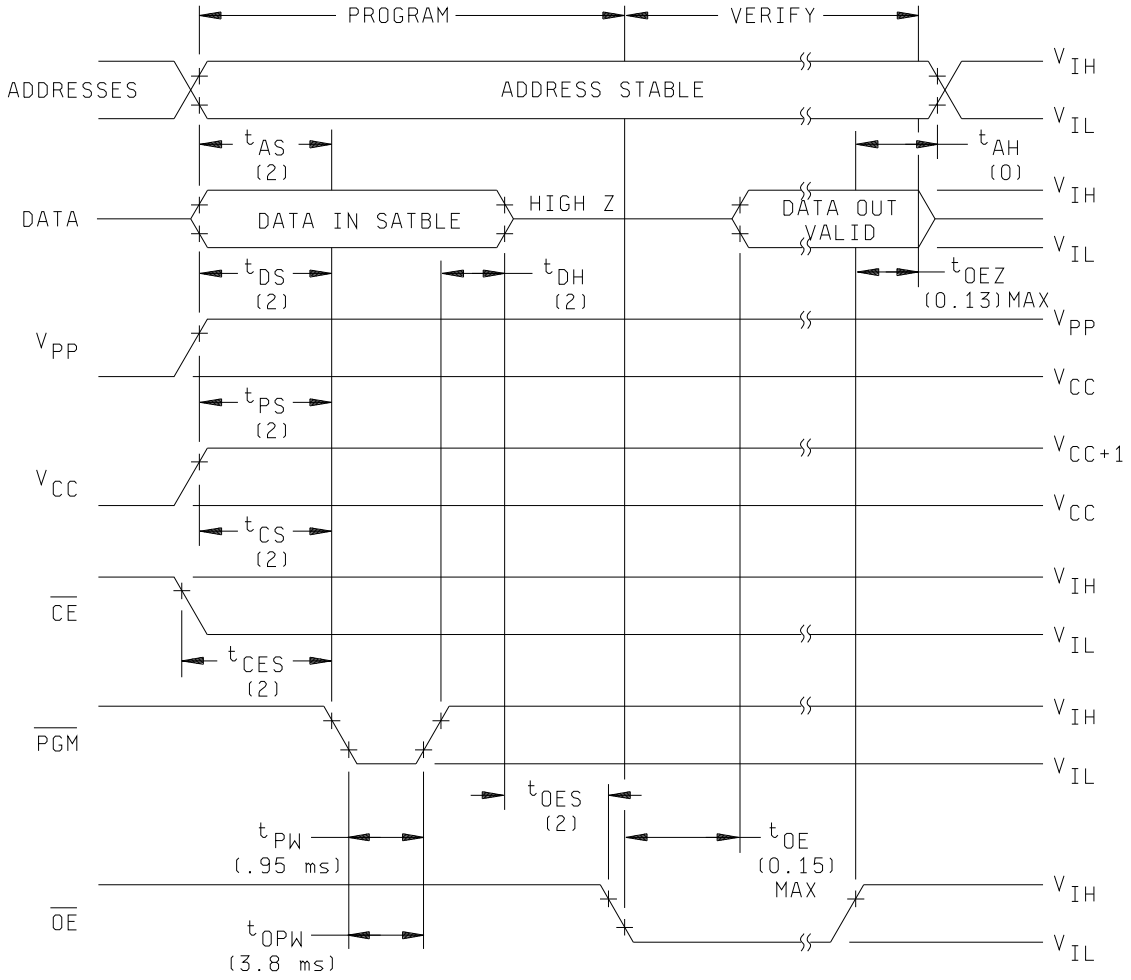
FIGURE 6. Programming timing diagram for method A.



NOTES:

1. All times shown in ( ) are minimum and in µsec unless otherwise specified.
2. The input timing reference level is .8 V for V_{IL} and 2 V for a V_{IH}.
3. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 6. Programming timing diagram for method B.



NOTES:

1. All times shown are minimum and in µsec unless otherwise specified.
2. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.
3. T_{oe} andTt_{ofp} are characteristics of the device but must be accommodated by the programmer.
4. When programming, a 0.1 µF ceramic capacitor is required across V_{pp} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 6. Programming timing diagram for method C.

TABLE IIIA. Programming characteristics for method A.

Test	Symbol	Conditions 1/	Limits		Unit
			Min	Max	
Input low voltage	V_{IL}			0.8	V
Input high voltage	V_{IH}		2.0	V_{CC} +1	V
Input leakage current	I_{IL}	Except $\overline{OE}$ / V_{PP} 0.4 V ≤ V_{IN} ≤ 5.25 V	-10	+10	µA
Programming voltage	V_{PP}		20.5	21.5	V
Programming supply current	I_{PP2}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}		30	mA
V_{CC} power supply current	I_{CC}			150	mA
Address setup time	t_{AS}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Program pulse width	t_{PN}		45	55	ms
V_{PP} setup time	t_{PS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
$\overline{CE}$ setup time	t_{CES}		2		µs

1/ t_{CEH} is measured from $\overline{OE}$ / V_{PP}.

TABLE IIIB. Programming characteristics for method B.

Test	Symbol	Conditions 1/ VCC = 6.0 V ±0.25 V, VPP = 12.5 V ±0.3 V	Limits		Units
			Min	Max	
Input current (all inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low voltage	V_{IL}		-0.1	0.8	V
Input high voltage	V_{IH}		2.0	V_{CC} +1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			100	mA
V_{PP} supply current (program)	I_{PP}	$\overline{CE} = V_{IL}$		50	mA
A_9 intelligent identifier voltage	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{OEZ}	2/	0	130	ns
V_{PP} setup time	t_{PS}		2		µs
V_{CC} setup time	t_{CS}		2		µs
$\overline{PGM}$ initial program pulse width	t_{PW}	3/	0.95	1.05	ms
$\overline{PGM}$ over program pulse width	t_{OPW}	4/	2.85	78.75	ms
Data valid from $\overline{OE}$	t_{OE}			150	ns

NOTES:

1/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2/ This parameter is only sampled and is not 100 per cent tested. Output float is defined as the point where data is no longer driven – see timing diagram for method B.

3/ Initial program pulse width tolerance is 1 ms ±5 per cent.

4/ The length of the over program pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.

TABLE IIIC. Programming characteristics for method C.

Test	Symbol	Conditions 1/ $5.75\ V \le V_{CC} \le 6.25\ V$, $20.5\ V \le V_{PP} \le 21.5\ V$ $T_A = +25°C \pm 5°C$	Limits		Units
			Min	Max	
Input current (all inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low voltage	V_{IL}		-0.1	0.8	V
Input high voltage	V_{IH}		2.0	V_{CC} +1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			120	mA
V_{PP} supply current (program)	I_{PP}	$\overline{CE} = V_{IL}$		50	mA
A_9 intelligent identifier voltage	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{OEZ}	2/	0	130	ns
V_{PP} setup time	t_{PS}		2		µs
V_{CC} setup time	t_{CS}		2		µs
$\overline{PGM}$ initial program pulse width	t_{PW}		0.95	1.05	ms
$\overline{PGM}$ over program pulse width	t_{OPW}		2.85	78.75	ms
Data valid from $\overline{OE}$	t_{OE}			150	ns
$\overline{CE}$ setup time	t_{CES}		2		µs

NOTES:
1/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2/ Tested by inference only.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved source of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-11-15

Approved sources of supply for SMD 82005 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Programming method	Margin test method
8200501YA	3/	DM2764-450	C	C
8200501ZA	3/	AM2764-45/BUA	A	A
8200502YA	3/	DM2764-250	C	C
8200502ZA	3/	AM2764-25/BUA	A	A
8200503YA	3/	AM2764A-35/BXA	B	A
	3/	MD2764A-35/B	B	B
	3V146	MC2764A-35/BYA	B	B
8200503ZA	3/	AM2764A-35/BUA	B	A
	3/	MD2764A-35/B	B	B
	3V146	MR2764A-35/BZA	B	B
8200504YA	3/	AM2764A-25/BXA	B	A
	3/	MD2764A-25/B	B	B
	3V146	MC2764A-25/BYA	B	B
8200504ZA	3/	AM2764A-25/BUA	B	A
	3/	MD2764A-25/B	B	B
	3V146	MR2764A-25/BZA	B	B
8200505YA	3/	AM2764A-20/BXA	B	A
8200505ZA	3/	AM2764A-20/BUA	B	A
8200506YA	3/	DM2764-150	C	C
8200507YA	3/	DM2764-200	C	C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address	Intelligent identifier manufacturer	Device
3V146	Rochester Electronics Inc. 10 Malcolm Hoyt Drive Newburyport, MA 01950	89	08

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.