REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added vendor CAGE 01295 with device types 04 - 07 complete revision.	83-10-07	N. A. Hauck
B	Added vendor CAGE 34335 to device types 01, 02, 03, 06, and 07. Added device types 08, 09, 10. Device types 04 and 05 not available from an approved source. Inactivated device types 01, 02, and 03 for DIP package for new design.	86-01-20	N. A. Hauck
C	Change limits of t_{OFF} and t_{RMW}. Editorial changes throughout.	86-05-23	R. P. Evans
D	Added vendor CAGE 6Y440 with device types 04 and 05. Changed to military drawing format.	87-04-28	N. A. Hauck
E	Changes in accordance with NOR 5962-R157-96.	96-06-26	M. A. Frye
F	Updated boilerplate. Added provisions for the supply of QD certified parts to the drawing. Added CAGE 3V146 to drawing. - glg	00-12-22	Raymond Monnin
G	Correction to marking paragraph 3.5, updated boilerplate paragraphs. ksr	05-03-02	Raymond Monnin
H	Boilerplate update, part of 5 year review. ksr	10-11-17	Charles F. Saffle

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE IS 67268.

REV																				
SHEET	H	H	H	H																
REV	15	16	17	18																
SHEET																				

REV STATUS OF SHEETS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Darrell Hill

DLA LAND AND MARITIME

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
C. R. Jackson

APPROVED BY
William E. Shoup

DRAWING APPROVAL DATE
82-05-28

REVISION LEVEL
H

MICROCIRCUIT, MEMORY, DIGITAL, NMOS, 65,536 x 1 BIT DYNAMIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**82010**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

82010	01	E	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types shall identify the circuit functions as follows:

Device type	Generic number 1/	Circuit	Access time	Refresh
01		65,536 X 1-bit RAM	150 ns	128 cycles (1 ms)
02		65,536 X 1-bit RAM	150 ns	128 cycles (2 ms)
03		65,536 X 1-bit RAM	200 ns	128 cycles (2 ms)
04		65,536 X 1-bit RAM	150 ns	256 cycles (4 ms)
05		65,536 X 1-bit RAM	200 ns	256 cycles (4 ms)
06		65,536 X 1-bit RAM	150 ns	256 cycles (4 ms)
07		65,536 X 1-bit RAM	200 ns	256 cycles (4 ms)
08		65,536 X 1-bit RAM	120 ns	256 cycles (4 ms)
09		65,536 X 1-bit RAM	150 ns	128 cycles (2 ms)
10		65,536 X 1-bit RAM	200 ns	128 cycles (2 ms)

1.2.2 Case outlines. The case outlines shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line package
Z	CQCC3-N18	18	rectangular chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -1.5 to +7.0 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D)
(minimum cycle time) ..... 1.0 W
Lead temperature (soldering, 5 seconds) ..... +270°C
Thermal resistance, junction-to-case (θ_{JC}): ..... See MIL-STD-1835
Junction temperature (T_J)- ..... +150°C
Short circuit output current ..... 150 mA

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535, as applicable (see 6.6 herein).

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc to 5.5 V dc
Maximum low-level input voltage (V_{IL}):	
Device types 01, 02, and 03	-1.5 V dc to 0.8 V dc
Device types 04, 05, 06, 07, and 08	-0.6 V dc to 0.8 V dc
Device types 09 and 10	-1.0 V dc to 0.8 V dc
Maximum high-level input voltage (V_{IH}):	
Device types 01, 02, and 03	2.4 V dc to 6.5 V dc
Device types 04, 05, 06, 07, and 08	2.4 V dc to 5.8 V dc
Device types 09 and 10	2.4 V dc to V_{CC} +1.0 V dc
Refresh cycle time:	
Device type 01	1.0 ms
Device types 02, 03, 09, and 10	2.0 ms
Device types 04, 05, 06, 07, and 08	4.0 ms
Case operating temperature range:	
Device types 01, 02, 03, 06, 07, 08, 09, and 10	-55°C to +110°C
Device types 04 and 05	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535 the “D” certification mark shall be used in place of the "C" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +110°C$, 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	V_{DD} = 5 V, V_{IN} = 0 or V_{DD} I_{OH} = -5 mA	1, 2, 3	All	2.4		V
Low-level output voltage	V_{OL}	V_{DD} = 5 V, V_{IN} = 0 or V_{DD} I_{OL} = 4.2 mA	1, 2, 3	All		0.4	V
Supply current, standby	I_{DD1}	V_{DD} = 5 V, $\overline{CAS}$ = $\overline{RAS}$ = V_{IH} D_{OUT} = High Z	1, 2, 3	All		5	mA
Supply current, operating	I_{DD2} 2/	V_{DD} = 5 V, $\overline{RAS}$ and $\overline{CAS}$ cycling $t_{CYC} = t_{RC}$ min	1, 2, 3	01,02,03, 04,05,06, 07,08,09 10		60 55	mA
Supply current, $\overline{RAS}$ only cycle	I_{DD3}	V_{DD} = 5 V, $\overline{RAS}$ = cycling, $t_{CYC} = t_{RC}$ min, $\overline{CAS}$ = V_{IH}	1, 2, 3	01,02,03, 04,05,06, 07,08,09 10		45 40	mA
Supply current, PAGE mode	I_{DD4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{pc} = min	1, 2, 3	09 10		45 40	mA
High-level input leakage current	I_{IH}	V_{DD} = 5 V, V_{IN} = 5.0 V	1, 2, 3	All		10	µA
Low-level input leakage current	I_{IL}	V_{DD} = 5 V, V_{IN} = 0.8 V	1, 2, 3	All		-10	µA
High-level output leakage current	I_{OH}	V_{DD} = 5 V, V_{OUT} = 5.5 V $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	1, 2, 3	All		10	µA
Low-level output leakage current	I_{OL}	V_{DD} = 5 V, V_{OUT} = GND $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	1, 2, 3	All		-10	µA
Input capacitance (A_0 - A_7)	C_1 3/	T_C = +25°C	4	01,02,03, 09,10 04,05, 06,07,08		5 7	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, DIN, $\overline{WE}$)	C_2 3/	T_C = +25°C	4	01,02,03, 04,05,06, 07,08 09,10		10 7	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +110°C$, 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output capacitance (RAS)	C_{OUT} 3/	T_C = +25°C	4	01,02,03, 04,05,06, 07,08		8	pF
				09,10		6	
Access time from $\overline{RAS}$	t_{RAC} 4/ 5/	See figure 3	9, 10, 11	01,02			ns
				04,06,09		150	
				03,05, 07,10		200	
				08		120	
Access time from $\overline{CAS}$	t_{CAC} 3/ 4/ 5/	See figure 3	9, 10, 11	04,06,10		100	ns
				01,02		90	
				03		120	
				05,07		135	
				08		70	
				09		75	
Time between refresh	t_{REF}	See figure 3	9, 10, 11	01		1.0	ms
				02,03,09,10		2.0	
				04, 05, 06,07,08		4.0	
$\overline{RAS}$ precharge time	t_{RP}	See figure 3	9, 10, 11	04	160		ns
				01,02,06,09	100		
				03	135		
				05	200		
				07,10	120		
				08	80		
$\overline{CAS}$ precharge time (nonpage cycles)	t_{CPN}		9, 10, 11	09	30		ns
				10	35		
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	See figure 3	9, 10, 11	All	0		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	See figure 3	9, 10, 11	04	20	50	ns
				01,02,06	30	60	
				03,07	35	80	
				05	25	65	
				08	15	50	
				09	30	75	
				10	35	100	
$\overline{RAS}$ hold time	t_{RSH}	See figure 3	9, 10, 11	04,06,10	100		ns
				01,02	90		
				03	120		
				05,07	135		
				08	60		
				09	75		
$\overline{CAS}$ hold time	t_{CSH}	See figure 3	9, 10, 11	04,06			ns
				01,02,09	150		
				03,05,07,10	200		
				08	120		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +110°C$, 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Row address setup time	t_{ASR}	See figure 3	9, 10, 11	01,02,03, 06,07,08, 09,10	0		ns
				04,05	5		
Row address hold time	t_{RAH}	See figure 3	9, 10, 11	01,02, 04,06,09	20		ns
				03,07,10,	25		
				08	15		
Column address setup time	t_{ASC}	See figure 3	9, 10, 11	01,02,03, 04,05,09, 10	0		ns
				06,07,08	-5		
Column address hold time	t_{CAH}	See figure 3	9, 10, 11	04	60		ns
				01,02,09	30		
				03,08,10	40		
				05	70		
				06	45		
				07	55		
Column address hold time, to $\overline{RAS}$	t_{AR}	See figure 3	9, 10, 11	04,06	95		ns
				01,02	100		
				03	130		
				05,07,10	140		
				08	85		
				09	105		
Transition time	t_T	See figure 3 6/	9, 10, 11	01,02,03, 06,07,08, 09,10	3	50	ns
				04,05	3	20	
Output buffer turn-off delay	t_{OFF}	See figure 3 7/	9, 10, 11	03,04,07, 10	0	50	ns
				01,02	0	40	
				06,08,09	0	40	
				05	0	60	
Read and refresh cycles: Random read cycle time	t_{RC}	See figure 3	9, 10, 11	04	330	1,500	ns
				01,02,06	260	10,000	
				03	345	10,000	
				05	420	1,500	
				07	330	10,000	
				08	230		
				09	260		
				10	330		
$\overline{RAS}$ pulse width	t_{RAS}	See figure 3	9, 10, 11	04	150	1,500	ns
				01,02,06,09	150	10,000	
				03,07,10	200	10,000	
				05	200	1,500	
				08	120	10,000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +110°C$, 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
				04	100	1,500	
$\overline{CAS}$ pulse width	t_{CAS}	See figure 3	9, 10, 11	01,02	90	10,000	ns
				03	120	10,000	
				05	135	1,500	
				06,10	100	10,000	
				07	135	10,000	
				09	75	10,000	
Read command set-up time	t_{RCS}	See figure 3	9, 10, 11	All	0		ns
Read command hold time	t_{RCH}	See figure 3	9, 10, 11	All	0		ns
				04	330	1,500	
Write cycle:		See figure 3		07	330	10,000	
Random write cycle time	t_{WC}		9, 10, 11	01,02,06	260	10,000	ns
				03	345	10,000	
				05	420	1,500	
				08	230		
				09	260		
				10	330		
Write command setup time	t_{WCS}	See figure 3	9, 10, 11	01,02,03, 04,05,06,07	0		ns
				08	-5		
				09,10	-10		
				04,06	60		
Write command hold time	t_{WCH}	See figure 3	9, 10, 11	01,02,10	45		ns
				03	55		
				05,07	80		
				08	40		
				09	35		
				04	125		
Write command hold time to $\overline{RAS}$	t_{WCR}	See figure 3	9, 10, 11	01,02	120		ns
				03	150		
				05	160		
				06,09	110		
				07,10	145		
				08	85		
				01,02			
Write command pulse width	t_{WP}	See figure 3	9, 10, 11	04,06,10	45		ns
				03,05,07	55		
				08	25		
				09	35		
				04,06	60		
Write command to $\overline{RAS}$ lead time	t_{RWL}	See figure 3	9, 10, 11	01,02,09	45		ns
				03,10	55		
				05,07	80		
				08	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +110°C$, 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Write command to $\overline{CAS}$ lead time	t_{CWL}	See figure 3	9, 10, 11	04,06	60		ns
				01,02,09	45		
				03,10	55		
				05,07	80		
				08	50		
Data-in setup time	t_{DS}	See figure 3	9, 10, 11	All	0		ns
Data-in hold time	t_{DH}	See figure 3	9, 10, 11	04,06	60		ns
				01,02,10	45		
				03	55		
				05,07	80		
				08	40		
				09	35		
Data-in hold time, to $\overline{RAS}$	t_{DHR}	See figure 3	9, 10, 11	04	125		ns
				01,02	120		
				03	150		
				05	160		
				06,09	110		
				07,10	145		
				08	85		
Read modify write cycle time	t_{RMW}	See figure 3	9, 10, 11	01,02	280	10,000	ns
				04	345	1,500	
				05	425	1,500	
				06	285	10,000	
				08	260	10,000	
				03	370	10,000	
				07	345	10,000	
				09	280		
				10	345		
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	See figure 3	9, 10, 11	04,06	110		ns
				01,02,09	120		
				03	165		
				05,07	130		
				08	85		
				10	155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	See figure 3	9, 10, 11	04,06	60		ns
				01,02,10	55		
				03	80		
				05,07	65		
				08	40		
				09	45		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	See figure 3	9, 10, 11	01,02,04,05	20		ns
				03	25		
				06,07,08	5		
				09,10	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \le T_C \le +110^{\circ}C$, 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Page mode read or write cycle	t_{PC}	See figure 3	9, 10, 11	09	145		ns
				10	190		
$\overline{CAS}$ precharge time, page mode	t_{CP}	See figure 3	9, 10, 11	09	60		ns
				10	80		

1/ Device types 04 and 05, $T_C = -55^{\circ}C$ to $+125^{\circ}C$.

2/ I_{DD} is dependent on output loading and cycle rates. The I_{DD} measurements are made with the outputs open. Limits are for cycle rates listed in condition column and worst case data pattern (alternate "1" and "0") at a PRR = 4.0 MHz. $T_{CYC} = T_{RC}$ min.

3/ Capacitance measured with Boonton meter or equivalent or effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and $V_{CC} = 5.0$ V.

4/ Load = One Schottky TTL +100 pF or equivalent for device types 01, 02, and 03.

5/ Load = Two Schottky TTL +100 pF or equivalent for device types 04, 05, 06, 07, 08, 09, and 10.

6/ Devices are tested at $t_T = 5$ ns, where t_T is the rise and fall time for $\overline{RAS}$ and $\overline{CAS}$.

7/ Tested only initially and after any design changes.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005,table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 9

* PDA applies to subgroup 1.

Device types	All	
Case outlines	E	Z
Terminal number	Terminal symbol	
1	NC	NC
2	D_{IN}	D_{IN}
3	$\overline{WE}$	$\overline{WE}$
4	$\overline{RAS}$	$\overline{RAS}$
5	A_0	NC
6	A_2	A_0
7	A_1	A_2
8	V_{DD}	A_1
9	A_7	V_{DD}
10	A_5	A_7
11	A_4	A_5
12	A_3	A_4
13	A_6	A_3
14	D_{OUT}	NC
15	$\overline{CAS}$	A_6
16	V_{SS}	D_{OUT}
17	- - -	$\overline{CAS}$
18	- - -	V_{SS}

FIGURE 1. Terminal connections.

Truth Table						
INPUTS						OUTPUT
Operation 7/	$\overline{RAS}$	$\overline{CAS}$	D_{IN}	Address	$\overline{Write}$	D_{OUT} 1/
Chip not selected	H	H	X 2/	X	X	High Z
Write "L" in cell A_{xy} 3/	L	L	L	A_{xy}	L	High Z 4/
Write "H" in cell A_{xy}	L	L	H	A_{xy}	L	High Z 4/
Read data in cell A_{xy}	L	L	X	A_{xy}	H	Data (A_{xy})
$\overline{RAS}$ only refresh	L	H	X	A_x 5/	X	High Z
Hidden $\overline{RAS}$ only refresh	L	L	H	A_x	H	Data ($A_{x-N,y-N}$) 6/

NOTES:
1/ D_{OUT} is not inverted from D_{IN}.
2/ "X" = Don't care.
3/ A_{xy} denotes proper address logic to address cell A_{xy}.
4/ For "EARLY WRITE" timing, data out remains at high impedance. For "LATE WRITE" timing, data out is valid from access time to the beginning of a subsequent cycle, or until $\overline{CAS}$ goes to a high level.
5/ A_x depends only on A_0-A_6; A_7 is a don't care.
6/ When $\overline{CAS}$ = V_{IL}, the data output will contain data from the last valid read cycle (i.e., N cycles before).
7/ A 500 µs pause and eight initialization cycles required before truth table applies. All timing requirements shall be applied.

FIGURE 2. Truth table.

Read cycle timing

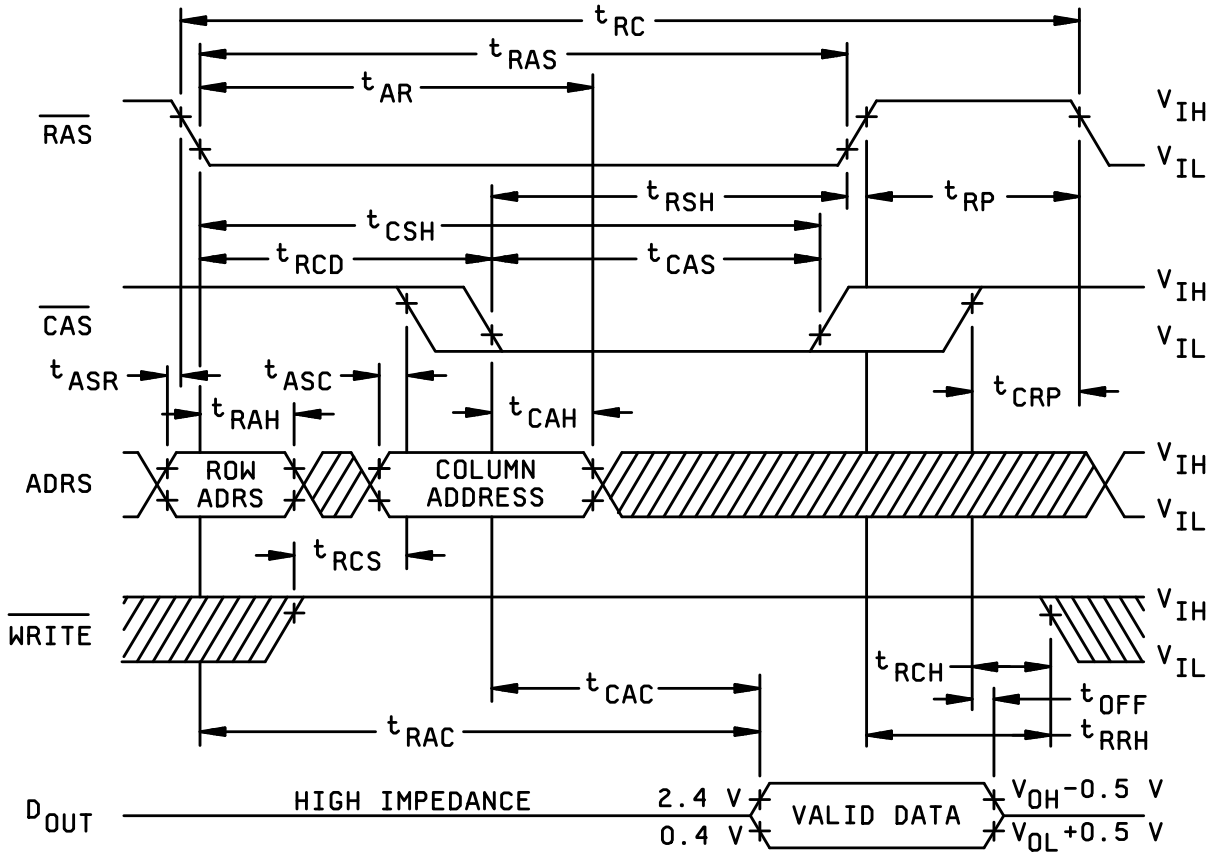


FIGURE 3. Switching waveforms.

Write cycle timing (Early write)

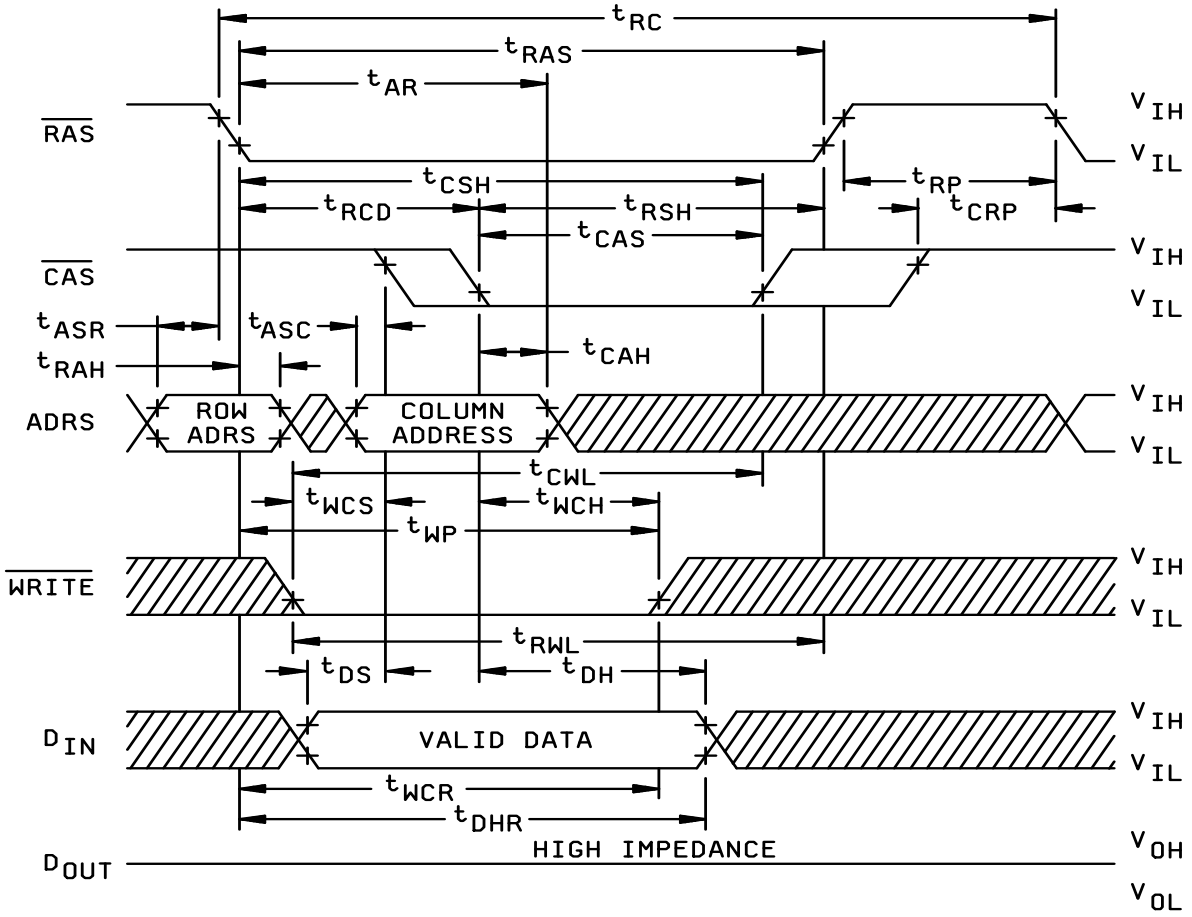


FIGURE 3. Switching waveforms - Continued.

Read/write - read/modify/write cycle

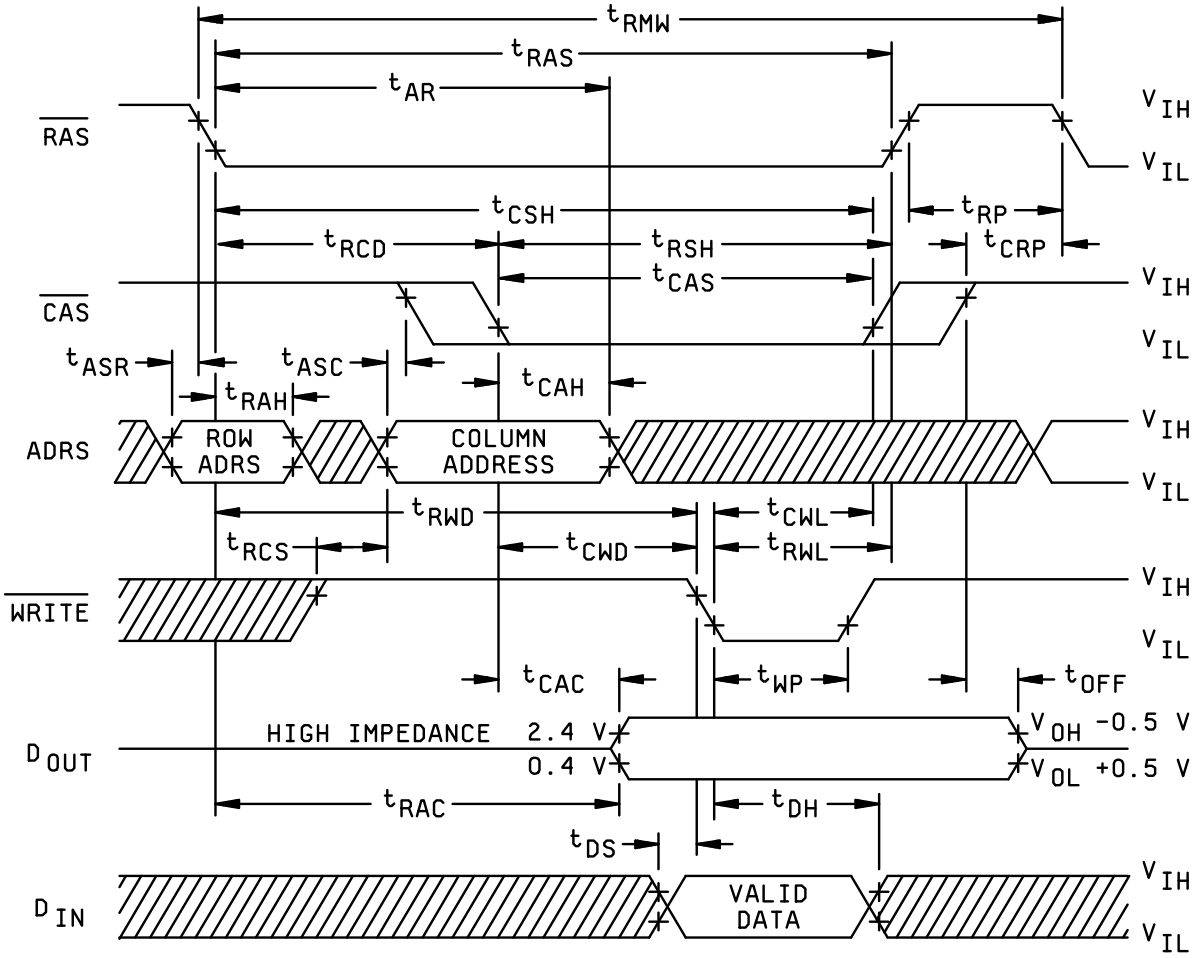
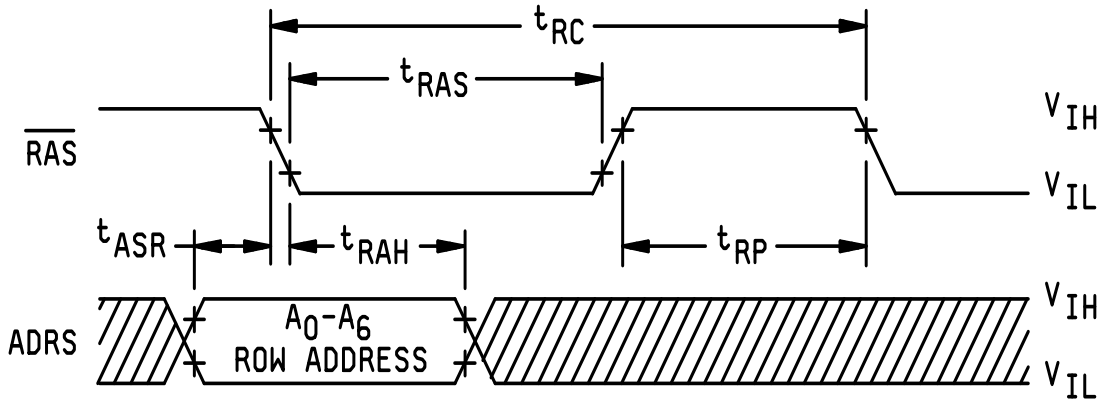


FIGURE 3. Switching waveforms - Continued.

$\overline{RAS}$ -Only refresh cycle



Notes:

1. $\overline{CAS}$ = V_{IH} ; $\overline{WRITE}$, D_{IN}, A_7 don't care.
2. D_{OUT} - high impedance.

FIGURE 3. Switching waveforms - Continued.

Page mode cycle timing

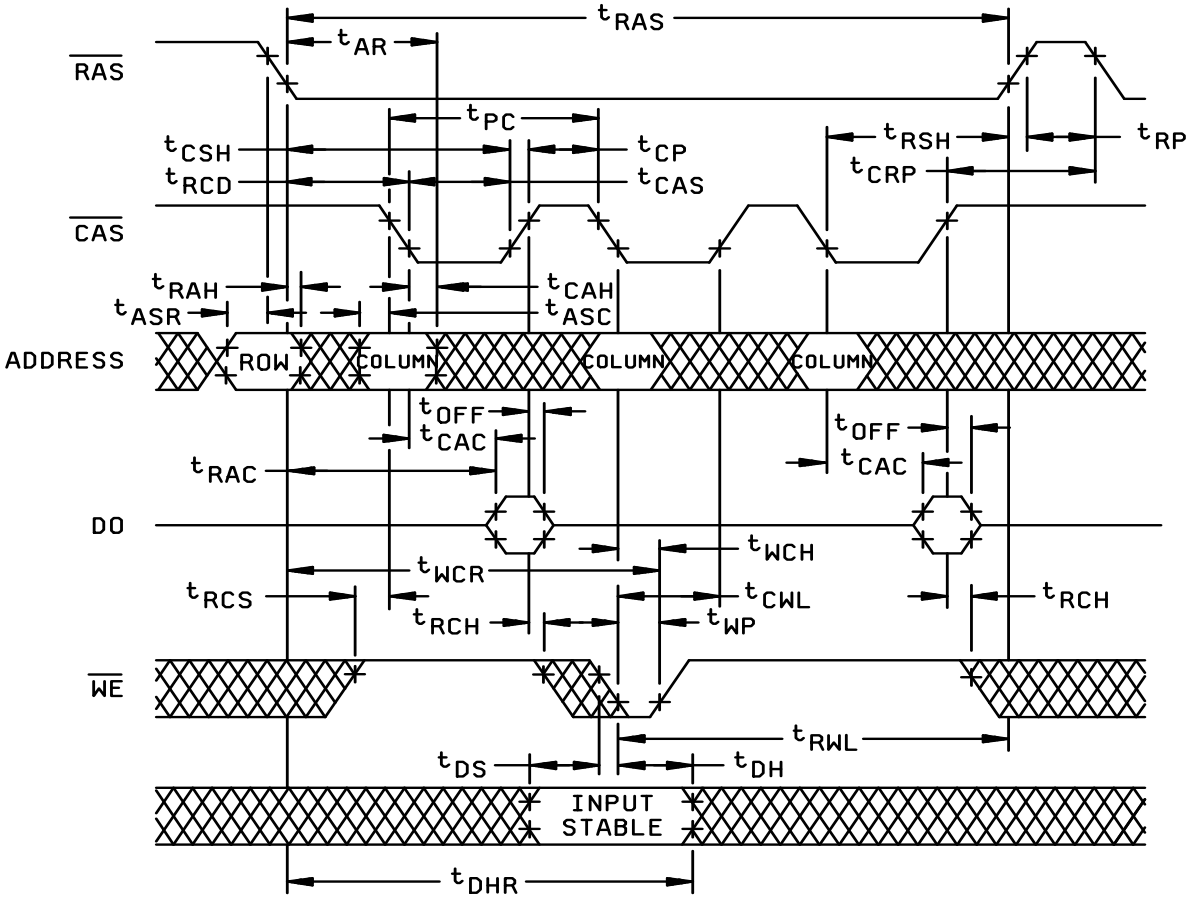


FIGURE 3. Switching waveforms - Continued.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_1, C_2 and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone 614-692-0540.

6.6 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-11-17

Approved sources of supply for SMD 82010 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Microcircuit drawing part number 1/	Vendor CAGE number	Vendor similar part number 2/
	3/	AM9064-15L/BEA
8201001EA	3/	MKB4564P-82
8201001ZA	3/	MKB4564E-82
	3/	AM9064-15L/BEA
8201002EA	3/	MKB4564P-82
8201002ZA	3/	MKB4564E-82
	3/	AM9064-20L/BEA
8201003EA	3/	MKB4564P-83
8201003ZA	3/	MKB4564E-83
8201004EA	3/	MT4264C-15
8201004ZA	3/	MT4264EC-15
8201005EA	3/	MT4264C-20
8201005ZA	3/	MT4264EC-20
8201006EA	3V146	4164-15JDS/BEA
	3/	AM9064-15L/BEA
	3/	SMJ4164-15JDS
8201006ZA	3/	SMJ4164-15FGS
	3V146	4164-15FGS/BZA
8201007EA	3V146	4164-20JDS/BEA
	3/	AM9064-20L/BEA
	3/	SMJ4164-20JDS
8201007ZA	3/	SMJ4164-20FGS
	3V146	4164-20FGS/BZA
8201008EA	3V146	4164-12JDS/BEA
	3/	SMJ4164-12JDS
8201008ZA	3/	SMJ4164-12FGS
	3V146	4164-12FGS/BZA
8201009EA	3/	AM9064-15L/BEA
8201010EA	3/	AM9064-20L/BEA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950