| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR MO DAY | APPROVED |
| E | Change to military drawing format. Add two new device types. Add vendor CAGE 61394. Add vendor for device types 01 and 02 in DIP only. | 87-06-29 | Michael A. Frye |
| F | Add the Z package to device types 08 and 09. Add vendor CAGE 61394 to devices 01ZX, 02ZX, 08ZX, AND 09ZX. Deleted vendor similar part number AM27128-45/BUA from devices 01ZX and 02ZX in paragraph 6.4. Changes to table I and table II. Also changes to recommend operating conditions and figure 2. Editorial changes throughout. | 88-11-01 | Michael A. Frye |
| G | Boilerplate updated to allow for alternative die/fabrication requirements. ksr | 02-09-05 | Raymond Monnin |
| H | Correction to marking paragraph 3.5. Update boilerplate paragraphs. ksr | 05-03-09 | Raymond Monnin |
| J | Updated boilerplate paragraphs, part of a five year review. ksr | 11-02-14 | Charles F. Saffle |

**CURRENT CAGE CODE 67268**

THE ORIGINAL FIRST SHEET OF THE DRAWING HAS BEEN REPLACED

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS OF SHEETS | REV | J | J | J | J | J | J | J | J | J | J | J | J | | |
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | |

PMIC N/A

PREPARED BY
James Jamison

**DLA LAND AND MARITIME**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael. A. Frye

DRAWING APPROVAL DATE
83 – 10 – 11

REVISION LEVEL
J

MICROCIRCUIT, MEMORY, DIGITAL, 16K X 8 UV ERASEABLE PROGRAMMABLE READ ONLY MEMORY (EPROM), MONOLITHIC SILICON

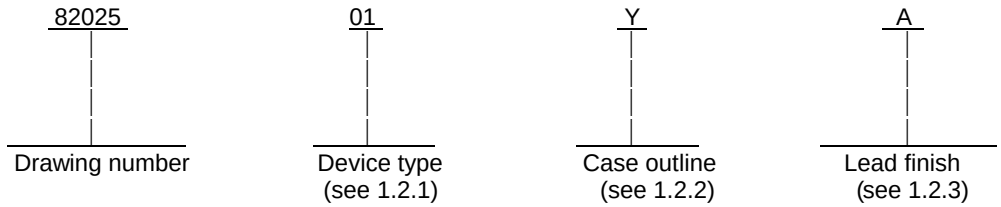
| SIZE | CAGE CODE | |
|---|---|---|
| A | **14933** | **82025** |

SHEET
1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:




1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit | Access |
|---|---|---|---|
| 01 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 450 ns |
| 02 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 250 ns |
| 03 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 200 ns |
| 04 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 300 ns |
| 05 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 250 ns |
| 06 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 150 ns |
| 07 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 110 ns |
| 08 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 200 ns |
| 09 | (see 6.4) | 16,384 x 8 - Bit UV EPROM | 300 ns |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style 1/ |
|---|---|---|---|
| Y | GDIP1-T28 and CDIP2-T28 | 28 | dual-in-line package |
| Z | CQCC1-N32 | 32 | rectangular chip carrier package |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 2/

Supply voltage ($V_{CC}$):
- Device types 01, 02, 08, 09 ..... -0.3 V dc to +7.0 V dc
- Device types 03 - 07 ..... -0.6 V dc to +6.0 V dc ±.25 V dc

Storage temperature range ..... -65°C to +150°C
Maximum power dissipation, ($P_D$) ..... 1.0 W
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature ($T_J$):
- Device types 01, 02, 08, 09 ..... +175°C
- Device types 03 - 07 ..... +150°C

Thermal resistance, junction-to-case ($\theta_{JC}$) ..... See MIL-STD-1835
All input or output voltages with respect to ground (device types 03 - 07) ..... -0.6 V dc to +6.25 V dc
Input voltage range:
- Device types 01, 02, 08, 09 ..... -0.3 V dc to +7.0 V dc

Endurance ..... 10,000 cycles/byte (minimum)
Data retention ..... 20 years (minimum)

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to $V_{SS}$.

1.4 Recommended operating conditions.

| | |
|---|---|
| Case operating temperature range | -55°C to +125°C |
| Input low voltage, $V_{IL}$ | -0.1 V dc to +0.8 V dc |
| Input high voltage, $V_{IH}$ | 2.0 V dc to $V_{CC}$ +1 V dc |
| Supply voltage ($V_{CC}$) | 4.5 V dc to 5.5 V dc |
| High level program input voltage $V_{IN}$(PR) | 21.0 V dc ±.5 V dc (devices 1,2,8, and 9) |
| High level program input voltage $V_{IN}$(PR) | 12.5 V dc ±.5 V dc (devices 3 – 7 ) |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). See 3.2.3.1 and 3.2.3.2

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroups 7 and 8) to verify that all bits are in proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification to DLA Land and Maritime-VA of change of product (see 6.3 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure. Margin test methods shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ and $C_O$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of five (5) devices with zero failures shall be required.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The device is erased by exposure to high intensity shortwave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm$^2$. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 shortwave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about one inch from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = -400 µA | $V_{CC}$ = 4.5 V | 1, 2, 3 | 01, 02, 08, 09 | 2.4 | | V |
| | | | $V_{CC}$ = 5.25 V | | 03 - 07 | | | |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 4.5 V | 1, 2, 3 | 01, 02, 08, 09 | | 0.4 | V |
| | | | $V_{CC}$ = 5.25 V | | 03 - 07 | | 0.45 | |
| Output leakage current (high) | $I_{OH}$ | $V_{CC}$ = 5.5 V 1/<br>$V_{OUT}$ = 5.5 V | | 1, 2, 3 | 01, 02, 08, 09 | | 10 | µA |
| | | | | | 03 - 07 | -10 | 10 | |
| Output leakage current (low) | $I_{OL}$ | $V_{CC}$ = 5.5 V 1/<br>$V_{OUT}$ = 0.1 V | | 1, 2, 3 | 01, 02, 08, 09 | | 10 | µA |
| | | | | | 03 - 07 | -10 | 10 | |
| High level input current | $I_{IH}$ | $V_{IN}$ = 5.5 V | $V_{CC}$ = 5.5 V | 1, 2, 3 | 01, 02, 08, 09 | | 1 | µA |
| | | | Outputs deselected<br>$V_{CC}$ = 5.25 V 2/ | | 03 - 07 | | 10 | |
| Low level input current | $I_{IL}$ | | $V_{CC}$ = 5.5 V<br>$V_{IN}$ = 0.1 V | 1, 2, 3 | 01, 02, 08, 09 | | -1 | µA |
| | | | Outputs deselected<br>$V_{CC}$ = 5.25 V<br>$V_{IN}$ = 0.4 V 2/ | | 03 - 07 | | -10 | |
| $V_{PP}$ read voltage | $V_{PP}$ | | | 1, 2, 3 | 01,02, 08,09 | $V_{CC}$ –0.7 | $V_{CC}$ +1 | V |
| | | | | | 03,04, 05,06, 07 | 4.5 | 5.5 | V |
| Input voltage low | $V_{IL}$ | $V_{CC}$ = 5.5 V 3/ | | 1, 2, 3 | All | -.1 | 0.8 | V |
| Input voltage high | $V_{IH}$ | $V_{CC}$ = 4.5 V 3/ | | 1, 2, 3 | All | 2.0 | 6.5 | V |
| $V_{PP}$ supply current read/standby 4/ | $I_{PP}$ | $V_{PP} = V_{CC}$ = 5.5 V | | 1, 2, 3 | All | | 5 | mA |
| Supply current (standby) | $I_{SB}$ | Outputs open<br>$\overline{CE} = V_{IH}$ | $V_{CC}$ = 5.5 V | 1, 2, 3 | 01, 02, 08, 09 | | 50 | mA |
| | | | $V_{CC}$ = 5.25 V | | 03 - 07 | | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | | Group A subgroups | Device type | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply current 2/ | $I_{CC}$ | Outputs open<br>$\overline{CE} = \overline{OE} = V_{IL}$ | $V_{CC}$ = 5.5 V | 1, 2, 3 | 01, 02, 08, 09 | | 150 | mA |
| | | | $V_{CC}$ = 5.25 V | | 03 - 07 | | 140 | |
| Input capacitance 2/ 5/ | $C_I$ | $V_{IN}$ = 0 V, f = 1 MHz<br>$T_C$ = +25°C | | 4 | All | | 10 | pF |
| Output capacitance 5/ | $C_O$ | | | | All | | 14 | pF |
| Address access time | $t_{AVQV}$<br>$t_{ACC}$ | $V_{CC}$ = 5.25 V<br>See figure 5<br>2/ 6/ | $\overline{CE} = \overline{OE} = V_{IL}$ | 9, 10, 11 | 01 | | 450 | ns |
| | | | | | 02, 05 | | 250 | |
| | | | | | 03, 08 | | 200 | |
| | | | | | 04, 09 | | 300 | |
| | | | | | 06 | | 150 | |
| | | | | | 07 | | 110 | |
| Output enable to high Z | $t_{DF}$<br>7/ | | $\overline{CE} = V_{IL}$ | | 01 | | 130 | ns |
| | | | | | 02, 08<br>09 | | 90 | |
| | | | | | 03 | | 65 | |
| | | | | | 04 | | 80 | |
| | | | | | 05 | | 65 | |
| | | | | | 06 | | 55 | |
| | | | | | 07 | | 45 | |
| Output hold from address change | $t_{OH}$<br>7/ | | $\overline{CE} = \overline{OE} = V_{IL}$ | | All | 0 | | ns |
| Chip enable access time | $t_{ELQV}$<br>$t_{CE}$ | | $\overline{OE} = V_{IL}$ | | 01 | | 450 | ns |
| | | | | | 02,05 | | 250 | |
| | | | | | 03,08 | | 200 | |
| | | | | | 04,09 | | 300 | |
| | | | | | 06 | | 150 | |
| | | | | | 07 | | 125 | |
| Output enable access time | $t_{OLQV}$<br>$t_{OE}$ | | $\overline{CE} = V_{IL}$ | | 01 | | 150 | ns |
| | | | | | 02,05 | | 100 | |
| | | | | | 03,08 | | 85 | |
| | | | | | 04,09 | | 110 | |
| | | | | | 06 | | 65 | |
| | | | | | 07 | | 55 | |

1/ Connect all address inputs and $\overline{OE}$ to $V_{IH}$ and measure $I_{OL}$ and $I_{OH}$ with the output under test connected to $V_{OUT}$.
2/ Outputs shall be loaded in accordance with figure 4.
3/ Tests for all input and control pins. $V_{IL}$ min and $V_{IH}$ max value are guaranteed, if not tested.
4/ $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP}$.
5/ All pins not being tested are to be grounded.
6/ Equivalent ac test conditions (actual load condition vary by tester).
Output load: 1 TTL gate and $C_L$ = 100 pF.
Input rise and fall times $\le$ 20 ns.
Input pulse levels: 0.4 V and 2.4 V.
Timing measurement reference levels:
Inputs = 1 V and 2 V.
Outputs = 0.8 V and 2 V.
7/ AC testing enable to three-state shall be tested initially and after any design changes.

| Device types | All | |
|---|---|---|
| Case outlines | Y | Z |
| Terminal number | Terminal symbol | |
| 1 | $V_{PP}$ | NC |
| 2 | A12 | $V_{PP}$ |
| 3 | A7 | A12 |
| 4 | A6 | A7 |
| 5 | A5 | A6 |
| 6 | A4 | A5 |
| 7 | A3 | A4 |
| 8 | A2 | A3 |
| 9 | A1 | A2 |
| 10 | A0 | A1 |
| 11 | O0 | A0 |
| 12 | O1 | NC |
| 13 | O2 | O0 |
| 14 | $V_{SS}$ | O1 |
| 15 | O3 | O2 |
| 16 | O4 | $V_{SS}$ |
| 17 | O5 | NC |
| 18 | O6 | O3 |
| 19 | O7 | O4 |
| 20 | $\overline{CE}$ | O5 |
| 21 | A10 | O6 |
| 22 | $\overline{OE}$ | O7 |
| 23 | A11 | $\overline{CE}$ |
| 24 | A9 | A10 |
| 25 | A8 | $\overline{OE}$ |
| 26 | A13 | NC |
| 27 | $\overline{PGM}$ | A11 |
| 28 | $V_{CC}$ | A9 |
| 29 | --- | A8 |
| 30 | --- | A13 |
| 31 | --- | $\overline{PGM}$ |
| 32 | --- | $V_{CC}$ |

FIGURE 1. Terminal connections.

Device types 03 through 07

| Mode/pins | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | $A_q$ | $V_{PP}$ | $V_{CC}$ | Outputs |
|---|---|---|---|---|---|---|---|
| Outside disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{CC}$ | $V_{CC}$ | $D_{OUT}$ |
| Standby | $V_{IH}$ | X | X | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Program inhibit | $V_{IL}$ | X | X | X | $V_{PP}$ | $V_{CC}$ | High Z |
| Program verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{OUT}$ |
| Intelligent identifiter | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_H$ | $V_{CC}$ | $V_{CC}$ | Code |
| Intelligent programming | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |

NOTES:
1. X means the input is a "don't care".
2. $V_H$ = 12 V ±0.5 V.

Device types 01, 02, 08, and 09

| Mode/pins | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | $V_{PP}$ | $V_{CC}$ | Outputs |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | $D_{OUT}$ |
| Outside disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | High Z |
| Standby | $V_{IH}$ | X | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{PP}$ | $V_{CC}$ | $D_{IN}$ |
| Program verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PP}$ | $V_{CC}$ | $D_{OUT}$ |
| Program inhibit | $V_{IH}$ | X | X | $V_{PP}$ | $V_{CC}$ | High Z |
| Silicon signature* (Intelligent identifiter) | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | Encoded Data |

NOTES:
1. X can be either $V_{IL}$ or $V_{IH}$.
2. *For silicon signature (tm) (intelligent identifier) A0 is toggled. A9 = 12 ±0.5 V, and all other addresses are at TTL low ($V_{IL}$).

FIGURE 2. Truth tables for unprogrammed devices.

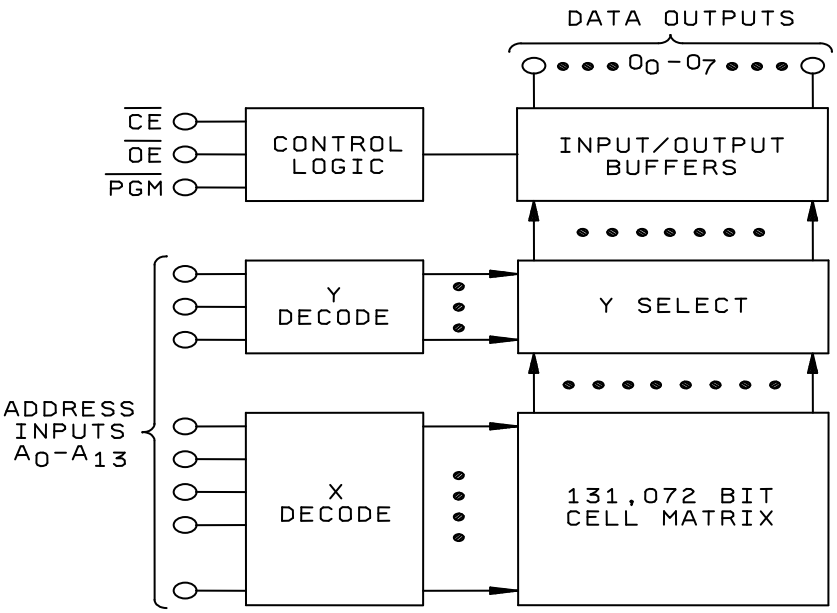



FIGURE 3. Logic diagram.

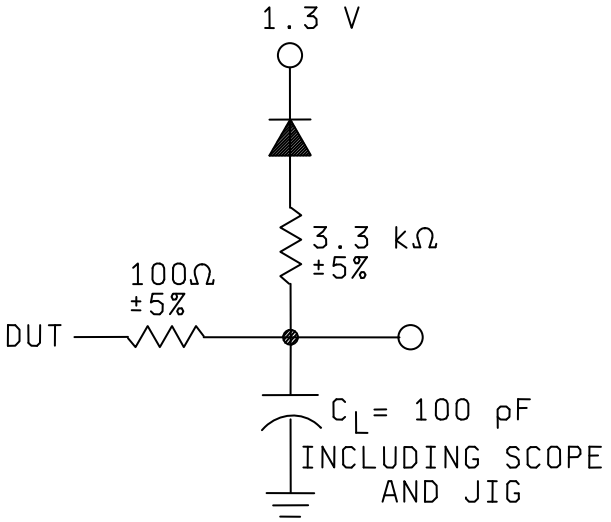
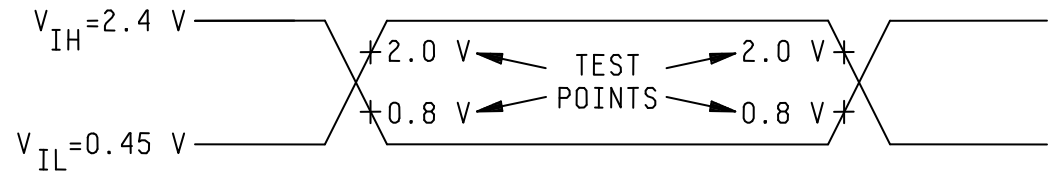
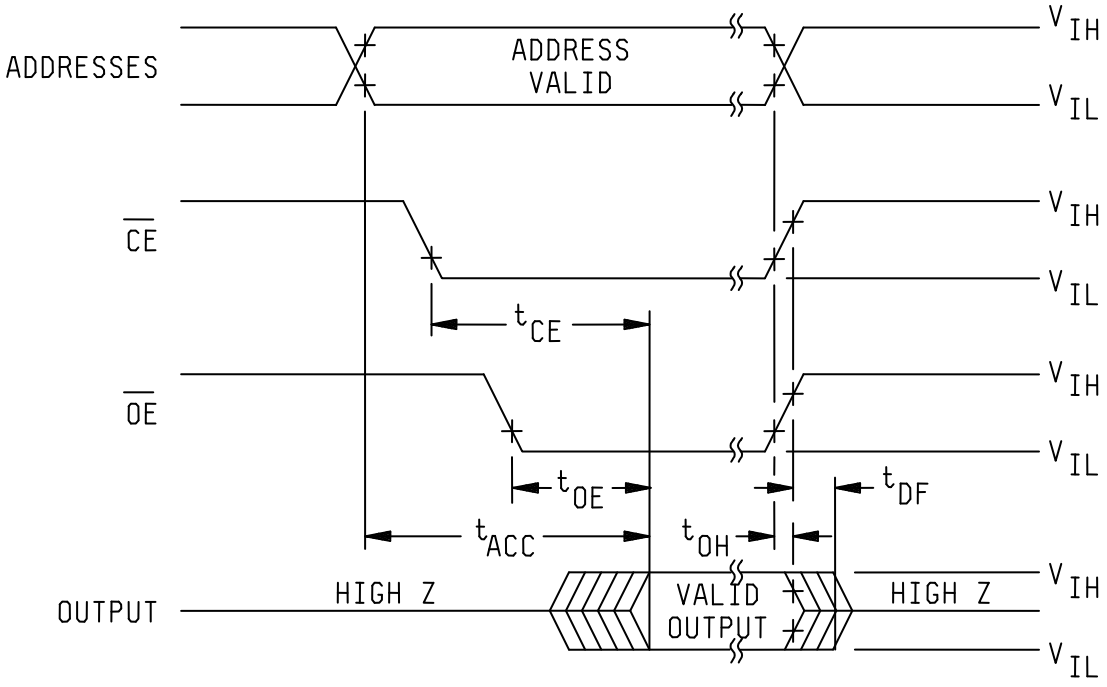



FIGURE 4. Output load (suggested).




NOTES:

1. $\overline{OE}$ may be delayed up to $t_{ACC}$ - $t_{OE}$ after falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

FIGURE 5. Timing diagram.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | - - - |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 2, 8 A, 10 |

1/ * PDA applies to subgroup 1.
2/ Any or all subgroup may be combined when using a high speed tester.
3/ Subgroup 7 and 8 shall consist of verifying the pattern specified.
4/ For all electrical tests, the device shall be programmed to the pattern specified.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-02-14

Approved sources of supply for SMD 82025 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 8202501YA | 3/ | DM27128-450 |
| 8202501ZA | 3/ | LM27128-450 |
| 8202502YA | 3/ | DM27128-250 |
| 8202502ZA | 3/ | LM27128-250 |
| 8202503YA | 3/ | MD27128A-20/B |
| | 3/ | AM27128A-20/BXA |
| | 3V146 | MC27128A-20/BYA |
| 8202503ZA | 3/ | AM27128A-20/BUA |
| | 3V146 | MR27128A-20/BZA |
| 8202504YA | 3/ | MD27128A-30/B |
| | 3/ | AM27128A-30/BXA |
| | 3V146 | MC27128A-30/BYA |
| 8202504ZA | 3/ | AM27128A-30/BUA |
| | 3V146 | MR27128A-30/BZA |
| 8202505YA | 3/ | MD27128A-25/B |
| | 3/ | AM27128A-25/BXA |
| | 3V146 | MC27128A-25/BYA |
| 8202505ZA | 3/ | AM27128A-25/BUA |
| | 3V146 | MR27128A-25/BZA |
| 8202506YA | 3/ | MD27128A-15/B |
| | 3V146 | MC27128A-15/BYA |
| 8202506ZA | 3V146 | MR27128A-15/BZA |

See notes at end of table.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 8202507YA | 3/<br>3V146 | MD27128A-11/B<br>MC27128A-11/BYA |
| 8202507ZA | 3V146 | MR27128A-11/BZA |
| 8202508YA | 3/ | DM27128-200 |
| 8202508ZA | 3/ | LM27128-200 |
| 8202509YA | 3/ | DM27128-300 |
| 8202509ZA | 3/ | LM27128-300 |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 3V146 | Rochester Electronics<br>10 Malcolm Hoyt Drive<br>Newburyport, MA. 01950 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.