REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert to military drawing format. Change drawing CAGE code to 67268. Add vendor CAGE 01295. Minor changes to table I and table II. Editorial changes throughout. Add device type 05	1987 OCT 13	M. A. Frye
D	Deleted CAGE 01295. Editorial changes throughout. Made technical changes to table I, margin test method C (step 4), paragraph 4.3.1 (step C), table II, figure 5, paragraph 4.2, margin test method B (step 3), paragraph 1.2.2, paragraph 1.3, paragraph 1.4, figure 6, and table III. Added footnote 3, removed vendor name and address under vendor name and address, and added M38510/22403BYX to 8411104YX.	1989 JAN 11	M. A. Frye
E	Convert to newer standard boilerplate with the additional of QD requirement paragraphs. Changed maximum C_I on table I from 6 pF to 10 pF and C_O from 12 pF to 15 pF. Changed subgroup 7 to 3 in Table II for Group C and D end-point electrical parameters. Updated boilerplate paragraphs. ksr	2004 NOV 08	Ray Monnin
F	Updated boilerplate paragraphs. glg	10-02-16	Charles Saffle

The original first page of this drawing has been replaced.

REV																				
SHEET																				
REV	F																			
SHEET	15																			

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A Frye

DRAWING APPROVAL DATE
18 October 1984

REVISION LEVEL
F

MICROCIRCUIT, MEMORY DIGITAL, 262,144-BIT (32K X 8) UV ERASEABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	84111

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

84111	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	27256-35	32K X 8-bit UV EPROM	350 ns
02	27256-25	32K X 8-bit UV EPROM	250 ns
03	27256-20	32K X 8-bit UV EPROM	200 ns
04	27256-17	32K X 8-bit UV EPROM	170 ns
05	27256-30	32K X 8-bit UV EPROM	300 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

Outline letter	Descriptive designator	Terminals	Package style
Y	GDIP1-T28 or CDIP2-T28	28	dual-in-line package 1/
Z	CQCC1-N32	32	rectangular chip carrier package 1/

1.3 Absolute maximum ratings.

Supply voltage (V_{CC}) 2/ ..... -0.6 V dc to +6.5 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 1.0 W
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C
All input or output voltages with respect to ground ..... -0.6 V dc to +6.5 V dc
Voltage on pin A_9 with respect to ground ..... -0.6 V dc to +13.5 V dc
V_{PP} supply voltage with respect to ground ..... -0.6 V dc to +13.0 V dc

1.4 Recommended operating conditions.

Case operating temperature range (T_C) ..... -55°C to +125°C
Input low voltage (V_{IL}) ..... -0.1 V dc to +0.8 V dc
Input high voltage (V_{IH}) ..... 2.0 V dc to V_{CC} +1 V dc
Supply voltage (V_{CC}) ..... 4.5 V dc to 5.5 V dc
High level program input voltage $V_{IN(PR)}$ ..... 12.5 V dc ±0.3 V dc (program method B)

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ All voltages referenced to V_{SS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. (This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.)

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram.. The block diagram shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the “5962-” on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. (For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.)

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.6.2).

(2) Bake, unbiased, for 12 hours at +200°C.

(3) Perform a margin test using $V_m = V_{CC} = 6.0$ V at +25°C using loose timing.

(4) Erase device, then program 45 to 50 percent of the bits to a worst case speed pattern.

(5) Perform dynamic burn-in (see 4.2a).

(6) Perform a margin test using $V_m = V_{CC} = 6.0$ V at +25°C.

(7) Perform 100 percent electrical testing at +25°C, +125°C and -55°C.

(8) Erase device (see 3.6.1), except devices submitted for groups A, B, C, and D.

(9) Verify erasure (see 3.6.3).

Margin test method B

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.6.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using $V_m = +6.0$ V at +25°C using loose timing (i.e., $t_{AVQV} = 1$ µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at $V_m = 6.0$ V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.6.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.6.3).

Margin test method C

I. Wafer margin test method:

(1) Program at +25°C with a greater than 95 percent pattern, (example, all "0's").

(2) Measure V_{CCMAX} and store in die signature row.

(3) Unbiased bake for 2 hours at +250°C.

(4) Test at +25°C. Measure V_{CCMAX} and compare to V_{CCMAX} store in die. Any die with a delta greater than 0.66 V constitutes a failure and is removed from the lot.

II. Back end margin test method:

(1) Program at +25°C with a greater than 95 percent pattern (example, all "0's") (see 3.6.2).

(2) Test at +25°C (8.0 V), V_{CCMAX} range (6.0 V). Measure and record V_{CCMAX} in signature row.

(3) Unbiased bake for 32 hours at +200°C.

(4) Test at +25°C (see I, step 4 above).

(5) Erase (see 3.6.1).

(6) Program at +25°C with a 50 percent pattern (example checkerboard bar) (see 3.6.2).

(7) Test at +25°C (see 3.6.3)

(8) Burn-in (see 4.2a).

(9) Test at +25°C (see 3.6.3).

(10) Test at +125°C (see 3.6.3).

(11) Test at -55°C (see 3.6.3).

(12) Erase (see 3.6.1). Devices may be submitted for groups A, B, C, and D testing at this point.

(13) Verify erasure at +25°C (see 3.6.3).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 5.50 V I_{OH} = -400 µA	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 5.50 V I_{OL} = 2.1 mA	1,2,3	All		0.45	V
Output leakage current	I_{OL}	V_{CC} = 5.5 V V_{OUT} = 5.5 V	1,2,3	All		10	µA
High level input current 1/	I_{IH}	V_{CC} = 5.50 V, Outputs deselected V_{IN} = 5.50 V	1,2,3	All		10	µA
V_{PP} supply current read/standby 2/	I_{PP}	V_{PP} = 5.5 V	1,2,3	All		5	mA
Supply current (standby)	I_{CC1}	V_{CC} = 5.50 V, $\overline{CE}$ = V_{IH} Outputs open	1,2,3	All		50	mA
Supply current 2/	I_{CC2}	V_{CC} = 5.50 V, $\overline{OE}$ = $\overline{CE}$ = V_{IL} O_0-O_7 = O mA	1,2,3	01, 02, 03, 05 04		125 140	mA
Input capacitance 1/	C_I	V_{IN} = 0 V, f = 1 MHz T_C = +25°C, see 4.3.1c	4	All		10	pF
Output capacitance	C_O	V_{OUT} = 0 V, f = 1 MHz T_C = +25°C, see 4.3.1c	4	All		15	pF
Address access time	t_{AVQV}	V_{CC} = 5.50 V 1/ see figure 4 $\overline{CE}$ = $\overline{OE}$ = V_{IL}	9,10,11	01 02 03 04 05		350 250 200 170 300	ns
Chip enable access time	t_{ELQV}	$\overline{OE}$ = V_{IL}	9,10,11	01 02 03 04 05		350 250 200 170 300	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C		Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output enable data on time	t_{OLQV}	V_{CC} = 5.50 V 1/ see figure 4	$\overline{CE}$ = V_{IL}	9,10,11	01		130	ns
					02		100	
					03		75	
					04		65	
					05		120	
Output enable to high Z	t_{EHQZ} 3/		$\overline{CE}$ = V_{IL}	9,10,11	01		110	ns
					02		60	
					03		55	
					04		55	
					05		105	
Output hold from address change	t_{AXQX} 3/		$\overline{CE}$ = $\overline{OE}$ =V_{IL}	9,10,11	All	0		ns

1/ Outputs shall be loaded per figure 5.

2/ V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC2} and I_{PP}.

3/ Tested initially and after any design changes.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurement) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

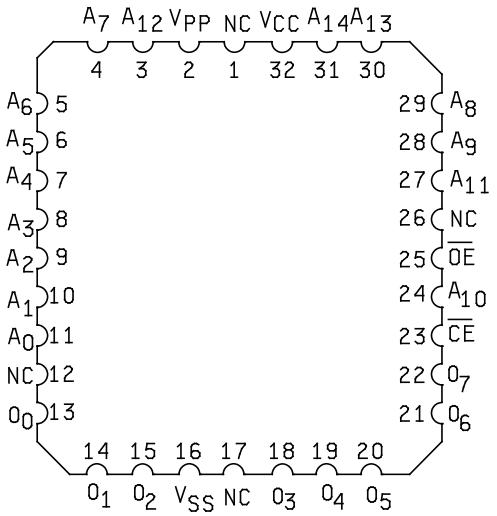
b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

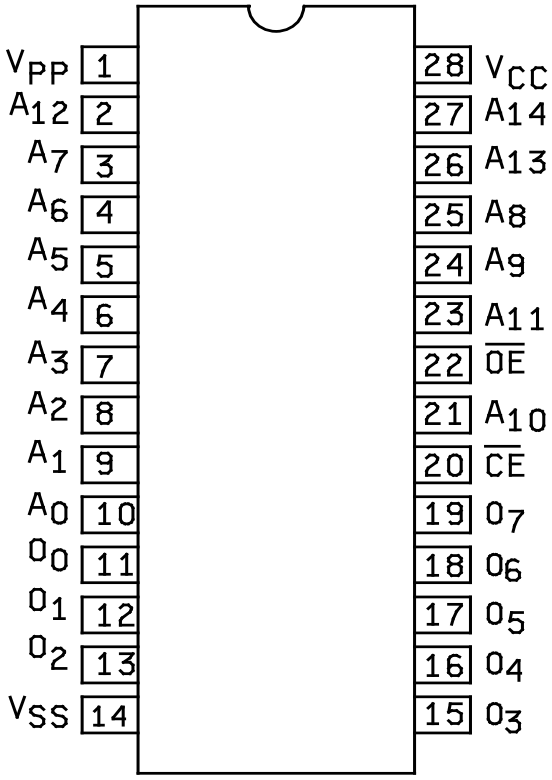
(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

CASE Z



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

CASE Y



Pin names

A_0 - A_{14}	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
O_{0-7}	Outputs

FIGURE 1. Terminal connections.

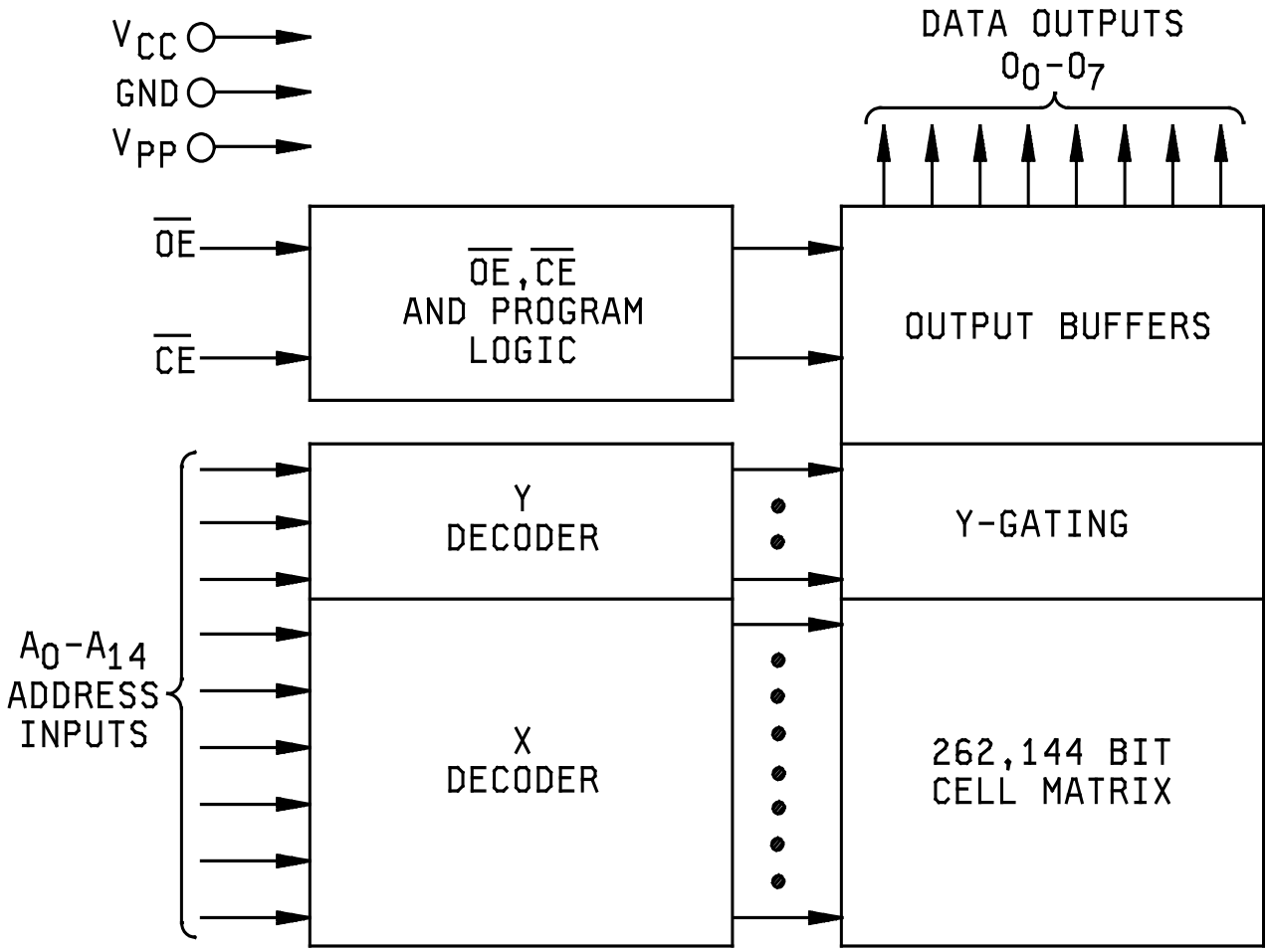
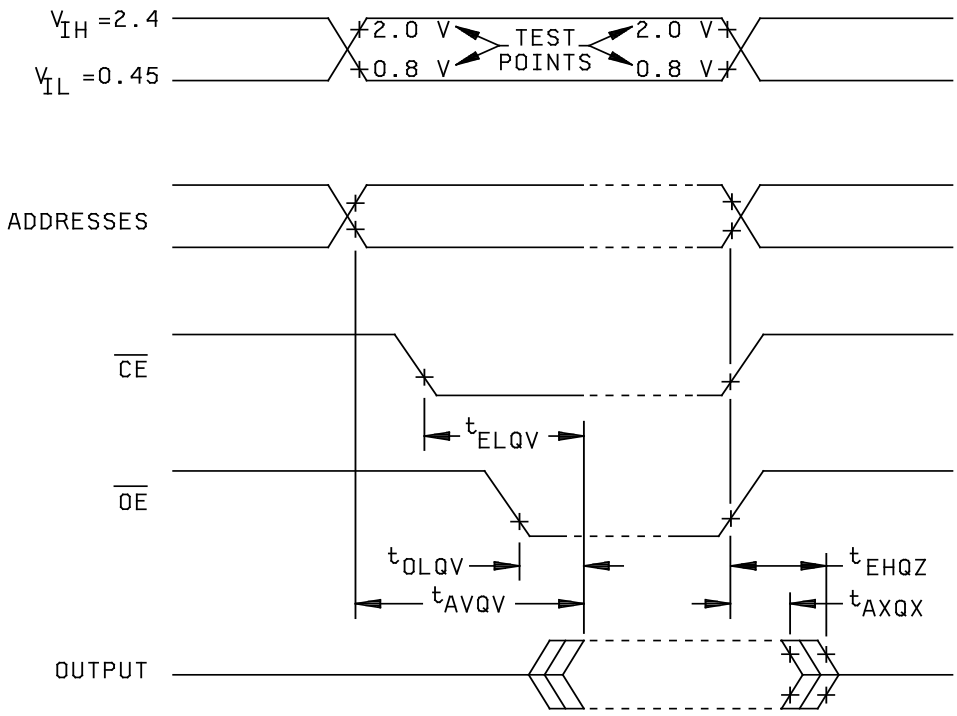


FIGURE 2. Block diagram.

Mode/pins	$\overline{CE}$	$\overline{OE}$	A_9	V_{PP}	V_{CC}	Outputs
Programming method	B	B	B	B	B	B
Deselect Output disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Program Verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Intelligent Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	V_{CC}	Code
Intelligent Programming	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}

NOTES:
1. It is recommended that verification for Method B devices be performed after the completion of programming all bytes.
2. X means the input is a "don't care".
3. Using the intelligent programming algorithm (Method B) allows the device to be programmed in a faster time.
4. $V_H = 12\ V \pm 0.5\ V$.

FIGURE 3. Truth table.



NOTES:

1. $\overline{OE}$ may be delayed up to t_{AVQV} - t_{OLQV} after falling edge of $\overline{CE}$ without impact on t_{AVQV}.
2. t_{EHQZ} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

FIGURE 4. Timing diagrams.

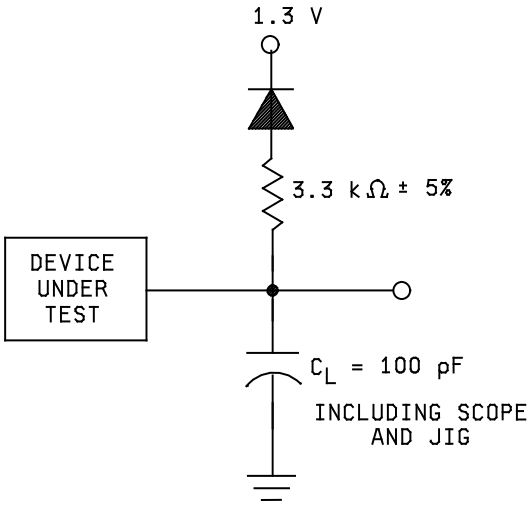


FIGURE 5. Output load circuit or equivalent

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	-----
Final electrical test parameters (method 5004)	1*, 2, 3, 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C and D end-point electrical parameters (method 5005)	1, 2, 3 or 2, 8(Hot), 10

1/ (*) Indicates PDA applies to subgroup 1 (see 4.2).
2/ Any or all subgroups may be combined when using a high speed tester.
3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.
4/ For all electrical tests, the device shall be programmed to the pattern specified.
5/ (**) See 4.3.1c.

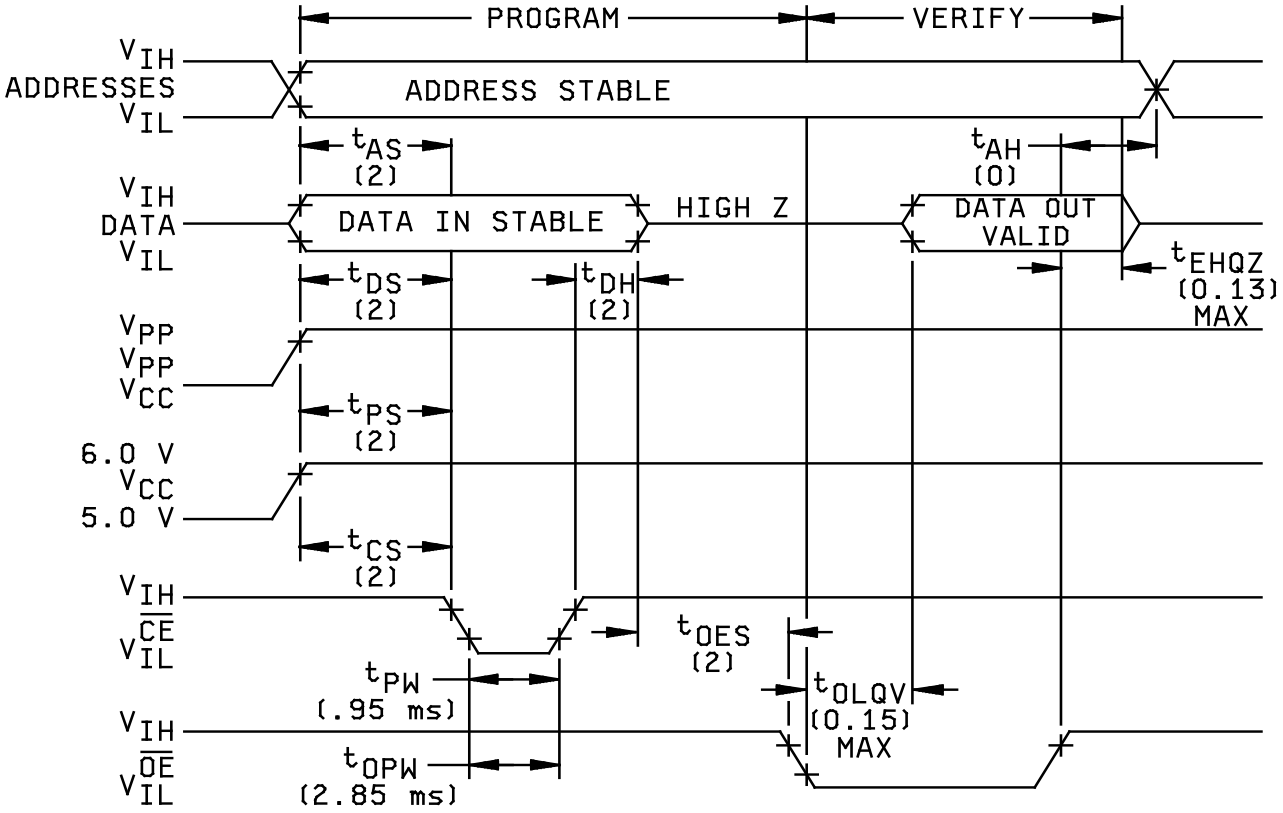
4.4 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm2. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedures for method B. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration for programming. The waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming low "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{PP} is 12.5 V +0.3 V and chip enable is brought low.



NOTES:
1. All times shown in parentheses are minimum and in μs unless otherwise specified.
2. The input and output timing reference level is 0.8 V for a V_{IL} and 2 V for V_{IH}.
3. t_{OLOV} and t_{EHQZ} are characteristics of the device but must be accommodated by the programmer.
4. When programming a 0.1 μF capacitor is required across V_{PP} and ground for suppression of spurious voltage transients which can damage the device.

FIGURE 6. Programming timing diagram for method B.

TABLE III. Programming characteristics for method B.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V T_A = +25°C	Limits		Unit
			Min	Max	
Input current (all inputs)	I_{IN}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low level (all inputs)	V_{IL}		-0.1	0.8	V
Input high level	V_{IH}		2.0	V_{CC}-1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			125	mA
V_{PP} supply current (program)	I_{PP}	$\overline{CE} = V_{IL}$		50	mA
A_9 intelligent identifier voltage	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{EHQZ}		0	130	ns
V_{PP} setup time	t_{PS}		2		µs

See footnotes at end of table.

TABLE III. Programming characteristics for method B - Continued.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V T_A = +25°C	Limits		Unit
			Min	Max	
V_{CC} setup time	t_{CS}		2		µs
$\overline{CE}$ initial program pulse width	t_{PW}	2/	0.95	1.05	ms
$\overline{CE}$ overprogram pulse width	t_{OPW}	3/	2.85	78.75	ms
Data valid from $\overline{OE}$	t_{OLQV}			150	ns

1/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2/ Initial program pulse width tolerance is 1 ms ±5%.
3/ The length of the overprogram pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-02-16

Approved sources of supply for SMD 84111 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Program Method	Margin Test method
8411101YA	3V146	MC27256-35/BYA	B	B
	3/	MD27256-35/B	B	B
	3/	AM27256-35/BXA	B	A
8411101ZA	3V146	MR27256-35/BZA	B	B
	3/	MR27256-35/B	B	B
	3/	AM27256-35/BUA	B	A
8411102YA	3V146	MC27256-25/BYA	B	B
	3/	MD27256-25/B	B	B
	3/	AM27256-25/BXA	B	A
	3/	SMJ27256-25JM	B	C
8411102ZA	3V146	MR27256-25/BZA	B	B
	3/	MR27256-25/B	B	B
	3/	AM27256-25/BUA	B	A
8411103YA	3V146	MC27256-20/BYA	B	B
	3/	MD27256-20/B	B	B
	3/	AM27256-20/BXA	B	A
	3/	SMJ27256-20JM	B	C
8411103ZA	3V146	MR27256-20/BZA	B	B
	3/	MR27256-20/B	B	B
	3/	AM27256-20/BUA	B	A
8411104YA	3V146	MC27256-17/BYA	B	B
	3/	MD27256-17/B	B	B
8411104ZA	3V146	MR27256-17/BZA	B	B
8411105YA	3/	SMJ27256-30JM	B	C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950