REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change case outline X to case outline Q. Add case outline Y. Delete group C programmability test and add margin test. Convert to military drawing format.	86-09-23	M. A. Frye
B	Add vendor CAGE 34335. Add device type 02. Change drawing CAGE number. Editorial changes throughout.	88-05-26	M. A. Frye
C	Changes made in accordance with NOR 5962-R038-93	92-12-09	Monica L. Poelking
D	Incorporated Revision C. Updated drawing to Q level. Updated boilerplate to MIL-PRF-38535 requirements. – LTG	01-12-03	Thomas M. Hess
E	Correct marking requirements in 3.5. Update boilerplate in accordance with MIL-PRF-38535 requirements. Editorial changes throughout. - PHN.	05-04-11	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED

REV																				
SHEET																				
REV	E	E	E	E	E															
SHEET	15	16	17	18	19															

REV STATUS	REV	E	D	E	E	D	D	D	D	D	D	D	D	D	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Ray Monnin

APPROVED BY

Michael A. Frye

DRAWING APPROVAL DATE

85-06-24

MICROCIRCUIT, DIGITAL, N-CHANNEL, MOS 8-BIT MICROCOMPUTER WITH 32 K-BIT UVEPROM, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
E	A	**67268**	**84190**

SHEET 1 OF 19

DSCC FORM 2233
APR 97

5962-E245-05

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

84190	01	Q	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	8751H-8	8.0 MHz max	8-bit microcomputer with 32 K bit UVEPROM
02	8751H	12.0 MHz max	8-bit microcomputer with 32 K bit UVEPROM

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line package
Y	CQCC1-N44	44	Square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage on any pin (except V_{PP}) 2/ ..... -0.5 V dc to +7.0 V dc
Voltage (V_{PP}) ..... 21.5 V dc
Power dissipation (P_D) ..... 2.0 W
Storage temperature range ..... -65°C to +150°C
Junction temperature (T_J) ..... +165°C
Lead temperature (soldering, 5 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}):
Cases Q and Y ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 4.5 V dc to 5.5 V dc
Program voltage (V_{PP}) ..... 21.0 V dc $\pm$0.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to V_{SS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Programmed EPROM device. The requirements for supplying programmed EPROM devices are not part of this drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.10.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that al bits are in the proper state. Any bit that does not verify to be the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1, 2, 3	All		0.7	V
Input high voltage (except XTAL2, RST)	V_{IH}		1, 2, 3	All	2.2		V
Input high voltage to XTAL2, RST	V_{IH1}	XTAL1 = V_{SS}	1, 2, 3	All	2.5		V
Output low voltage ports 1, 2, 3	V_{OL}	I_{OL} = 1.2 mA	1, 2, 3	All		0.45	V
Output low voltage port 0 ALE, PSEN	V_{OL1}	I_{OL} = 2.8 mA	1, 2, 3	All		0.60	V
		I_{OL} = 2.4 mA				0.45	
Output high voltage ports 1, 2, 3	V_{OH}	I_{OH} = -60 µA	1, 2, 3l	All	2.4		V
Output high voltage port 0 (in external bus mode), ALE, PSEN	V_{OH1}	I_{OH} = -300 µA	1, 2, 3	All	2.4		V
Logical 0 input current P1, P2, P3	I_{IL}	V_{IN} = 0.45 V	1, 2, 3	All		-500	µA
Logical 0 input current to EA/V_{PP}	I_{IL1}	V_{IN} = 0.45 V	1, 2, 3	All		-15	mA
Logical 0 input current to XTAL2	I_{IL2}	XTAL1 = V_{SS}, V_{IN} = 0.45 V	1, 2, 3	All		-4.5	mA
Input leakage current to port 0	I_{LI}	0.45 V < V_{IN} < V_{CC}	1, 2, 3	All		±125	µA
Logical input current to EA/V_{PP}	I_{IH}	V_{IN} = 2.4 V	1, 2, 3	All		500	µA
Input current to RST/V_{PD} to activate reset	I_{IH1}	V_{IN} < (V_{CC} –1.5 V)	1, 2, 3	All		500	µA
Power supply current	I_{CC}	All outputs disconnected, EA = V_{CC}	1, 2, 3	All		275	mA
Capacitance of I/O buffers	$C_{I/O}$	fc = 1 MHz, T_C = +25°C See 4.3.1c	4	All		30	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Limits 2/		Unit
					Min	Max	Min	Max	
Oscillator period	t_{CLCL}	C_L (Port 0, ALE, $\overline{PSEN}$) = 100 pF C_L (all others) = 80 pF f_{MAX} = 8 MHz device 01 f_{MAX} = 12 MHz device 02 See figures 3 and 4 4/	9, 10, 11	01	125	286	t_{CLCL}	t_{CLCL}	ns
				02	83	286	t_{CLCL}	t_{CLCL}	
High time 1/ 3/	t_{CHCX}		9, 10, 11	All	20		20		ns
Low time 1/ 3/	t_{CLCX}		9, 10, 11	All	20		20		ns
Rise time 1/ 3/	t_{CLCH}		9, 10, 11	All		20		20	ns
Fall time 1/ 3/	t_{CHCL}		9, 10, 11	All		20		20	ns
ALE pulse width	t_{LHLL}		9, 10, 11	01	195		$2t_{CLCL}$ -55		ns
				02	112		$2t_{CLCL}$ -55		
Address valid to ALE	t_{AVLL}		9, 10, 11	01	70		t_{CLCL} -55		ns
				02	28		t_{CLCL} -55		
Address hold after ALE	t_{LLAX}		9, 10, 11	01	75		t_{CLCL} -50		ns
				02	33		t_{CLCL} -50		
ALE to valid instr in	t_{LLIV}		9, 10, 11	01		335		$4t_{CLCL}$ -165	ns
				02		168		$4t_{CLCL}$ -165	
ALE to $\overline{PSEN}$	t_{LLPL}		9, 10, 11	01	85		t_{CLCL} -40		ns
				02	43		t_{CLCL} -40		
$\overline{PSEN}$ pulse width	t_{PLPH}		9, 10, 11	01	300		$3t_{CLCL}$ -75		ns
				02	175		$3t_{CLCL}$ -75		
$\overline{PSEN}$ to valid instr in	t_{PLIV}		9, 10, 11	01		210		$3t_{CLCL}$ -165	ns
				02		85		$3t_{CLCL}$ -165	
Input instr hold after PSEN	t_{PXIX}		9, 10, 11	All	0		0		ns
Input instr float after PSEN 1/	t_{PXIZ}		9, 10, 11	01		90		t_{CLCL} -35	ns
				02		48		t_{CLCL} -35	
$\overline{PSEN}$ to address valid	t_{PXAV}		9, 10, 11	01	100		t_{CLCL} -25		ns
				02	58		t_{CLCL} -25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device type	Limits		Limits 2/		Unit
					Min	Max	Min	Max	
Address to valid instr in	t_{AVIV}	C_L (Port 0, ALE, $\overline{PSEN}$) = 100 pF C_L (all others) = 80 pF f_{MAX} = 8 MHz device 01 f_{MAX} = 12 MHz device 02 See figures 3 and 4 4/	9, 10, 11	01		460		$5t_{CLCL}$ -165	ns
				02		252		$5t_{CLCL}$ -165	
Address float to PSEN 1/	t_{AZPL}		9, 10, 11	All	0		0		ns
$\overline{RD}$ pulse width	t_{RLRH}		9, 10, 11	01	650		$6t_{CLCL}$ -100		ns
				02	400		$6t_{CLCL}$ -100		
$\overline{WR}$ pulse width	t_{WLWH}		9, 10, 11	01	650		$6t_{CLCL}$ -100		ns
				02	400		$6t_{CLCL}$ -100		
Address hold after ALE	t_{LLAX}		9, 10, 11	01	75		t_{CLCL} -50		ns
				02	33		t_{CLCL} -50		
$\overline{RD}$ to valid data in	t_{RLDV}		9, 10, 11	01		440		$5t_{CLCL}$ -185	ns
				02		232		$5t_{CLCL}$ -185	
Data hold after $\overline{RD}$	t_{RHDX}		9, 10, 11	All	0		0		ns
Data float after $\overline{RD}$ 1/	t_{RHDZ}		9, 10, 11	01		165		$2t_{CLCL}$ -85	ns
				02		82		$2t_{CLCL}$ -85	
ALE to valid data in	t_{LLDV}		9, 10, 11	01		830		$8t_{CLCL}$ -170	ns
				02		496		$8t_{CLCL}$ -170	
Address to valid data in	t_{AVDV}		9, 10, 11	01		940		$9t_{CLCL}$ -185	ns
				02		565		$9t_{CLCL}$ -185	
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}		9, 10, 11	01	310	440	$3t_{CLCL}$ -65	$3t_{CLCL}$ +65	ns
				02	185	315	$3t_{CLCL}$ -65	$3t_{CLCL}$ +65	
Address to $\overline{WR}$ or RD	t_{AVWL}		9, 10, 11	01	355		$4t_{CLCL}$ -145		ns
				02	188		$4t_{CLCL}$ -145		
Data valid to $\overline{WR}$ transition	t_{QVWX}		9, 10, 11	01	40		t_{CLCL} -85		ns
				02	0		t_{CLCL} -85		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device type	Limits		Limits 2/		Unit
					Min	Max	Min	Max	
Data setup to WR high	t_{QVWH}	C_L (Port 0, ALE, $\overline{PSEN}$) = 100 pF C_L (all others) = 80 pF f_{MAX} = 8 MHz device 01 f_{MAX} = 12 MHz device 02 See figures 3 and 4 4/	9, 10, 11	01	800		$7t_{CLCL}$ -75		ns
				02	508		$7t_{CLCL}$ -75		
Data held after WR	t_{WHQX}		9, 10, 11	01	60		t_{CLCL} -65		ns
				02	18		t_{CLCL} -65		
$\overline{RD}$ low to address float 1/	t_{RLAZ}		9, 10, 11	All	0		0		ns
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		9, 10, 11	01	60	190	t_{CLCL} -65	t_{CLCL} +65	ns
				02	18	148	t_{CLCL} -65	t_{CLCL} +65	

1/ Tested only initially and after any design changes.

2/ Variable oscillator equations provided for design purposes.

3/ Required external clock drive characteristics (XTAL2).

4/ AC testing: Inputs are driven at 2.4 V for a logic “1” and 0.45 V for a logic “0”. Timing measurements are made at 2.0 V for a logic “1” and 0.8 V for a logic “0”.

Device types	All		
Case outline	Q		
Terminal numbers	Terminal symbols	Terminal numbers	Terminal symbols
1	P1.0	21	P2.0
2	P1.1	22	P2.1
3	P1.2	23	P2.2
4	P1.3	24	P2.3
5	P1.4	25	P2.4
6	P1.5	26	P2.5
7	P1.6	27	P2.6
8	P1.7	28	P2.7
9	RST	29	$\overline{\text{PSEN}}$
10	P3.0/RXD	30	ALE/$\overline{\text{PROG}}$
11	P3.1/TXD	31	$\overline{\text{EA}}/V_{PP}$
12	P3.2/$\overline{\text{INT0}}$	32	P0.7
13	P3.3/$\overline{\text{INT1}}$	33	P0.6
14	P3.4/T0	34	P0.5
15	P3.5/T1	35	P0.4
16	P3.6/$\overline{\text{WR}}$	36	P0.3
17	P3.7/$\overline{\text{RD}}$	37	P0.2
18	XTAL2	38	P0.1
19	XTAL1	39	P0.0
20	V_{SS}	40	V_{CC}

FIGURE 1. Terminal connections.

Device types	All		
Case outline	Y		
Terminal numbers	Terminal symbols	Terminal numbers	Terminal symbols
1	NC	23	NC
2	P1.0	24	P2.0
3	P1.1	25	P2.1
4	P1.2	26	P2.2
5	P1.3	27	P2.3
6	P1.4	28	P2.4
7	P1.5	29	P2.5
8	P1.6	30	P2.6
9	P1.7	31	P2.7
10	RST	32	$\overline{\text{PSEN}}$
11	P3.0/RXD	33	ALE/$\overline{\text{PROG}}$
12	NC	34	NC
13	P3.1/TXD	35	$\overline{\text{EA}}/V_{PP}$
14	P3.2/$\overline{\text{INT0}}$	36	P0.7
15	P3.3/$\overline{\text{INT1}}$	37	P0.6
16	P3.4/T0	38	P0.5
17	P3.5/T1	39	P0.4
18	P3.6/$\overline{\text{WR}}$	40	P0.3
19	P3.7/$\overline{\text{RD}}$	41	P0.2
20	XTAL2	42	P0.1
21	XTAL1	43	P0.0
22	V_{SS}	44	V_{CC}

NC = No connection

FIGURE 1. Terminal connections – Continued.

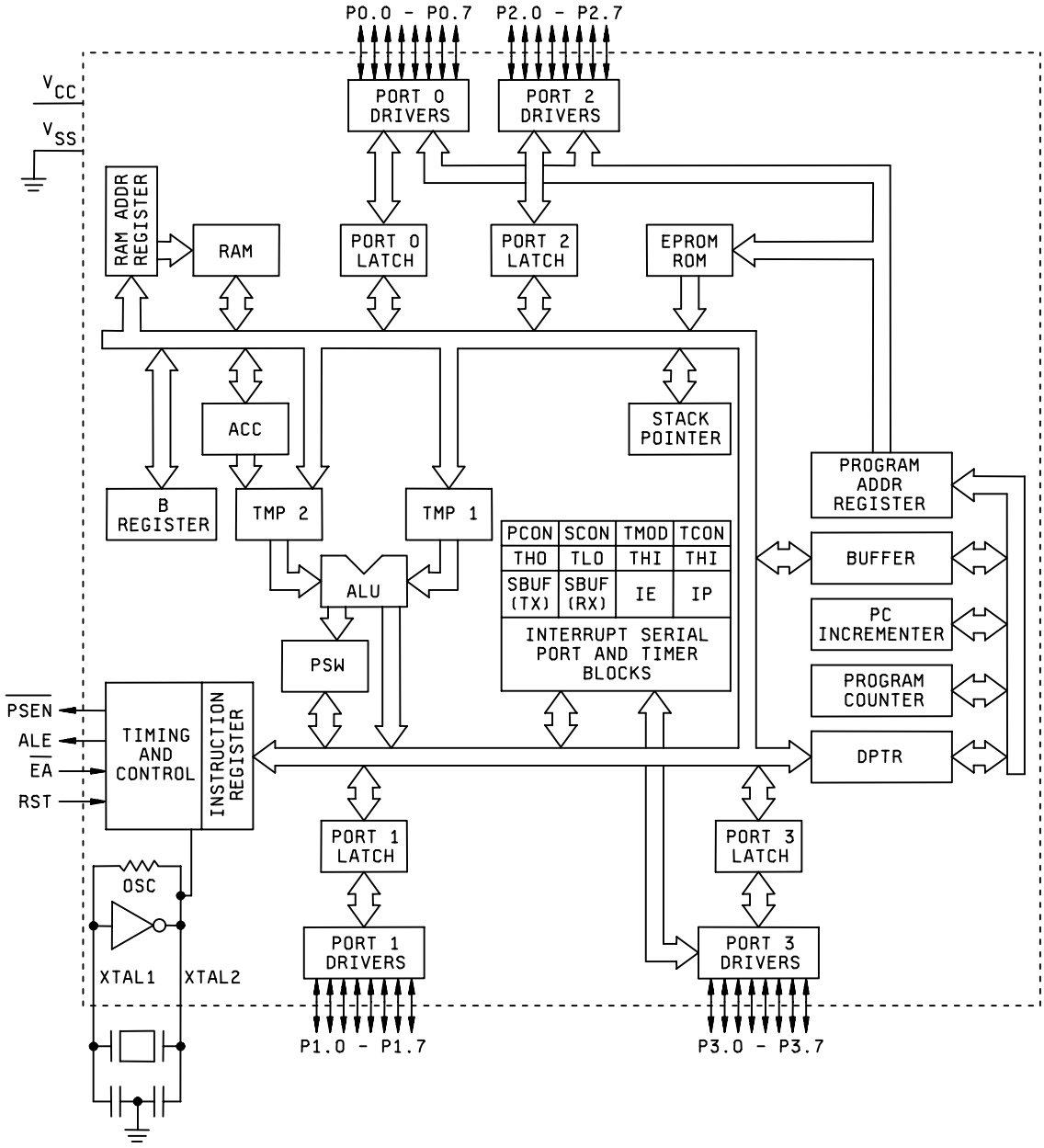


FIGURE 2. Block diagram.

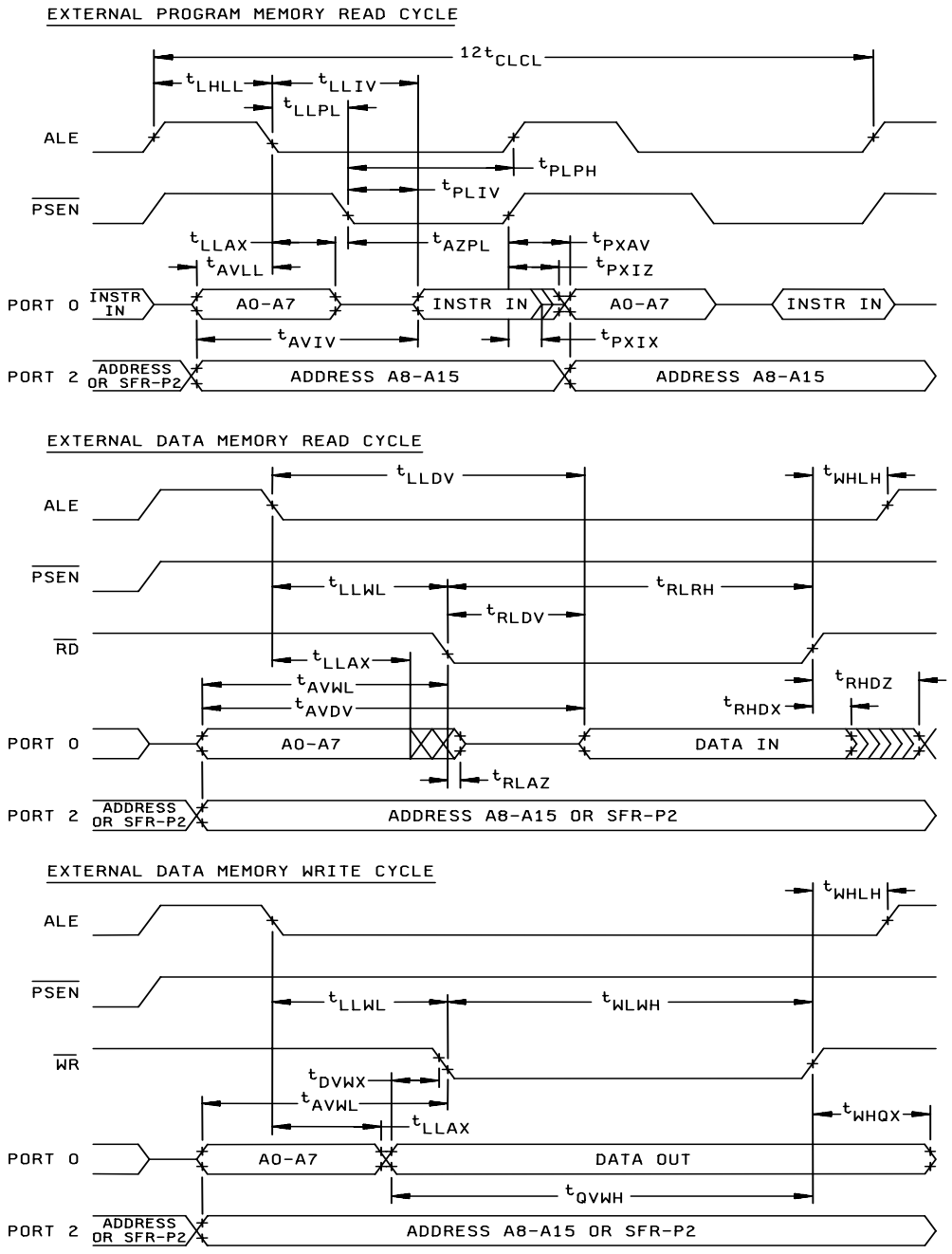


FIGURE 3. AC timing circuits.

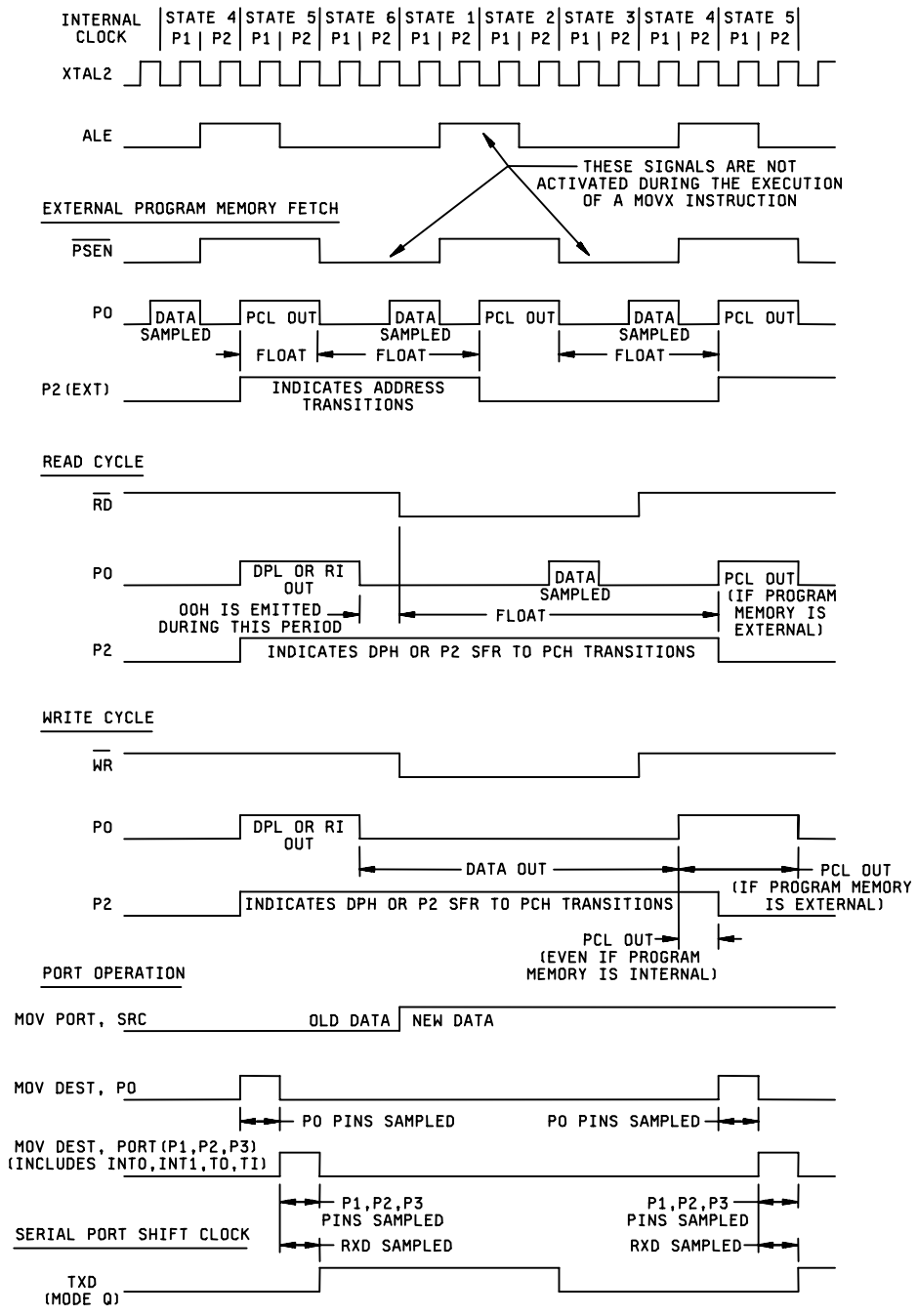
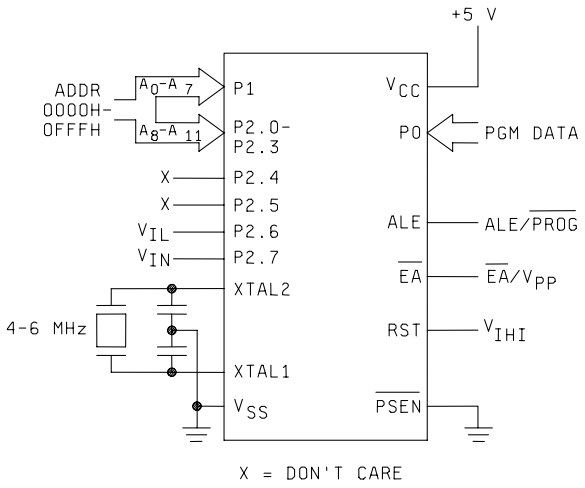


FIGURE 4. Clock waveforms.

PROGRAMMING



X = DON'T CARE

PROGRAM VERIFICATION

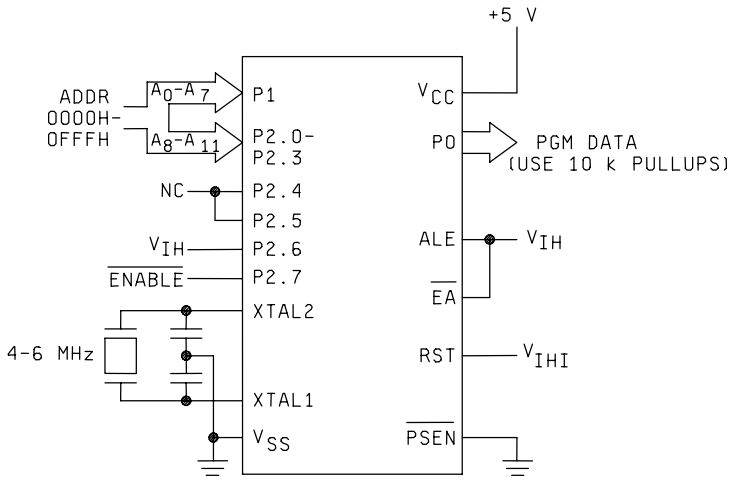


FIGURE 5. Programming logic.

SECURITY BIT PROGRAMMING

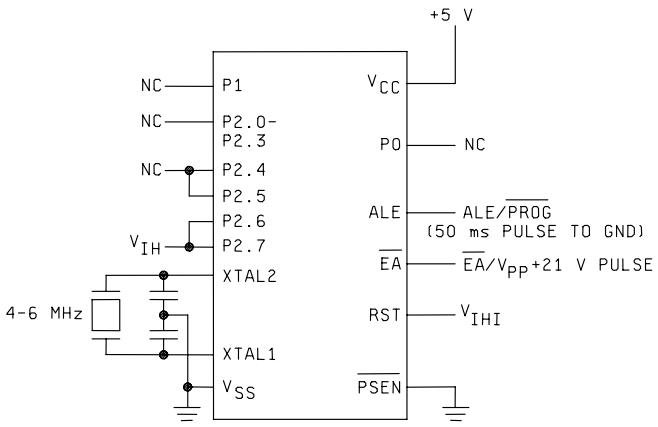


FIGURE 5. Programming logic – Continued.

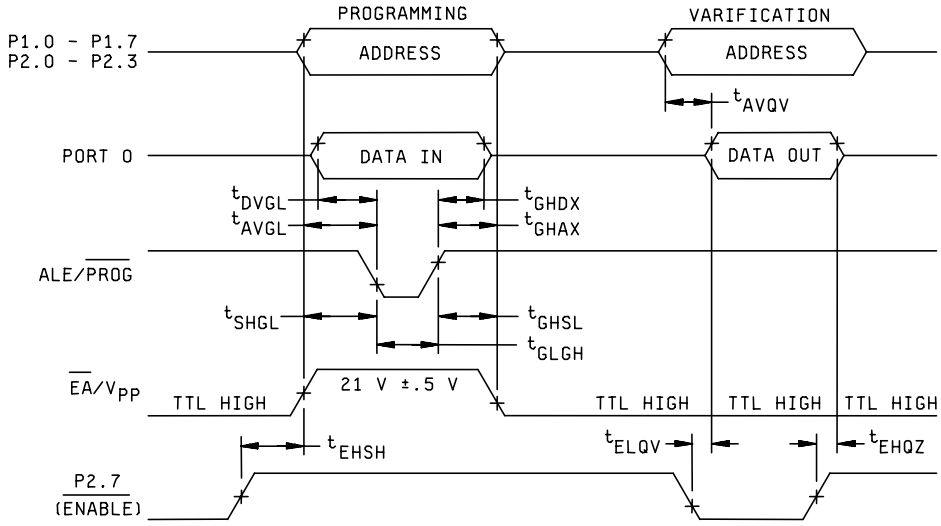


FIGURE 6. Programming waveforms

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.10.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using Vm = +5.9 V at +25°C using loose timing (i.e., T_{ACC} = 1 μs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at Vm = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.10.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero failures shall be required.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified and the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved source of supply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I) 1/ 2/ 3/ 4/
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10 or 1, 2, 3

1/ * PDA applies to subgroup 1.
2/ Any or all subgroups may be combined when using a high speed tester.
3/ Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified and the instruction set.
4/ For all electrical tests, the device shall be programmed to the pattern specified (see 4.3.1d)* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 mm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch from the lamp tubes. After erasures, all bits are in the high state.

4.5 Programming procedures for method A. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration (see figure 5) for programming the waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high “H” state. Information is introduced by selectively programming “L” into the desired bit locations. A programmed “L” can be changed to an “H” by ultraviolet light erasure (see 4.4).

TABLE III. Programming characteristics.

Parameter	Symbol	Conditions	Min	Max	Units
Programming supply voltage	V_{PP}	V_{CC} = 5.0 V ±10% T_C = +25°C	20.5	21.5	V
Programming current	I_{PP}			30.0	mA
Oscillator frequency	$1/t_{CLCL}$		4.0	6.0	MHz
$\overline{\text{PROG}}$ Address setup to	t_{AVGL}		$48t_{CLCL}$		ns
$\overline{\text{PROG}}$ Address hold after	t_{GHAX}		$48t_{CLCL}$		ns
$\overline{\text{PROG}}$ Data setup to	t_{DVGL}		$48t_{CLCL}$		ns
$\overline{\text{PROG}}$ Data hold after	t_{GHDX}		$48t_{CLCL}$		ns
$\overline{\text{ENABLE}}$ high to V_{PP}	t_{EHSH}		$48t_{CLCL}$		ns
V_{PP} setup to $\overline{\text{PROG}}$	t_{SHGL}		10.0		µs
V_{PP} hold after $\overline{\text{PROG}}$	t_{GHSL}		10.0		µs
$\overline{\text{PROG}}$ width	t_{GLGH}		45.0	55.0	ms
Address to data valid	t_{AVQV}			$48t_{CLCL}$	ns
$\overline{\text{ENABLE}}$ to data valid	t_{ELQV}			$48t_{CLCL}$	ns
Data float after $\overline{\text{ENABLE}}$	t_{EHQZ}		0	$48t_{CLCL}$	ns

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Symbols, definitions, and functional descriptions. The symbol, definitions, and functional description for this device shall be as follows:

Port 0 — Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory. It also receives the instruction bytes during EPROM programming, and outputs instruction bytes during program verification. (External pull-ups are required during program verification). Port 0 can sink (and in bus operations can source) eight LS TTL inputs.

Port 1 — Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during EPROM programming and program verification. Port 1 can sink/source four LS TTL inputs.

Port 2 — Port 2 is an 8-bit bidirectional I/O port with internal pullups. It emits the high-order address byte during accesses to external memory. It also receives the high-order address bits during EPROM programming and program verification. Port 2 can sink/source four LS TTL inputs.

Port 3 — Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features as listed below:

Port pin	Alternate function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt)
P3.3	INT1 (external interrupt)
P3.4	T0 (timer/counter 0 external input)
P3.5	T1 (timer/counter 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 can sink/source four LS TTL inputs

RST — A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor (8.2 kΩ) from RST to V_{SS} permits power-on reset when a capacitor (10 μF) is also connected from this pin to V_{CC}.

ALE/$\overline{\text{PROG}}$ — Address latch enable output for latching the low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming.

$\overline{\text{PSEN}}$ — Program store enable output is the read strobe to external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external program memory. (However, even when executing out of external program memory two activations of PSEN are skipped during each access to external data memory). $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. PSEN can sink/source 8 LS TTL inputs.

$\overline{\text{EA}}/V_{PP}$ — When $\overline{\text{EA}}$ is held high, the device executes out of internal program memory (unless the program counter exceeds 0FFFH). When EA is held low, the device executes only out of external program memory. This pin also receives the 21 V programming supply voltage (V_{PP}) during EPROM programming. This pin should not be floated during normal operation.

XTAL1 — Input to the inverting amplifier that forms the oscillator, XTAL1 should be grounded when an external oscillator is used.

XTAL2 — Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator signal when an external oscillator is used.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-04-11

Approved sources of supply for SMD 84190 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8419001QA	3V146	8751H-8/BQA MC8751H-8/BQA
8419001YA	3V146	8751H-8/BYA MR8751H-8/BYA
8419002QA	3V146	8751H/BQA
8419002YA	3V146	8751H/BYA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 10 Malcolm Hoyt Drive Newburyport, MA 01950