REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert drawing to new boilerplate. Corrected vendor similar part number for vendor CAGE 34335. Editorial changes throughout.	90-02-06	W. Heckman
D	Changes in accordance with NOR 5962-R010-00.	00-07-07	Monica L. Poelking
E	Incorporated revision D and updated boilerplate and editorial changes throughout. Added vendor CAGE CODE 3V146. – LTG	00-09-27	Monica L. Poelking
F	Correct marking requirements in 3.5. Update boilerplate in accordance with MIL-PRF-38535 requirements. Editorial changes throughout. - PHN.	05-02-24	Thomas M. Hess
G	Correct case outline Z terminal count and descriptive designator in paragraph 1.2.2. Correct the figure 2 case Z terminal description for location C11 from ARDY to SRDY. - CFS.	07-08-16	Thomas M. Hess

REV																				
SHEET																				
REV	E	E	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	G	G	F	F	E	E	E	E	E	E	E	E	E	G
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Jeffery Tunstall

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
85-10-08

MICROCIRCUIT, DIGITAL, 16-BIT N-CHANNEL MICROPROCESSOR, MONOLITHIC SILICON
MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**85010**

REVISION LEVEL
G

SHEET 1 OF 34

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

85010	01	Y	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	M80186	8 MHz	16 bit N-channel microprocessor
02	M80186	6 MHz	16 bit N-channel microprocessor

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Ceramic quad flat pack
Z	CMGA3-68	68	Pin grid array package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage on any pin (referenced to GND) ---------- -1.0 V dc to +7.0 V dc
Storage temperature range ---------- -65°C to +150°C
Maximum power dissipation (P_D) ---------- 3 W
Thermal resistance, junction-to-case (θ_{JC}):
  Case Y ---------- 12°C/W
  Case Z ---------- See MIL-STD-1835
Junction temperature (T_J)---------- +150°C
Lead temperature (soldering, 5 seconds) ---------- +260°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}):
  Device type 01 ---------- 4.75 V dc to 5.25 V dc
  Device type 02 ---------- 4.75 V dc to 5.25 V dc
Frequency of operation:
  Device type 01 ---------- 8 MHz
  Device type 02 ---------- 6 MHz
Case operating temperature range (T_C)---------- -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms . The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Low-level input voltage	V_{IL}		01, 02	1,2,3	-0.5	+0.8	V
High-level input voltage (All except X1) and ($\overline{RES}$)	V_{IH1}		01, 02	1,2,3	2.0	V_{CC} +0.5	V
High-level input voltage at ($\overline{RES}$)	V_{IH2}		01, 02	1,2,3	3.0	V_{CC} +0.5	V
Low-level output voltage	V_{OL}	I_{OL} = 2.5 mA for $\overline{S0}$ - $\overline{S2}$ I_{OL} = 2.0 mA for all other outputs	01, 02	1,2,3		0.45	V
High-level output voltage	V_{OH}	I_{OH} = -400 µA	01, 02	1,2,3	2.4		V
Power supply current	I_{CC}	V_{CC} = 5.25 V	01, 02	1,2,3		600	mA
Input leakage current	I_{IL}	$0\ V < V_{IN} < V_{CC}$	01, 02	1,2,3		±10	µA
Output leakage current	I_{OL}	$0.45V < V_{OUT} < V_{CC}$	01, 02	1,2,3		±10	µA
Low-level clock output voltage	V_{CLO}	I_{OUT} = 4.0 mA	01, 02	1,2,3		0.6	V
High-level clock output voltage	V_{CHO}	I_{OUT} = -200 µA	01, 02	1,2,3	4.0		V
Low-level clock input voltage	V_{CL1}		01, 02	1,2,3	-0.5	+0.6	V
High-level clock input voltage	V_{CH1}		01, 02	1,2,3	3.9	V_{CC} +1.0	V
Functional tests		See 4.3.1d	01, 02	7,8			
Input capacitance	C_{IN}	See 4.3.1c	01, 02	4		10	pF
I/O capacitance	C_{IO}	See 4.3.1c	01, 02	4		20	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data in setup (A/D)	t_{DVCL}	C_L = 20 to 200 pF, all outputs	01,02	9,10,11	20		ns
Data in hold (A/D)	t_{CLDX}		01,02	9,10,11	10		ns
Asynchronous ready (ALREADY) active setup time	t_{ARYHCH}		01,02	9,10,11	20		ns
AREADY inactive setup time	t_{ARYLCL}		01,02	9,10,11	38		ns
AREADY hold time	t_{CHARYX}		01,02	9,10,11	15		ns
Synchronous ready (SREADY) transition setup time	t_{SRYCL}		01,02	9,10,11	35		ns
SREADY transition hold time	t_{CLSRY}		01,02	9,10,11	15		ns
Hold setup 2/	t_{HVCL}		01,02	9,10,11	25		ns
INTR, NMI, $\overline{TEST}$, TIMERIN setup 2/	t_{INVCH}		01,02	9,10,11	25		ns
DRQ0, DRQ1, setup	t_{INVCL}		01,02	9,10,11	25		ns
Address valid delay	t_{CLAV}		01	9,10,11	5	59	ns
			02	9,10,11	5	63	ns
Address hold	t_{CLAX}		01	9,10,11	5		ns
			02	9,10,11	5		ns
Address float delay	t_{CLAZ}		01	9,10,11	t_{CLAX}	35	ns
			02	9,10,11	t_{CLAX}	44	ns
Address valid to clock high	t_{AVCH}		01,02	9,10,11	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Command lines float delay	t_{CHCZ}	C_L = 20 to 200 pF, all outputs	01	9,10,11		45	ns
			02	9,10,11		56	ns
Command lines valid delay (after float)	t_{CHCV}		01	9,10,11		55	ns
			02	9,10,11		76	ns
ALE width	t_{LHLL}		01,02	9,10,11	t_{CLCL} -35		ns
ALE active delay	t_{CHLH}		01	9,10,11		35	ns
			02	9,10,11		44	ns
ALE inactive delay	t_{CHLL}		01	9,10,11		35	ns
			02	9,10,11		44	ns
Address hold to ALE inactive	t_{LLAX}		01	9,10,11	t_{CHCL} -25		ns
			02	9,10,11	t_{CHCL} -30		ns
Data valid delay	t_{CLDV}		01	9,10,11	5	44	ns
			02	9,10,11	5	55	ns
Data hold time	t_{CLDOX}		01,02	9,10,11	5		ns
Data hold after $\overline{WR}$	t_{WHDX}		01	9,10,11	t_{CLCL} -40		ns
			02	9,10,11	t_{CLCL} -50		ns
Control active delay 1	t_{CVCTV}		01	9,10,11	5	70	ns
			02	9,10,11	5	87	ns
Control active delay 2	t_{CHCTV}		01	9,10,11	5	73	ns
			02	9,10,11	5	76	ns
$\overline{DEN}$ inactive delay (non-write cycle)	t_{CVDEX}		01	9,10,11	10	70	ns
			02	9,10,11	10	87	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Address float to $\overline{RD}$ active	t_{AZRL}	C_L = 20 to 200 pF, all outputs	01,02	9,10,11	0		ns
$\overline{RD}$ active delay	t_{CLRL}		01	9,10,11	10	70	ns
			02	9,10,11	10	87	ns
$\overline{RD}$ inactive delay	t_{CLRH}		01	9,10,11	10	55	ns
			02	9,10,11	10	76	ns
$\overline{RD}$ inactive to address active	t_{RHAV}		01	9,10,11	t_{CLCL} -40		ns
			02	9,10,11	t_{CLCL} -50		ns
HLDA valid delay	t_{CLHAV}		01,02	9,10,11	5	67	ns
$\overline{RD}$ width	t_{RLRH}		01,02	9,10,11	$2t_{CLCL}$ -50		ns
$\overline{WR}$ width	t_{WLWH}		01,02	9,10,11	$2t_{CLCL}$ -40		ns
Address valid to ALE low	t_{AVAL}		01	9,10,11	t_{CLCH} -25		ns
			02	9,10,11	t_{CLCH} -45		ns
Status active delay	t_{CHSV}		01	9,10,11	10	55	ns
			02	9,10,11	10	76	ns
Status inactive delay	t_{CLSH}		01	9,10,11	10	65	ns
			02	9,10,11	10	76	ns
Timer output delay	t_{CLTMV}	C_L = 100 pF maximum	01	9,10,11		60	ns
			02	9,10,11		75	ns
Control inactive delay	t_{CVCTX}	C_L = 20 to 200 pF, all outputs	01	9,10,11		55	ns
			02	9,10,11		76	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Reset delay	t_{CLRO}	C_L = 20 to 200 pF, all outputs	01	9,10,11		60	ns
			02	9,10,11		75	ns
Queue status delay	t_{CHQSV}		01	9,10,11		35	ns
			02	9,10,11		44	ns
Chip-select active delay	t_{CLCSV}		01	9,10,11	5	66	ns
			02	9,10,11	5	80	ns
Chip-select hold from command inactive	t_{CXCSX}		01,02	9,10,11	35		ns
Chip-select inactive delay	t_{CHCSX}		01,02	9,10,11	5	47	ns
CLKIN period	t_{CKIN}		01	9,10,11	62.5	250	ns
			02	9,10,11	83	250	ns
CLKIN fall time	t_{CKHL}	3.5 V to 1.0 V 3/	01,02	9,10,11		10	ns
CLKIN rise time	t_{CKLH}	1.0 V to 3.5 V 3/	01,02	9,10,11		10	ns
CLKIN low time	t_{CLCK}	1.5 V 3/	01	9,10,11	25		ns
			02	9,10,11	33		ns
CLKIN high time	t_{CHCK}	1.5 V 3/	01	9,10,11	25		ns
			02	9,10,11	33		ns
CLKIN to CLKOUT skew	t_{CICO}	C_L = 20 to 200 pF, all outputs	01	9,10,11		50	ns
			02	9,10,11		62.5	ns
CLKOUT period	t_{CLCL}		01	9,10,11	125	500	ns
			02	9,10,11	167	500	ns
CLKOUT low time	t_{CLCH}	1.5 V 3/	01,02	9,10,11	1/2 t_{CLCL} -7.5		ns

See footnotes at end of table I.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 5\%$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
CLKOUT high time	t_{CHCL}	1.5 V 3/	01,02	9,10,11	1/2 t_{CLCL} -7.5		ns
CLKOUT rise time	t_{CH1CH2}	1.0 V to 3.5 V 3/	01,02	9,10,11		15	ns
CLKOUT fall time	t_{CL2CL1}	3.5 V to 1.0 V 3/	01,02	9,10,11		15	ns

1/ All AC parameters tested as per circuit on figure 4.
2/ Setup requirements only to guarantee recognition at next CLK.
3/ Voltage indicated refer to voltage measurements on waveforms in figure 4.

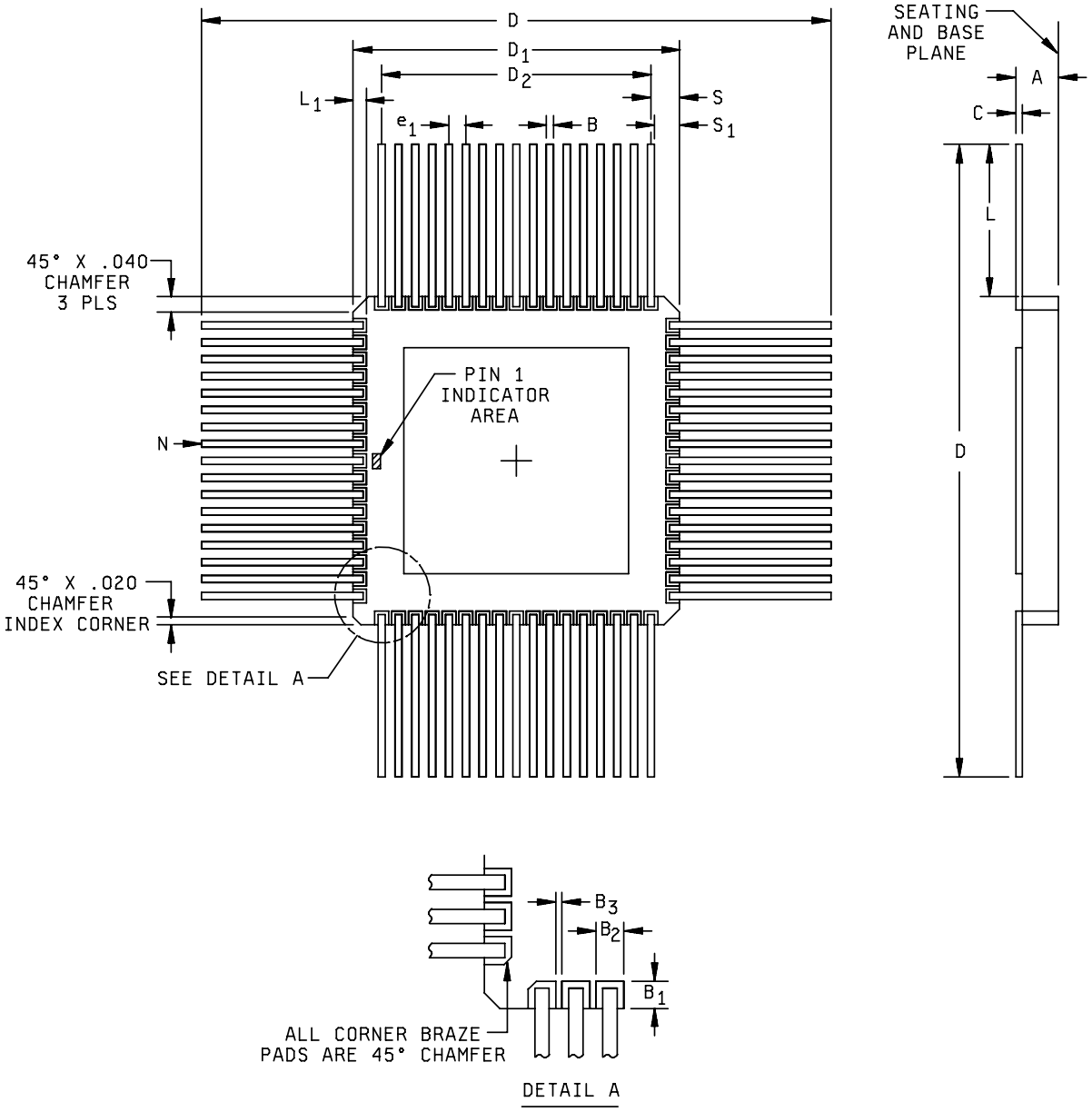


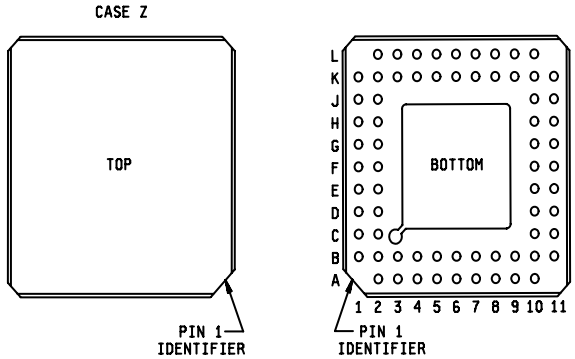
FIGURE 1. Case outline Y.

Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.080	.106	2.03	2.69
B	.016	.020	0.41	0.51
B_1	.040	.060	1.02	1.52
B_2	.030	.040	0.76	1.02
B_3	.005	.020	0.13	0.51
C	.008	.012	0.20	0.30
D	1.640	1.870	41.66	47.50
D_1	.935	.970	23.75	24.64
D_2	.800 BSC		20.32 BSC	
e_1	.050 BSC		1.27 BSC	
L	.375	.450	9.53	11.43
L_1	.040	.060	1.02	1.52
N	68 PINS		68 PINS	
S	.66	.087	1.68	2.21
S_1	.050		1.27	

FIGURE 1. Case outline Y - Continued.

Device type All			
Case outline Y			
Pin number	Pin symbol	Pin number	Pin symbol
1	V_{CC}	35	V_{CC}
2	AD4	36	INT2/ $\overline{\text{INTA0}}$
3	AD12	37	INT3/ $\overline{\text{INTA1}}$
4	AD5	38	DT/ $\overline{\text{R}}$
5	AD13	39	$\overline{\text{DEN}}$
6	AD6	40	$\overline{\text{MCS0}}$
7	AD14	41	$\overline{\text{MCS1}}$
8	AD7	42	$\overline{\text{MCS2}}$
9	AD15	43	$\overline{\text{MCS3}}$
10	A16/S3	44	$\overline{\text{UCS}}$
11	A17/S4	45	$\overline{\text{LCS}}$
12	A18/S5	46	$\overline{\text{PCS6}}$ /A2
13	A19/S6	47	$\overline{\text{PCS5}}$ /A1
14	$\overline{\text{BHE}}$ /S7	48	$\overline{\text{PCS4}}$
15	$\overline{\text{WR}}$ /QS1	49	$\overline{\text{PCS3}}$
16	$\overline{\text{RD}}$ / $\overline{\text{QSMD}}$	50	$\overline{\text{PCS2}}$
17	ALE/QS0	51	$\overline{\text{PCS1}}$
18	V_{SS}	52	V_{SS}
19	X1	53	$\overline{\text{PCS0}}$
20	X2	54	$\overline{\text{RES}}$
21	RESET	55	TMR OUT1
22	CLKOUT	56	TMR OUT0
23	ARDY	57	TMR IN1
24	$\overline{\text{S2}}$	58	TMR IN0
25	$\overline{\text{S1}}$	59	DRQ1
26	$\overline{\text{S0}}$	60	DRQ0
27	HLDA	61	AD0
28	HOLD	62	AD8
29	SRDY	63	AD1
30	$\overline{\text{LOCK}}$	64	AD9
31	$\overline{\text{TEST}}$	65	AD2
32	NMI	66	AD10
33	INT0	67	AD3
34	INT1	68	AD11

FIGURE 2. Terminal connections.



Case outline Z

Symbol	Location	Symbol	Location	Symbol	Location
V_{CC}, V_{CC}	F1, F11	A16/S3	A2	$\overline{RD}$ / $\overline{QSMD}$	A5
V_{SS}, V_{SS}	L6, A6	AD15	B1	ARDY	B9
RESET	B8	AD14	C1	SRDY	C11
X1, X2	B7, A7	AD13	D1	$\overline{LOCK}$	D10
CLKOUT	A8	AD12	E1	$\overline{S0}$	A10
$\overline{RES}$	L5	AD11	F2	$\overline{S1}$	B10
$\overline{TEST}$	D11	AD10	G2	$\overline{S2}$	A9
TMR IN0	L3	AD9	H2	HOLD	C10
TM,R IN1	K3	AD8	J2	(Input)	
TMR OUT0	L4	AD7	B2	HLDA	B11
TMR OYT1	K4	AD6	C2	(output)	
DRQ0	L2	AD5	D2	$\overline{UCS}$	L10
DRQ1	K2	AD4	E2	$\overline{LCS}$	K9
NM1	E10	AD3	G1	$\overline{MCS0}$ - 3	J10, J11, K10, K11
INT0, INT1	E11, F10	AD2	H1	$\overline{PCS0}$	K5
INT2/ $\overline{INTA0}$	G10	AD1	J1	$\overline{PCS1}$ - 4	K6, L7, K7, L8
INT3/ $\overline{INTA1}$	G11	AD0	K1	$\overline{PCS5}$ /A1	K8
A19/S6	B4	$\overline{BHE}$ /S7	A4	$\overline{PCS6}$ /A2	L9
A18/S5	A3	ALE/QS0	B6	DT/ $\overline{R}$	H10
A17/S4	B3	$\overline{WR}$ /QS1	B5	$\overline{DEN}$	H11

FIGURE 2. Terminal connections - Continued.

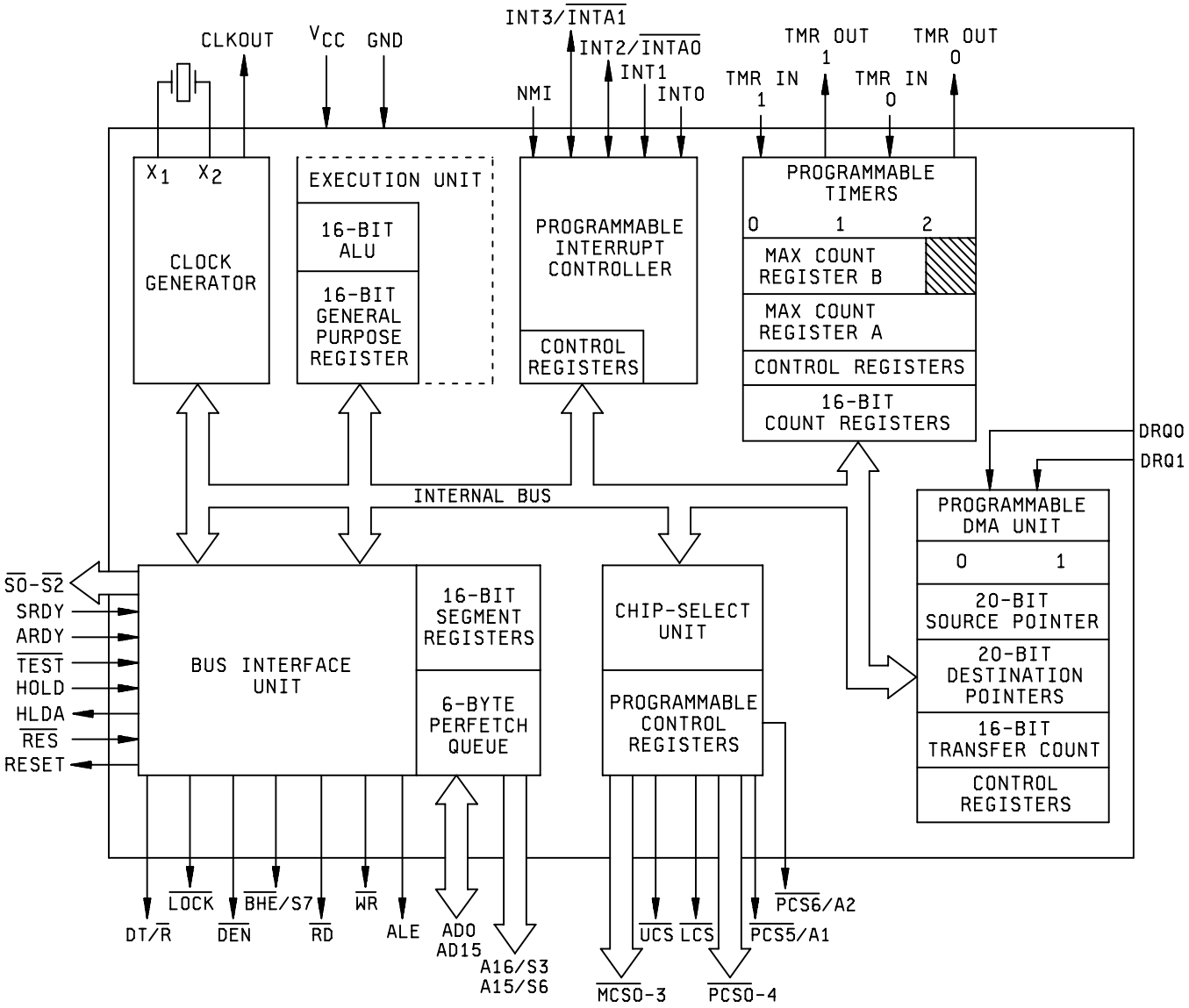


FIGURE 3. Functional block diagram.

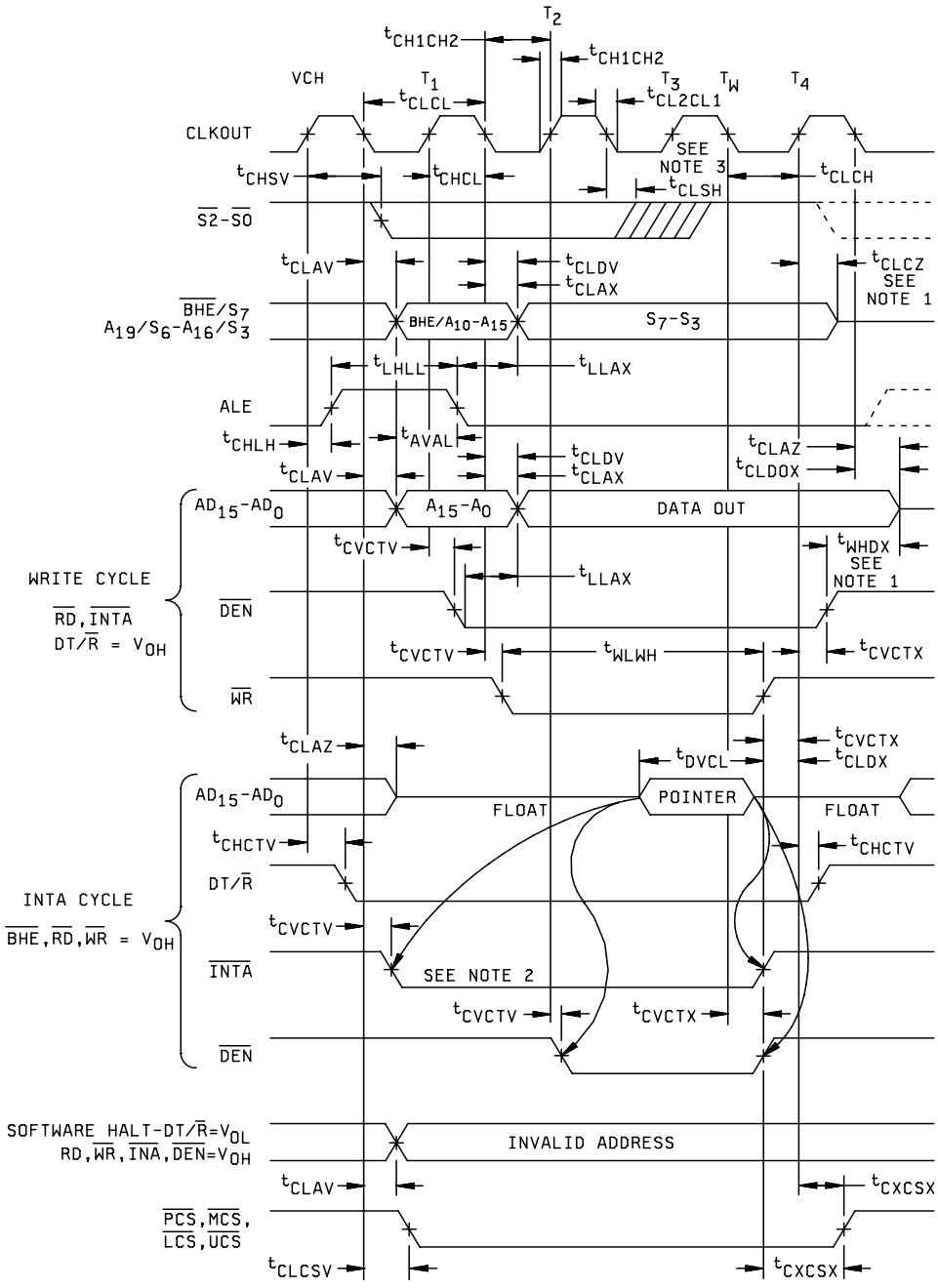
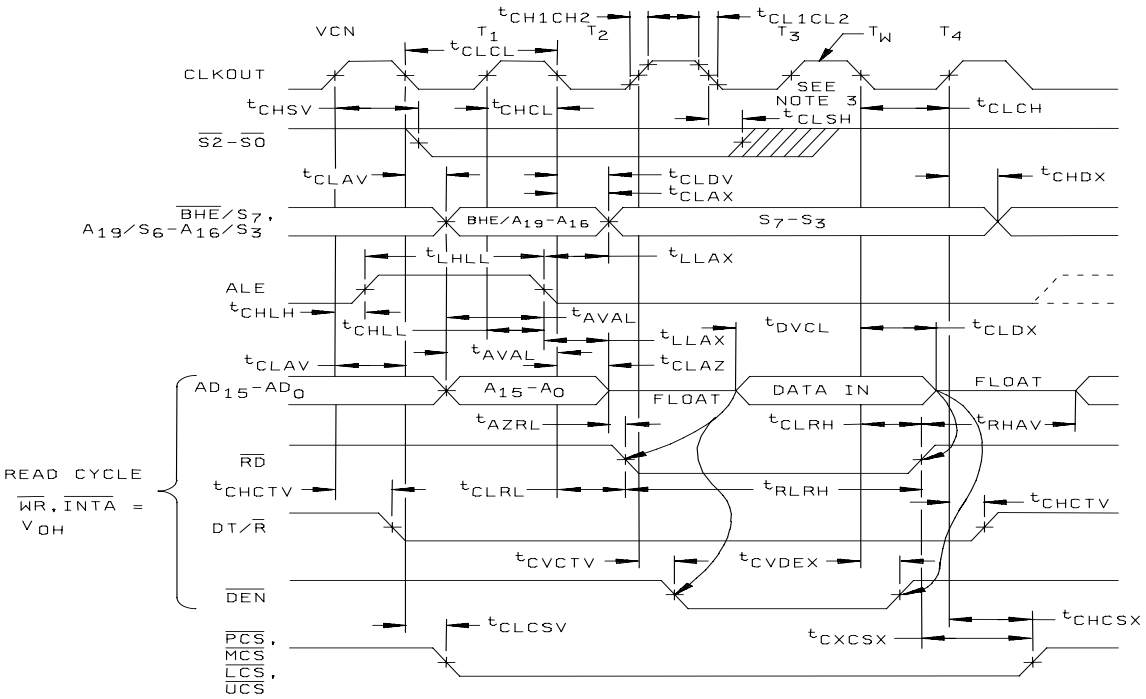


FIGURE 4. Timing waveforms.



NOTES:

1. Following a write cycle, the local bus is floated by the 80186 only when the 80186 enters a "hold acknowledge" state.
2. $\overline{\text{INTA}}$ occurs one clock later in RMX-mode.
3. Status inactive just prior to T4.

FIGURE 4. Timing waveforms - Continued.

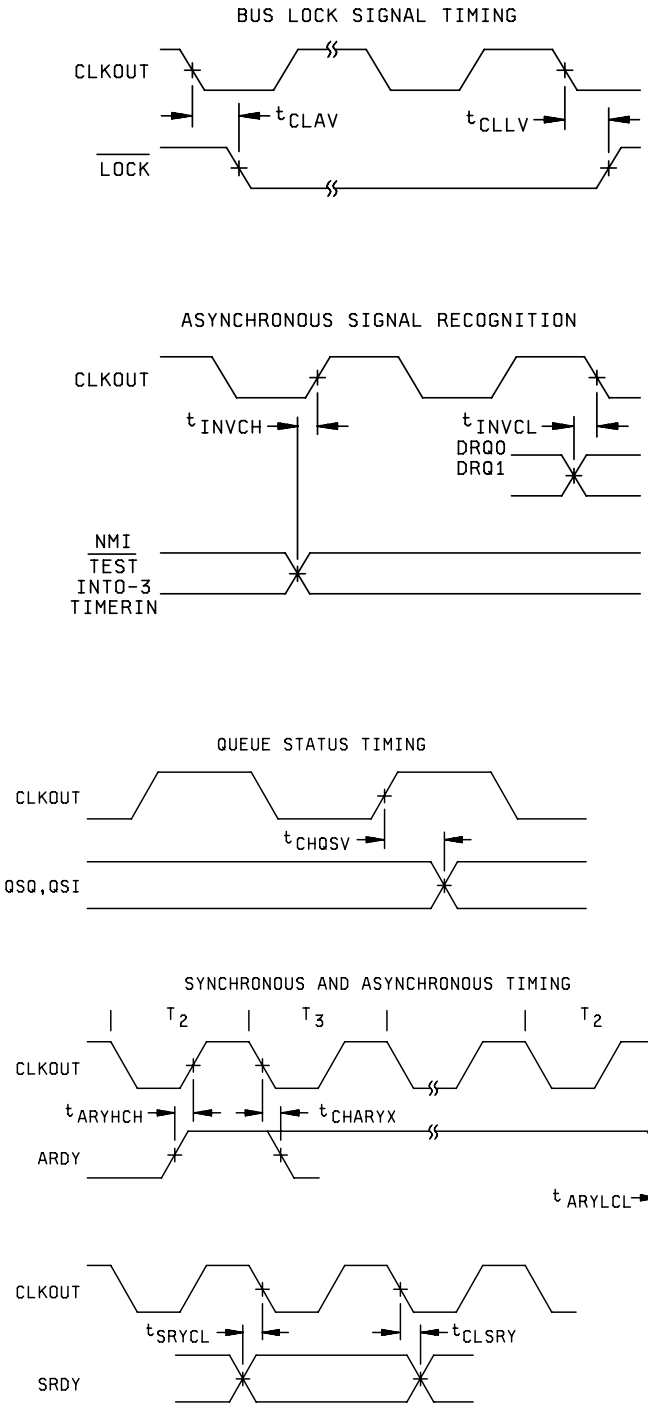
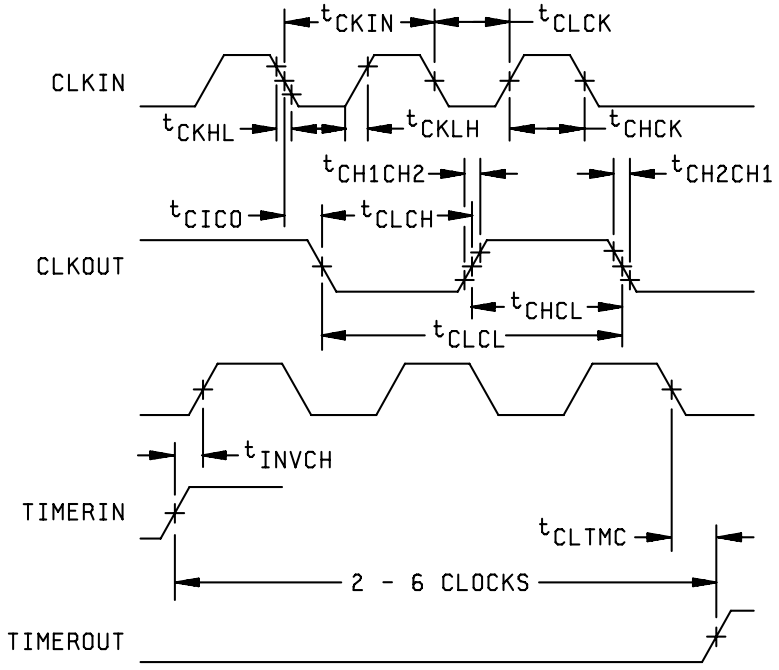


FIGURE 4. Timing waveforms - Continued.

TIMER TIMING



HOLD-HLDA TIMING

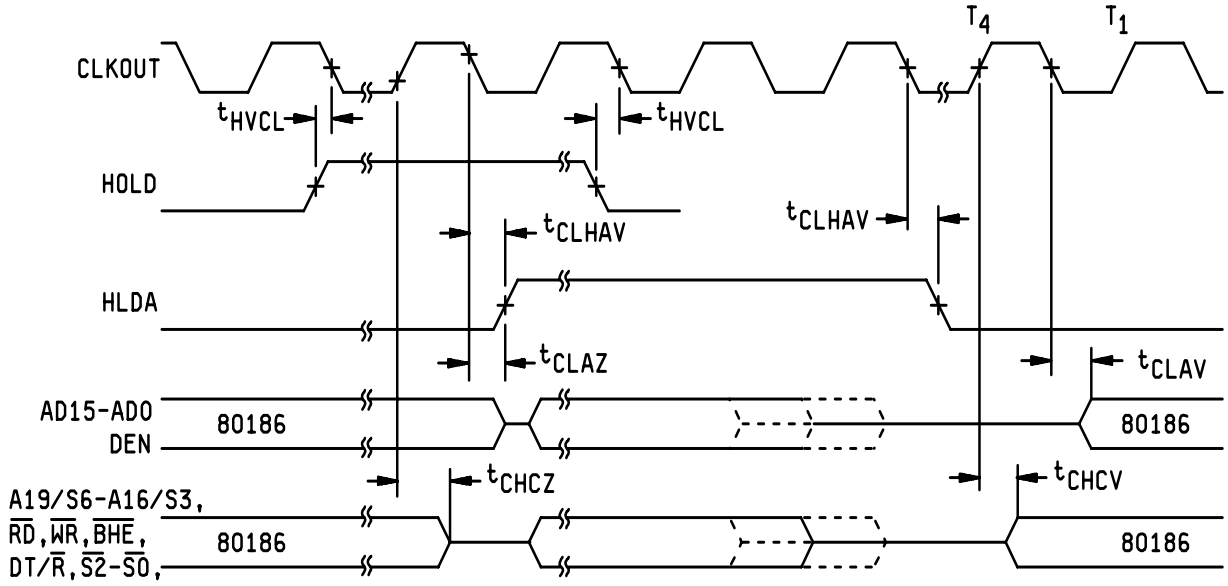


FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	------
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	2/ 1, 2, 3, 4, 7, 8 ,9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(+125°C only), 10 or 1,2,3,7,8

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN,}$ and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero failures shall be required.

d. Subgroups 7 and 8 shall include verification of the programming set. See table III.

TABLE III. Instruction set summary.

Function	Format			Clock cycles	Comments
DATA TRANSFER MOV = Move:					
Register to register/memory	1 0 0 0 1 0 0 w	mod reg r/m		1/12	
Register/memory to register	1 0 0 0 1 0 1 w	mod reg r/m		2/9	
Immediate to register/memory	1 1 0 0 0 1 1 w	mod reg r/m	data data if W = 1	12-13	8/16-bit
Immediate to register	1 0 1 1 w reg	data	data if W = 1	3-4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	9	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	8	
Register/memory to segmet register	1 0 0 0 1 1 1 0	mod 0 reg r/m		2/9	
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		2/11	
PUSH = Push:					
Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		16	
Register	0 1 0 1 0 reg			10	
Segment register	0 0 0 reg 1 1 0			9	
Immediate	0 1 1 0 1 0 s 0	data	data if s = 0	10	
PUSHA = Push All	0 1 1 0 0 0 0 0				
POP = Pop:					
Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		20	
Register	0 1 0 1 1 reg			10	
Segment register	0 0 0 reg 1 1 1	(reg 01)		8	
POPA = Pop All	0 1 1 0 0 0 0 1			51	
XCHG = Exchange:					
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		4/17	
Register with accumulator	1 0 0 1 0 reg			3	
IN = Input from:					
Fixed port	1 1 1 0 0 1 0 w	port		10	
Variable port	1 1 1 0 1 1 0 w			8	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
OUT = Output to:			
Fixed port	1 1 1 0 0 1 1w | port	9	
Variable port	1 1 1 0 1 1 1 wW	7	
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1	11	
LEA = Load EA to register	1 0 0 0 1 1 0 1 | mod reg r/m	6	
LDS = Load pointer to DS	1 1 0 0 0 1 0 1 | mod reg r/m | (mod ≠ 11)	18	
LES = Load pointer to ES	1 1 0 0 0 1 0 0 | mod reg r/m | (mod ≠ 11)	18	
LAHF = Load AH with flags	1 0 0 1 1 1 1 1	2	
SAHF = Store AH into flags	1 0 0 1 1 1 1 0	3	
PUSHF = Push flags	1 0 0 1 1 1 0 0	9	
POPF = Pop flags	1 0 0 1 1 1 0 1	8	
SEGMENT = Segment Override:			
CS	0 0 1 0 1 1 1 0	2	
DS	0 0 1 1 0 1 1 0	2	
ES	0 0 1 0 0 1 1 0	2	
ARITHMETIC			
ADD = Add:			
Reg/memory with register to either	0 0 0 0 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 s w | mod 0 0 0 r/m | data | data if s w =	4/16	
Immediate to accumulator	0 0 0 0 0 1 0 w | data | data if w = 1	3/4	8/16-bit
ADC = Add with carry:			
Reg/memory with register to either	0 0 0 1 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 s w | mod 0 1 0 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0 0 0 1 0 1 0 w | data | data if w = 1	3/4	8/16-bit
INC = Increment:			
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 0 r/m	3/15	
Register	0 1 0 0 0 reg	3	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
Sub = Subtract:			
Reg/memory and register to either	0 0 1 0 1 0 d w | mod reg r/m	3/10	
Immediate from register/memory	1 0 0 0 0 0 w | mod 1 0 1 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0 0 1 0 1 1 0 w | data | data if w = 1	3/4	8/16-bit
SSB = Subtract with borrow:			
Reg/memory and register to either	0 0 0 1 1 0 d w | mod req r/m	3/10	
Immediate from register/memory	1 0 0 0 0 0 s w | mod 0 1 1 r/m | data | data if s w =	4/16	
Immediate from accumulator	0 0 0 1 1 1 0 w | data | data if w = 1	3/4	8/16-bit
DEC = Decrement:			
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	3/15	
Register	0 1 0 0 1 reg	3	
CMP = Compare:			
Register/memory with register	0 0 1 1 1 0 1 w | mod reg r/m	3/10	
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	3/10	
Immediate with register/memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w = 01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w | data | data if w = 1	3/4	8/16-bit
NEG = Change sign	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	3	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	
DAS = Decimal adjust for substract	0 0 1 0 1 1 1 1	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | moc 1 0 0 r/m		
Register-Byte		26-28	
Register-Word		35-37	
Memory-Byte		32-34	
Memory-Word		41-43	
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m		
Register-Byte		25-28	
Register-Word		34-37	
Memory-Byte		31-34	
Memory-Word		40-43	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
ARITHMETIC (Continued):			
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1 | mod reg r/m | data | data if s = 0	22-25/ 29-32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w | mod 1 1 0 r/m		
Register-Byte		29	
register-Word		38	
Memory-Byte		35	
Memory-Word		44	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w | mod 1 1 1 r/m		
Register-Byte		44-52	
Register-Word		53-61	
Memory-Byte		50-58	
Memory-Word		59-67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1	4	
LOGIC			
Shift/rotate instructions:			
Register/memory by 1	1 1 0 1 0 0 0 w | mod TTT r/m	2/15	
Register/memory by CL	1 1 0 1 0 0 1 w | mod TTT r/m	5+n/ 17+n	
Register/memory by count	1 1 0 0 0 0 0 w | mod TTT r/m | count	5+n/ 17+n	

TTT	Instruction
0 0 0	ROL
0 0 1	ROR
0 1 0	RCL
0 1 1	RCR
1 0 0	SHL/SAL
1 0 1	SHR
1 1 1	SAR

TABLE III. Instruction set summary - Continued.

Function	Format				Clock cycles	Comments
AND = And:						
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1		3/4	8/16-bit
TEST = And function to flags, no result:						
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1		3/4	8/16-bit
OR = Or:						
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1		3/4	8/16-bit
XOR = Exclusive or:						
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1		3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w	moc 0 1 0 r/m			3	
STRING MANIPULATION:						
MOVS = Move byte/word	1 0 1 0 0 1 0 w				14	
CMPS = Compart byte/word	1 0 1 0 0 1 1 w				22	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w				15	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w				12	
STOS = Store byte/wd from AL/A	1 0 1 0 1 0 1 w				10	
INS = input byte/wd from DX port	0 1 1 0 1 1 0 w				14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w				14	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
STRING MANIPULATION (Continued): Repeated by count in CX			
MOVS = Move string	1 1 1 1 0 0 1 0 | 1 0 1 0 0 1 0 w	8+8n	
CMPS = Compare string	1 1 1 1 0 0 1 z | 1 0 1 0 0 1 1 w	5+22n	
SCAS = Scan string	1 1 1 1 0 0 1 z | 1 0 1 0 1 1 1 w	5+15n	
LODS = Load string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 1 0 w	6+11n	
STOS = Store string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 0 1 w	6+9n	
INS = Input string	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 0 w	8+8n	
OUTS = Output str9ng	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 1 w	8+8n	
CONTROL TRANSFER			
CALL = Call:			
Direct within segment	1 1 1 0 1 0 0 0 | disp-low | disp-high	14	
Register/memory indirect within segment	1 1 1 1 1 1 1 1 | mod 0 1 0 r/m	13/19	
Direct intersegment	1 0 0 1 1 0 1 0 | segment offset segment selector	23	
Indirect intersegment	1 1 1 1 1 1 1 1 | mod 0 1 1 r/m	38	
JMP = Unconditional jump:			
Short/long	1 1 1 0 1 0 1 1 | disp-low	13	
Direct within segment	1 1 1 0 1 0 0 1 | disp-low | disp-high	13	
Register/memory indirect within segment	1 1 1 1 1 1 1 1 | mod 1 0 0 r/m	11/17	
Direct intersegment	1 1 1 0 1 0 1 0 | segment offset segment selector	13	
Indirect intersegment	1 1 1 1 1 1 1 1 | mod 1 0 1 r/m	26	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1	16	
Within seg adding immed to SP	1 1 0 0 0 1 0 | data-low | data-high	18	
Intersegment	1 1 0 0 1 0 1 1	22	
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0 | data-low | data-high	25	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
CONTROL TRANSFER (Continued):			
JE/JZ = Jump on equal zero	0 1 1 1 0 1 0 0 disp	4/13	JMP not taken/JMP
JL/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0 disp	4/13	taken
JLE/JNG = Jump on less or equal/ not greater	0 1 1 1 1 1 1 0 disp	4/13	
JB/JNAE = Junp on below/not above or equal	0 1 1 1 0 0 1 0 disp	4/13	
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0 disp	4/13	
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0 disp	4/13	
JO = Jump on overflow	0 1 1 1 0 0 0 0 disp	4/13	
JS = Jump on sign	0 1 1 1 1 0 0 0 disp	4/13	
JNE/JNZ = Jump on not equal/ not zero	0 1 1 1 0 1 0 1 disp	4/13	
JNL/JGE = Jump on not less/ greater or equal	0 1 1 1 1 1 0 1 disp	4/13	
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1 disp	4/13	
JNB/JAE = Jump on not below/ above or equal	0 1 1 1 0 0 1 1 disp	4/13	
JNBE/JA = Jump on not below/ or equal/above	0 1 1 1 0 1 1 1 disp	4/13	
JNP/JPO = Jump on not par/par odd	0 1 1 1 1 0 1 1 disp	4/13	
JNO = Jump on not overflow	0 1 1 1 0 0 0 1 disp	4/13	
JNS = Jump on not sign	0 1 1 1 1 0 0 1 disp	4/13	
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1 disp	5/15	
LOOP = Loop CX times	1 1 1 0 0 0 1 0 disp	6/16	
LOOPZ/LOOPE = Loop while zero/ equal	1 1 1 0 0 0 0 1 disp	6/16	LOOP not Taken/LOOP taken
LOOPNZ/LOOPNE = Loop while not Zero/equal	1 1 1 0 0 0 0 0 disp	6/16	

TABLE III. Instruction set summary - Continued.

Function	Format	Clock cycles	Comments
ENTER = Enter procedure	1 1 0 0 1 0 0 0 data-low data-high L		
L = 0		15	
L = 1		25	
L > 1		22+16 (n-1)	
LEAVE = Leave procedure	1 1 0 0 1 0 0 1	8	
INT = Interrupt:			
Type specified	1 1 0 0 1 1 0 1 type	47	
Type 3	1 1 0 0 1 1 0 0	45	if INT. taken/
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	48/4	if INT. not taken
IRET = Interrupt return	1 1 0 0 1 1 1 1	28	
BOUND = Detect value out of range	0 1 1 0 0 0 1 0 mod reg r/m	33-35	
PROCESSOR CONTROL			
CLC = Clear carry	1 1 1 1 1 0 0 0	2	
CMC = Complement carry	1 1 1 1 0 1 0 1	2	
STC = Set carry	1 1 1 1 1 0 0 1	2	
CLD = Clear direction	1 1 1 1 1 1 0 0	2	
STD = Set direction	1 1 1 1 1 1 0 1	2	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	2	
STI = Set interrupt	1 1 1 1 1 0 1 1	2	
HLT = Halt	1 1 1 1 0 1 0 0	2	
WAIT = Wait	1 0 0 1 1 0 1 1	6	if test = 0
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	2	
ESC = Processor extension escape	1 0 0 1 1 T T T mod LLL r/m (TTT LLL are opcode to processor extension)	6	

NOTES:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field

if mod = 00 then DISP = 0*, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent

if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 010 then EA = (BP) + (SI) + DISP

if r/m = 011 then EA = (BP) + (DI) + DISP

if r/m = 100 then EA = (SI) + DISP

if r/m = 101 then EA = (DI) + DISP

if r/m = 110 then EA = (BP) + DISP*

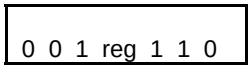
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*Except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

SEGMENT OVERRIDE PREFIX



reg is assigned according to the following:

reg	Register Segment
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit(w = 1)	8-Bit(w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Symbols, definitions and functional descriptions. The symbols, definitions, and functional descriptions for this device shall be as follows:

Symbol	Name and function
V_{CC}	System power: +5 volt power supply.
V_{SS}	System ground.
RESET	Reset output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the RES signal.
X1, X2	Crystal inputs, X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	Clock output provides the system with a 50 percent duty cycle waveform. All device pin timings are specified relative to CLKOUT.
$\overline{\text{RES}}$	System reset causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately 7 clock cycles after $\overline{\text{RES}}$ is returned HIGH. $\overline{\text{RES}}$ is required to be LOW for greater than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to-HIGH transition of $\overline{\text{RES}}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{\text{RES}}$ generation via an RC network. When $\overline{\text{RES}}$ occurs, the 80186 will drive the status lines to an inactive level for one clock, and then three-state them.
$\overline{\text{TEST}}$	$\overline{\text{TEST}}$ is examined by the WAIT instruction. If the $\overline{\text{TEST}}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{\text{TEST}}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for $\overline{\text{TEST}}$, interrupts will be serviced. The input is synchronized internally.
TMR IN 0, TMR IN 1	Timer inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	Timer outputs are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ0 DRQ1	DMA request is driven HIGH by an external device when it desires that a DMA channel (channel 0 or 1) perform a transfer. These signals are active HIGH, level-triggered, and internally synchronized.
NMI	Non-maskable interrupt is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a LOW to HIGH initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
INT0, INT1, INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$	Maskable interrupt requests can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge-or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowleged. When iRMX mode is selected, the function of these pins changes.

A19/S6, A18/S5, A17/S4, A16/S3

Address bus outputs (16-19) and bus cycle status (3-6) reflect the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, status information is available on these lines as encoded below:

	Low	High
S6	Processor cycle	DMA cycle

S3, S4, and S5 are defined as LOW during T_2-T_4.

AD_{15}-AD_0

Address/data bus (0-15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH A_0 is analogous to BHE for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory of I/O operations.

$\overline{BHE}$ /S7

During T_1 the bus high enable signal should be used to determine if data is to be enabled onto the most significant half of the data bus, pins D_{15}-D_8.

$\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S7 status information is available during T_2, T_3, and T_4. S7 is logically equivalent to $\overline{BHE}$. The signal is active LOW, and is three-stated OFF during bus HOLD.

$\overline{BHE}$ and A0 encodings		
$\overline{BHE}$ value	A0 value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D15-D8)
1	0	Byte transfer on lower half of data bus (D7-D0)
1	1	Reserved

ALE/QS0

Address latch enable/queue status 0 is provided by the 80186 to latch the address into the address latches. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle. The trailing edge is generated off the CLKOUT rising edge in T_1. Note that ALE is never floated.

$\overline{WR}$ /QS1

Write strobe/queue status 1 indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats during "HOLD." It is driven HIGH for one clock during reset and then floated. When the 80186 is in queue status mode, the ALE/QS0 and $\overline{WR}$ /QS1 pins provide information about processor instruction queue interaction.

QS1	QS0	Queue operation
0	0	No queue operation
0	1	First opcode byte fetched from the queue
1	1	Subsequent byte fetched from the queue
1	0	Empty the queue

$\overline{RD}$ / $\overline{QSMD}$ — Read strobe indicates that the 80186 is performing a memory or I/O read cycle. $\overline{RD}$ is active LOW for T_2, T_3, and T_W of any read cycle. It is guaranteed not to go LOW in T_2 until after the address bus is floated. $\overline{RD}$ is active LOW, and floats during "HOLD." $\overline{RD}$ is driven HIGH for one clock during reset, and then the output driver is floated. A weak internal pull-up mechanism on the $\overline{RD}$ line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the 80186 should provide ALE, $\overline{WR}$, and $\overline{RD}$, or if the queue-status should be provided. $\overline{RD}$ should be connected to GND to provide queue-status data.

ARDY — Asynchronous ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the 80186. This means that the falling edge of ARDY must be synchronized to the 80186 clock. If connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle.

SRDY — Synchronous ready must be synchronized externally to the 80186. The use of SRDY provides a relaxed system-timing specification on the ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW.

$\overline{LOCK}$ — $\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the $\overline{LOCK}$ prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the $\overline{LOCK}$ prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ is active LOW, is driven HIGH for one clock during RESET, and then floated. If unused, this line should be tied LOW.

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$ — Bus cycle status $\overline{S0}$ - $\overline{S2}$ are encoded to provide bus-transaction information.

80186 bus cycle status information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus cycle initiated
0	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	Passive (no bus cycle)

The status pins float during "HOLD.
$\overline{S2}$ may be used as a logical M/IO indicator, and $\overline{S1}$ as a DT/$\overline{S1}$ indicator.
The status lines are driven HIGH for one clock during reset, and then floated until a bus cycle begins.

HOLD (input) HLDA (output)	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80186 clock. The 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of T_4 or T_1. Simultaneous with the issuance of HLDA the 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{\text{UCS}}$	Upper memory chip select is an active LOW output whenever a memory reference is made to the defined upper portion (1K-256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{\text{UCS}}$ is software programmable.
$\overline{\text{LCS}}$	Lower memory chip select is active LOW whenever a memory reference is made to the defined lower portion (1K-256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{\text{LCS}}$ is software programmable.
$\overline{\text{MCS0}}$ -3	Mid-range memory chip select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K-512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{\text{MCS0}}$ -3 are software programmable.
$\overline{\text{PCS0}}$ $\overline{\text{PCS1}}$-4	Peripheral chip select signals 0-4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{\text{PCS0}}$ -4 are software programmable.
$\overline{\text{PCS5}}$ /A1	Peripheral chip select 5 or latched A_1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A_1 signal. The address range activating $\overline{\text{PCS5}}$ is software programmable. When programmed to provide latched A_1, rather than $\overline{\text{PCS5}}$, this pin will retain the previously latched value of A_1 during a bus HOLD. A_1 is active HIGH.
$\overline{\text{PCS6}}$ /A2	Peripheral chip select 6 or latched A_2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A_2 signal. The address range activating $\overline{\text{PCS6}}$ is software programmable. When programmed to provide latched A_2, rather than $\overline{\text{PCS6}}$, this pin will retain the previously latched value of A_2 during a bus HOLD. A_2 is active HIGH.
DT/$\overline{\text{R}}$	Data transmit/receive controls the direction of data flow through the external data bus transceiver. When LOW, data is transferred to the 80186. When HIGH the 80186 places write data on the data bus.
$\overline{\text{DEN}}$	Data enable is provided as a data bus transceiver output enable. $\overline{\text{DEN}}$ is active LOW during each memory and I/O access. $\overline{\text{DEN}}$ is HIGH whenever DT/$\overline{\text{R}}$ changes state.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-08-16

Approved sources of supply for SMD 85010 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8501001ZA	3V146	MG80186-8/BZA
8501001ZC	3V146	MG80186-8/BZC
8501001YA	3V146	MQ80186-8/BYA
8501001YC	3V146	MQ80186-8/BYC
8501002ZA	3V146	MG80186-6/BZA
8501002ZC	3V146	MG80186-6/BZC
8501002YA	3V146	MQ80186-6/BYA
8501002YC	3V146	MQ80186-6/BYC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics, Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950