REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to military drawing. Changes to table I. Changes to figures 2 and 4. Editorial changes throughout.	87-04-14	N. A. Hauck
B	Changes to table I and figure 1 dimensions.	88-01-22	M. A. Frye
C	Update boilerplate to MIL-PRF-38535 requirements. Add “QD” device criteria. Add vendor CAGE 3V146. Correct drawing title. - CFS	03-02-13	Thomas M. Hess
D	Correct marking requirements in 3.5. Update boilerplate in accordance with MIL-PRF-38535 requirements. Editorial changes throughout. - PHN.	05-04-11	Thomas M. Hess

REV																				
SHEET																				
REV	C																			
SHEET	15																			

REV STATUS	REV	D	C	D	D	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

D. A. Di Cenzo

APPROVED BY

N. A. Hauck

DRAWING APPROVAL DATE

86-04-04

REVISION LEVEL

D

MICROCIRCUIT, DIGITAL, 4-BIT BIPOLAR STATUS AND SHIFT CONTROL UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**86017**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

86017	01	Q	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2904	4-bit bipolar status and shift control unit

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
Y	See figure 1	42	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.914 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-STD-1835
Case Y	9°C/W
DC output current into inputs	30 mA
DC input current	-30 mA to +5.0 mA
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH})	+2.0 V dc
Maximum low-level input voltage (V_{IL})	+0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Load circuits. The load circuits shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified			Group A subgroups	Device type	Limits		Unit
							Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -1.6 mA Y_Z, Y_C, Y_N, Y_{OVR}		1, 2, 3	01	2.4		V
			I_{OH} = -0.8 mA SIO_o, SIO_n, QIO_o, QIO_n, CT, C_O				2.4		
Output low voltage	V_{OL}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 16 mA Y_Z, Y_C, Y_N, Y_{OVR}					0.5	V
			I_{OL} = 8 mA SIO_o, SIO_n, QIO_o, QIO_n, CT, C_O					0.5	
Input high voltage	V_{IH}	1/					2.0		V
Input low voltage	V_{IL}	1/						0.8	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA						-1.5	V
Input low current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.5 V	CP					-0.7	mA
			$\overline{CE}_m$, $\overline{CE}_\mu$					-1.8	
			I_Z, I_C, I_N, I_{OVR}					-1.2	
			I_0-I_{12}, $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, E_{OVR}, OE_Y, OE_{CT}, C_X, Y_Z, Y_C, Y_N, Y_{OVR}					-0.45	
			$\overline{SE}$, SIO_o, SIO_n, QIO_o, QIO_n					-1.35	
Input high current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V	CP, I_0-I_{12}, $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, E_{OVR}, OE_Y, OE_{CT}, C_X					20	µA
			$\overline{CE}_m$, $\overline{CE}_\mu$					80	
			I_Z, I_C, I_N, I_{OVR}, $\overline{SE}$					60	
			SIO_o, SIO_n, QIO_o, QIO_n					110	
			Y_Z, Y_C, Y_N, Y_{OVR}					70	
Input high current	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V						1.0	mA
Off-state (high impedance) output current	I_{OZH}, I_{OZL}	V_{CC} = 5.5 V	CT	V_O = 2.4 V				50	µA
				V_O = 0.5 V				-50	
			SIO_o, SIO_n, QIO_o, QIO_n 2/	V_O = 2.4 V				110	
				V_O = 0.5 V				-1350	
			Y_Z, Y_C, Y_N, Y_{OVR} 2/	V_O = 2.4 V				70	
				V_O = 0.5 V				-450	
Output short circuit current 3/	I_{OS}	V_{CC} = 5.75 V, V_O = 0.5 V					-30	-85	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power supply current 4/	I_{CC}	V_{CC} = 5.5 V	T_C = -55°C to +125°C	1, 2, 3	01		348	mA
			T_C = +125°C	2			222	
Setup time 1	t_{s1}	C_L = 50 pF, see figure 4		9, 10, 11		15		ns
Hold time 1	t_{h1}	Inputs: I_Z, I_{IN}, I_{OVR}					5	ns
Setup time 2	t_{s2}	C_L = 50 pF, see figure 4				28		ns
Hold time 2	t_{h2}	Inputs: I_C (I_1, I_2, I_3 = 001)					5	ns
Setup time 3	t_{s3}	C_L = 50 pF, see figure 4				15		ns
Hold time 3	t_{h3}	Inputs: I_C (I_1, I_2, $I_3 \ne 001$)					5	ns
Setup time 4	t_{s4}	C_L = 50 pF, see figure 4				20		ns
Hold time 4	t_{h4}	Inputs: $\overline{CE}_\mu$					3	ns
Setup time 5	t_{s5}	C_L = 50 pF, see figure 4				23		ns
Hold time 5	t_{h5}	Inputs: $\overline{CE}_m$					4	ns
Setup time 6	t_{s6}	C_L = 50 pF, see figure 4				23		ns
Hold time 6	t_{h6}	Inputs: $\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$					4	ns
Setup time 7	t_{s7}	C_L = 50 pF, see figure 4				48		ns
Hold time 7	t_{h7}	Inputs: $I_0 - I_5$					2	ns
Setup time 8	t_{s8}	C_L = 50 pF, see figure 4				44		ns
Hold time 8	t_{h8}	Inputs: $I_6 - I_{10}$					2	ns
Setup time 9	t_{s9}	C_L = 50 pF, see figure 4				40		ns
Hold time 9	t_{h9}	Inputs: $\overline{SE}$					0	ns
Setup time 10	t_{s10}	C_L = 50 pF, see figure 4				16		ns
Hold time 10	t_{h10}	Inputs: Y_Z, Y_C, Y_N, Y_{OVR}, I_{0-5} = LOW					6	ns
Setup time 11	t_{s11}	C_L = 50 pF, see figure 4				20		ns
Hold time 11	t_{h11}	Inputs: SIO_o, SIO_n, QIO_o, QIO_n					5	ns
Propagation delay 1: From (input): I_Z, I_C, I_N, I_{OVR} To (output): Y_Z, Y_C, Y_N, Y_{OVR}	t_{pd1}	C_L = 50 pF, see figure 4					40	ns
Propagation delay 2: From (input): CP To (output): Y_Z, Y_C, Y_N, Y_{OVR}	t_{pd2}						45	ns
Propagation delay 3: From (input): I_4, I_5 To (output): Y_Z, Y_C, Y_N, Y_{OVR}	t_{pd3}						38	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay 4: From (input): I_Z, I_C, I_N, I_{OVR} To (output): CT	t_{pd4}	C_L = 50 pF, see figure 4	9, 10, 11	01		44	ns
Propagation delay 5: From (input): CP To (output): CT	t_{pd5}					40	ns
Propagation delay 6: From (input): I_0 - I_5 To (output): CT	t_{pd6}					41	ns
Propagation delay 7: From (input): C_X To (output): C_O	t_{pd7}					22	ns
Propagation delay 8: From (input): CP To (output): C_O	t_{pd8}					28	ns
Propagation delay 9: From (input): I_1, I_2, I_3, I_5, I_{11}, I_{12} To (output): C_O	t_{pd9}					42	ns
Propagation delay 10: From (input): SIO_n, QIO_n To (output): SIO_o	t_{pd10}					20	ns
Propagation delay 11: From (input): SIO_o, QIO_o To (output): SIO_n	t_{pd11}					20	ns
Propagation delay 12: From (input): I_C, I_N, I_{OVR} To (output): SIO_o	t_{pd12}					29	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay 13: From (input): SIO_n, QIO_n To (output): QIO_o	t_{pd13}	C_L = 50 pF, see figure 4	9, 10, 11	01		20	ns
Propagation delay 14: From (input): SIO_o, QIO_o To (output): QIO_n	t_{pd14}					20	ns
Propagation delay 15: From (input): CP To (output): SIO_o, SIO_n, QIO_o, QIO_n	t_{pd15}					32	ns
Propagation delay 16: From (input): $I_6 - I_{10}$ To (output): SIO_o, SIO_n, QIO_o, QIO_n	t_{pd16}					31	ns
Enable time 1: From (input): $\overline{OE}_{CT}$ To (output): CT	t_{EN1}					25	ns
Disable time 1: From (input): $\overline{OE}_{CT}$ To (output): CT	t_{DIS1}	C_L = 5 pF, see figure 4				18	ns
Enable time 2: From (input): $\overline{SE}$ To (output): SIO_o, SIO_n, QIO_o, QIO_n	t_{EN2}	C_L = 50 pF, see figure 4				35	ns
Disable time 2: From (input): $\overline{SE}$ To (output): SIO_o, SIO_n, QIO_o, QIO_n	t_{DIS2}	C_L = 5 pF, see figure 4				20	ns

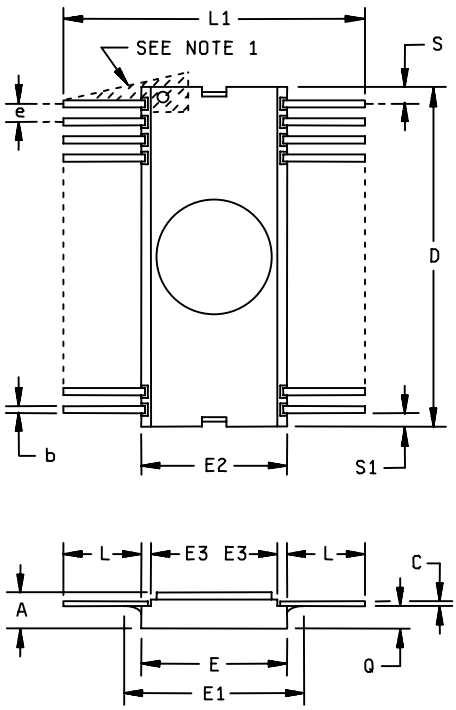
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable time 3: From (input): I_{10} To (output): SIO_o, SIO_n, QIO_o, QIO_n	t_{EN3}	C_L = 50 pF, see figure 4	9, 10, 11	01		43	ns
Disable time 3: From (input): I_{10} To (output): SIO_o, SIO_n, QIO_o, QIO_n	t_{DIS3}	C_L = 5 pF, see figure 4				32	ns
Enable time 4: From (input): $\overline{OEY}$ To (output): Y_Z, Y_C, Y_N, Y_{OVR}	t_{EN4}	C_L = 50 pF, see figure 4				28	ns
Disable time 4: From (input): $\overline{OEY}$ To (output): Y_Z, Y_C, Y_N, Y_{OVR}	t_{DIS4}	C_L = 5 pF, see figure 4				23	ns
Enable time 5: From (input): $I_0 - I_5$ To (output): Y_Z, Y_C, Y_N, Y_{OVR}	t_{EN5}	C_L = 50 pF, see figure 4				30	ns
Disable time 5: From (input): $I_0 - I_5$ To (output): Y_Z, Y_C, Y_N, Y_{OVR}	t_{DIS5}	C_L = 5 pF, see figure 4				41	ns
Minimum clock low time	t_{CL}				25		ns
Minimum clock high time	t_{CH}				25		ns

1/ These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).
2/ These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with output enables high.
3/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4/ Worst case I_{CC} is at minimum temperature.

Case outline Y



Case outline	Y	
Symbol	Inches	
	Minimum	Maximum
A	.070	.098
b	.017	.023
c	.006	.010
D	1.050	1.090
E	.620	.660
E1	---	.720
E2	.520	---
E3	.030	---
e	.045	.055
L	.310	.370
L1	1.280	1.360
Q	.030	.060
S	---	.045
S1	.005	---

NOTES:
1. Index area: A notch, tab, or pin one identification mark shall be located within the shaded area shown.
2. E1 allows for Ag-Cu alloy brazed overrun.
3. Dim. b and c increase by 3 mils max. limit if tinplate/solder dip lead finish is applied.
4. All dimensions are given in inches.

FIGURE 1. Case outlines.

Device type	01		
Case outline Q		Case outline Y	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I_7	1	I_3
2	$\overline{CE}_\mu$	2	$\overline{CE}_m$
3	I_6	3	$\overline{E}_Z$
4	I_5	4	NC
5	I_4	5	I_Z
6	I_3	6	V_{CC}
7	$\overline{CE}_m$	7	$\overline{E}_C$
8	$\overline{E}_Z$	8	I_C
9	I_Z	9	$\overline{E}_N$
10	V_{CC}	10	I_N
11	$\overline{E}_C$	11	$\overline{E}_{OVR}$
12	I_C	12	NC
13	$\overline{E}_N$	13	I_{OVR}
14	I_N	14	CP
15	$\overline{E}_{OVR}$	15	I_0
16	I_{OVR}	16	I_1
17	CP	17	$\overline{OEY}$
18	I_0	18	I_2
19	I_1	19	I_{11}
20	$\overline{OEY}$	20	I_{12}
21	I_2	21	C_X
22	I_{11}	22	C_O
23	I_{12}	23	$\overline{OE}_{CT}$
24	C_X	24	CT
25	C_O	25	Y_{OVR}
26	$\overline{OE}_{CT}$	26	Y_N
27	CT	27	GND
28	Y_{OVR}	28	Y_C
29	Y_N	29	Y_Z
30	GND	30	QIO_n
31	Y_C	31	QIO_o
32	Y_Z	32	SIO_n
33	QIO_n	33	SIO_o
34	QIO_o	34	$\overline{SE}$
35	SIO_n	35	I_{10}
36	SIO_o	36	I_9
37	$\overline{SE}$	37	I_8
38	I_{10}	38	I_7
39	I_9	39	$\overline{CE}_\mu$
40	I_8	40	I_6
		41	I_5
		42	I_4

FIGURE 2. Terminal connections.

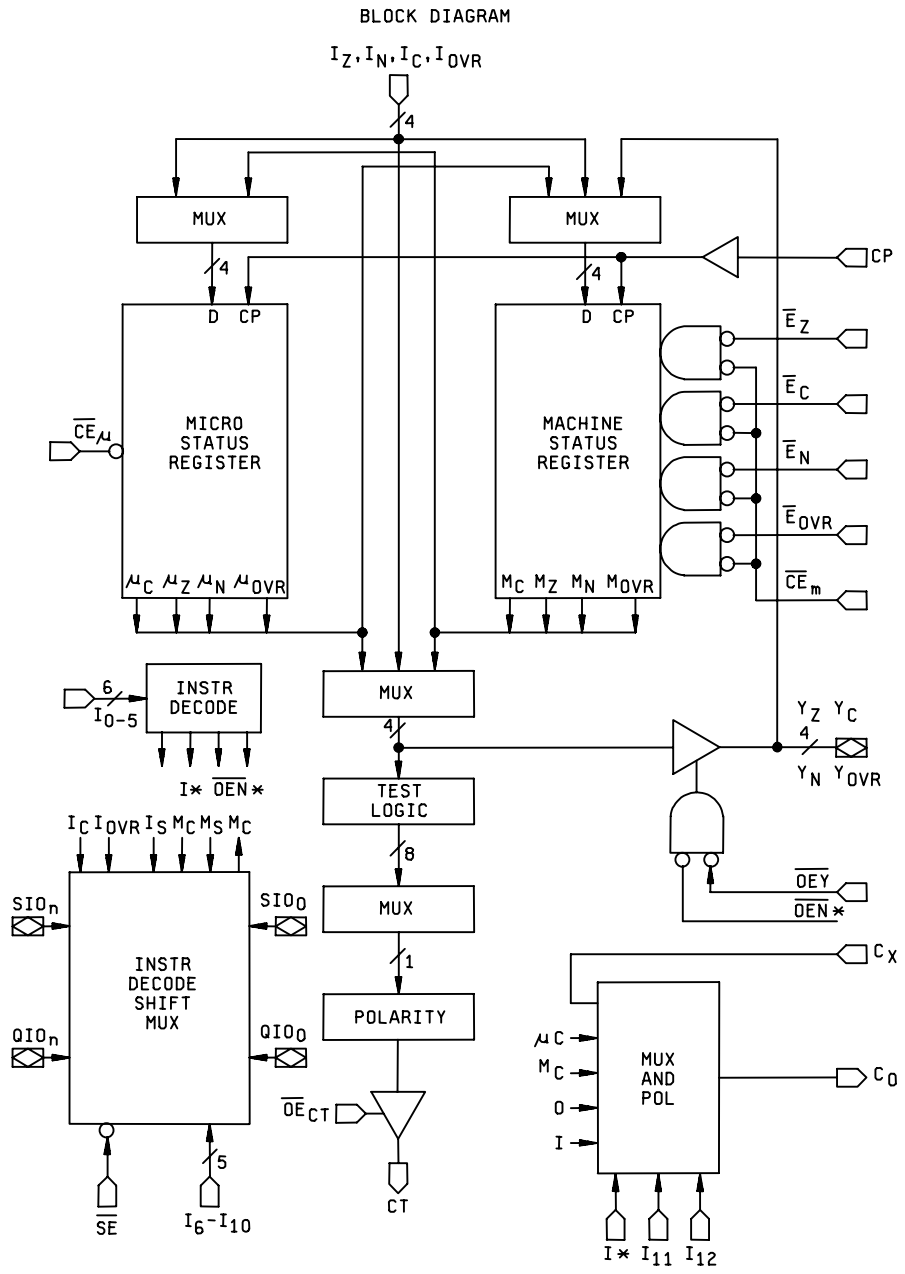
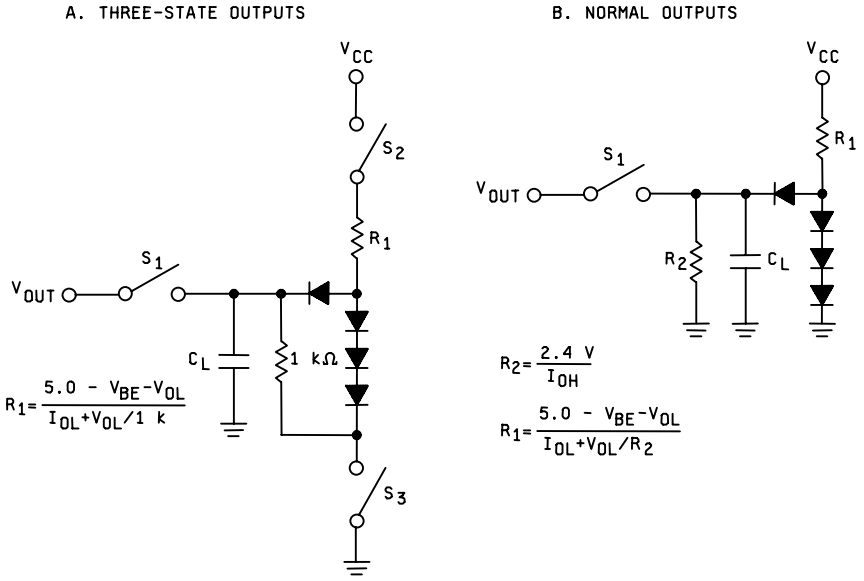


FIGURE 3. Functional block diagram.

SWITCHING TEST CIRCUIT



Pin (DIP)	Pin (FP)	Pin label	Test circuit	R_1	R_2
25	22	C_O	B	470	3k
27	24	CT	A	430	1k
28	25	Y_{OVR}	A	220	1k
29	26	Y_N	A	220	1k
31	28	Y_C	A	220	1k
32	29	Y_Z	A	220	1k
33	30	QIO_n	A	430	1k
34	31	QIO_o	A	430	1k
35	32	SIO_n	A	430	1k
36	33	SIO_o	A	430	1k

NOTES:
1. C_L = 50 pF includes scope probe, wiring, and stray capacitances without device in test fixture.
2. S_1, S_2, and S_3 are closed during function tests and all ac tests except output enable test.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test. S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5 pF for output disable tests.

FIGURE 4. Load circuits.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the input to output logic combinations.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-04-11

Approved sources of supply for SMD 86017 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8601701QA	3V146	2904/BQA
8601701YA	3V146	2904/BYA
8601701YC	3V146	2904/BYC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 10 Malcolm Hoyt Drive Newburyport, MA 01950