

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to military drawing format, page 2, case Z change from 2150 mW to 1825 mW. Page 5, table I, change V <sub>OL</sub> test condition I <sub>OL</sub> from -1 mA to 1 mA. Change code identification number to 67268.	87-11-25	M. A. FRYE
B	Add a C-J4 package and change the vendor's part number. Editorial changes throughout.	90-10-15	M. A. FRYE
C	Make correction to marking paragraph 3.5. Drawing updated to reflect current requirements. -rrp	05-04-04	R. MONNIN
D	Change to setup time, t <sub>SU</sub> , condition from 20 ns to 28 ns for device type 01 in 1.4. -rrp	06-07-07	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

**CURRENT CAGE CODE 67268**

REV																				
SHEET																				
REV	D	D	D																	
SHEET	15	16	17																	

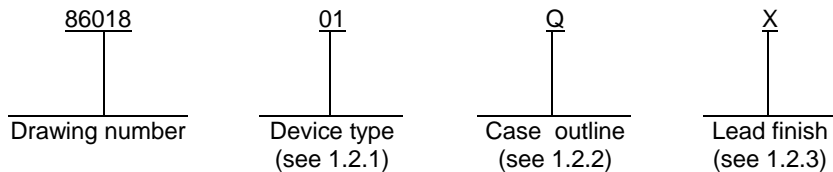
REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A	PREPARED BY RICK C. OFFICER	<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dsccl.dla.mil">http://www.dsccl.dla.mil</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY CHARLES E. BESORE																		
	APPROVED BY MICHAEL A. FRYE	<p align="center">MICROCIRCUIT, LINEAR, AC PLASMA DISPLAY DRIVERS, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 86-04-15																		
	REVISION LEVEL D		SIZE A	CAGE CODE <b>14933</b>	<b>86018</b>														
		SHEET	1 OF 17																

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	55500	AC plasma display driver (line select)
02	55501	AC plasma display driver (matrix - addressable)

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC2-J44	44	J-lead chip carrier
Z	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Input voltage .....	$V_{CC1} + 0.3 \text{ V}$
Supply voltage ( $V_{CC1}$ ) .....	13.8 V <u>1/</u>
Supply voltage ( $V_{CC2}$ ) .....	100 V
Storage temperature range .....	-65°C to +150°C
Continuous total dissipation at (or below) $T_A = +25^\circ\text{C}$ :	
Case Q .....	1650 mW
Cases X and Z .....	1825 mW
Lead temperature soldering (0.0625 inch from case for 60 seconds):	
Case Q .....	+300°C
Cases X and Z .....	+260°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835

1/ Voltage values are with respect to network ground terminal.

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1.4 Recommended operating conditions.

Supply voltage ( $V_{CC1}$ ) .....	10.8 V to 13.2 V
Supply voltage ( $V_{CC2}$ ) .....	0 V to 100 V
High level input voltage ( $V_{IH}$ ) as a percentage of $V_{CC1}$ .....	75% minimum
Low level input voltage ( $V_{IL}$ ) as a percentage of $V_{CC1}$ .....	25% maximum
Peak high level output current .....	-20 mA maximum
Peak low level output current .....	20 mA maximum
High level output clamp current .....	20 mA maximum
Low level output clamp current .....	-20 mA maximum
Clock frequency ( $f_{clock}$ ) .....	0 MHz to 8 MHz <u>2/</u>
Duration of high or low clock pulse ( $t_W$ ) .....	62 ns minimum
Setup time ( $t_{SU}$ ) data inputs before clock low to high, device type 01 .....	28 ns minimum
Setup time ( $t_{SU}$ ) data inputs before clock low to high, device type 02.....	20 ns minimum
Setup time ( $t_{SU}$ ) select inputs before strobe high to low, device type 01 .....	50 ns minimum
Hold time ( $t_H$ ), data inputs after clock low to high .....	50 ns minimum
Hold time ( $t_H$ ), strobe input after clock low to high, device type 01 .....	50 ns minimum
Hold time ( $t_H$ ), strobe high hold time after clock high, device type 02 .....	150 ns minimum
Hold time ( $t_H$ ), select inputs after strobe low to high, device type 01 .....	50 ns minimum
Hold time ( $t_H$ ), strobe high hold time after sustain high, device type 02 .....	250 ns minimum
Ambient operating temperature range ( $T_A$ ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2/ For operation above  $T_A = +25^\circ\text{C}$  junction temperature (see figure 1).

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### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic symbols and functional block diagrams. The logic symbols and functional block diagrams shall be as specified on figure 3.

3.2.4 Switching waveforms. The switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V <sub>IK</sub>	V <sub>CC1</sub> = 12 V, I <sub>I</sub> = -12 mA	1, 2, 3	01		-1.5	V
High level output voltage	V <sub>OH</sub>	V <sub>CC1</sub> = 13.2 V, I <sub>OH</sub> = -1 mA, V <sub>CC2</sub> = 100 V	1, 2, 3	01	94		V
		V <sub>CC1</sub> = 13.2 V, I <sub>OH</sub> = -10 mA, V <sub>CC2</sub> = 100 V			92		
		V <sub>CC1</sub> = 13.2 V, I <sub>OH</sub> = -15 mA, V <sub>CC2</sub> = 100 V			90		
Low level output voltage	V <sub>OL</sub>	V <sub>CC1</sub> = 13.2 V, I <sub>OL</sub> = 1 mA, V <sub>CC2</sub> = 100 V	1, 2, 3	01		2.0	V
		V <sub>CC1</sub> = 13.2 V, I <sub>OL</sub> = 10 mA, V <sub>CC2</sub> = 100 V				4.0	
		V <sub>CC1</sub> = 13.2 V, I <sub>OL</sub> = 15 mA, V <sub>CC2</sub> = 100 V				5.0	
Output clamp voltage	V <sub>OK</sub>	V <sub>CC2</sub> = 0 V, I <sub>O</sub> = 20 mA	1, 2, 3	01		2.5	V
		V <sub>CC2</sub> = 0 V, I <sub>O</sub> = -20 mA				-2.5	
High level input current	I <sub>IH</sub>	V <sub>CC1</sub> = 13.2 V, V <sub>I</sub> = V <sub>IH</sub> minimum	1, 2, 3	01		1.0	μA
Low level input current	I <sub>IL</sub>	V <sub>CC1</sub> = 13.2 V, V <sub>I</sub> = V <sub>IL</sub> maximum	1, 2, 3	01		-1.0	μA
Supply current	I <sub>CC1</sub>	V <sub>CC1</sub> = 13.2 V, V <sub>I</sub> = V <sub>CC1</sub> max	1, 2, 3	01		1.0	mA
		V <sub>CC1</sub> = 13.2 V, V <sub>I</sub> = 0				1.0	
Supply current	I <sub>CC2</sub>	V <sub>CC2</sub> = 100 V, 8 outputs high	1, 2, 3	01		5.0	mA
		V <sub>CC2</sub> = 100 V, all output low				3.0	
Delay time, high to low level output from strobe input	t <sub>DHL</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V	9	01		250	ns
			10, 11			350	
Delay time, low to high level output from strobe input	t <sub>DLH</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V	9	01		450	ns
			10, 11			550	
Transition time, high to low level output	t <sub>THL</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V	9, 10, 11	01		200	ns
Transition time, low to high level output	t <sub>TLH</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V	9, 10, 11	01		250	ns

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V <sub>IK</sub>	V <sub>CC1</sub> = 12 V, I <sub>I</sub> = -12 mA	1, 2, 3	02		-1.5	V
High level output voltage	V <sub>OH</sub>	V <sub>CC1</sub> = 13.2 V, I <sub>OH</sub> = -1 mA, V <sub>CC2</sub> = 100 V, Q outputs	1, 2, 3	02	94		V
		V <sub>CC1</sub> = 13.2 V, I <sub>OH</sub> = -10 mA, V <sub>CC2</sub> = 100 V, Q outputs			92		
		V <sub>CC1</sub> = 13.2 V, I <sub>OH</sub> = -15 mA, V <sub>CC2</sub> = 100 V, Q outputs			90		
		V <sub>CC1</sub> = 10.8 V, I <sub>OH</sub> = -100 μA, V <sub>CC2</sub> = 100 V, serial data			9		
Low level output voltage	V <sub>OL</sub>	V <sub>CC1</sub> = 13.2 V, I <sub>OL</sub> = 1 mA, V <sub>CC2</sub> = 100 V, Q outputs	1, 2, 3	02		2.0	V
		V <sub>CC1</sub> = 13.2 V, I <sub>OL</sub> = 10 mA, V <sub>CC2</sub> = 100 V, Q outputs				4.0	
		V <sub>CC1</sub> = 13.2 V, I <sub>OL</sub> = 15 mA, V <sub>CC2</sub> = 100 V, Q outputs				5.0	
		V <sub>CC1</sub> = 10.8 V, I <sub>OL</sub> = 100 μA, V <sub>CC2</sub> = 100 V, serial data				1.0	
Q output clamp voltage	V <sub>OK</sub>	V <sub>CC2</sub> = 0 V, I <sub>O</sub> = 20 mA	1, 2, 3	02		2.5	V
		V <sub>CC2</sub> = 0 V, I <sub>O</sub> = -20 mA				-2.5	
High level input current	I <sub>IH</sub>	V <sub>CC1</sub> = 13.2 V, V <sub>CC2</sub> = 100 V V <sub>IH</sub> = V <sub>IH</sub> minimum	1, 2, 3	02		1.0	μA
Low level input current	I <sub>IL</sub>	V <sub>CC1</sub> = 13.2 V, V <sub>CC2</sub> = 100 V V <sub>IL</sub> = V <sub>IL</sub> maximum	1, 2, 3	02		-1.0	μA
Low voltage supply current	I <sub>CC1</sub>	V <sub>CC1</sub> = 13.2 V, V <sub>I</sub> = V <sub>CC1</sub> , V <sub>CC2</sub> = 100 V	1, 2, 3	02		1.0	mA
		V <sub>CC1</sub> = 13.2 V, V <sub>I</sub> = GND, V <sub>CC2</sub> = 100 V				1.0	
High voltage supply current	I <sub>CC2</sub>	V <sub>CC2</sub> = 100 V, outputs low	1, 2, 3	02		1.0	mA
		V <sub>CC2</sub> = 100 V, outputs high				5.0	
Transition time high to low level Q output	t <sub>THL</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V	9, 10, 11	02		200	ns
Transition time low to high level Q output	t <sub>TLH</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V	9, 10, 11	02		250	ns
Delay time to high to low transition	t <sub>DHL</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V, from strobe to Q outputs	9	02		250	ns
			10, 11			300	
		C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V, from sustain to Q outputs	9			250	
			10, 11			300	

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time to low to high transition	t <sub>DLH</sub>	C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V, from strobe to Q outputs	9	02		450	ns
			10, 11			650	
		C <sub>L</sub> = 30 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V, from sustain to Q outputs	9			450	
			10, 11			650	
Delay time to high to low from clock to serial data output	t <sub>DHL</sub>	C <sub>L</sub> = 20 pF, V <sub>CC1</sub> = 12 V, V <sub>CC2</sub> = 100 V	9	02		147	ns
			10, 11			300	
	t <sub>DLH</sub>		9			147	
			10, 11			300	

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

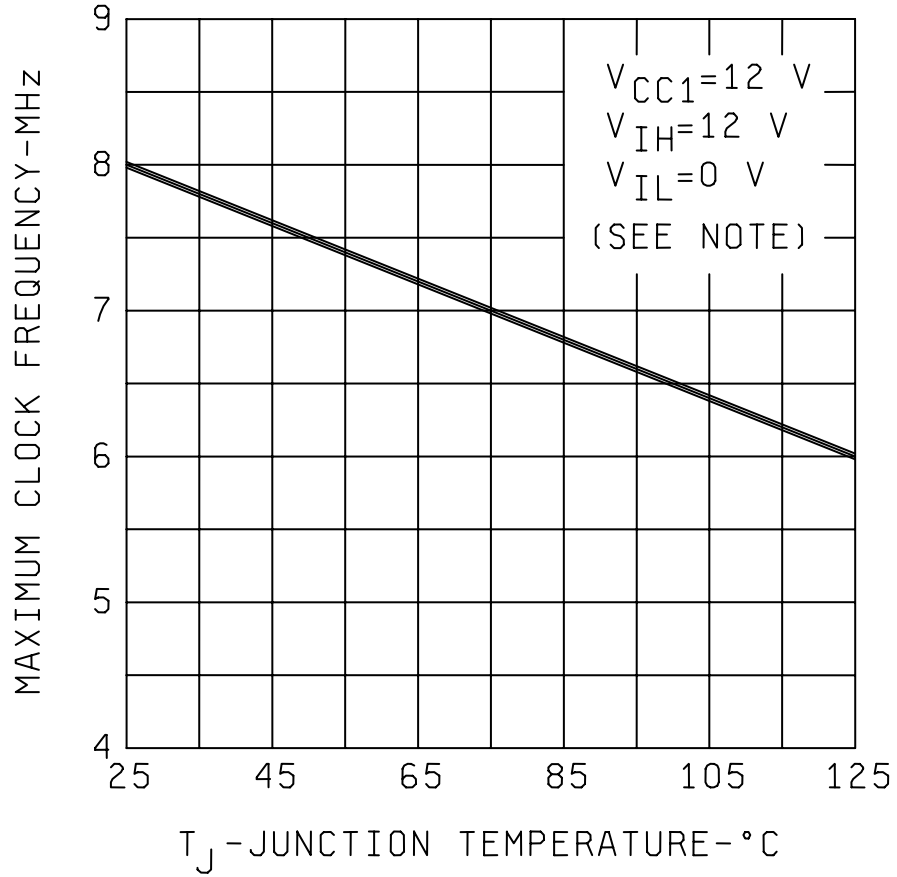
(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T<sub>A</sub> = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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MAXIMUM CLOCK FREQUENCY  
 VS  
 VIRTUAL JUNCTION TEMPERATURE



NOTE: This curve assumes a symmetrical clock pulse.

FIGURE 1. Clock-frequency to temperature curve.

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Device types	01		02	
Case outlines	Q	X and Z	Q	X and Z
Terminal number	Terminal symbol			
1	SO	NC	CLOCK	NC
2	DATA	S0	SUSTAIN	CLOCK
3	CLOCK	DATA	STROBE	SUSTAIN
4	1Q1	CLOCK	Q1	STROBE
5	1Q2	NC	Q2	NC
6	1Q3	1Q1	Q3	Q1
7	1Q4	1Q2	Q4	Q2
8	1Q5	1Q3	Q5	Q3
9	1Q6	1Q4	Q6	Q4
10	1Q7	1Q5	Q7	Q5
11	1Q8	1Q6	Q8	Q6
12	2Q1	1Q7	Q9	Q7
13	2Q2	1Q8	Q10	Q8
14	2Q3	2Q1	Q11	Q9
15	2Q4	2Q2	Q12	Q10
16	2Q5	2Q3	Q13	Q11
17	2Q6	2Q4	Q14	Q12
18	2Q7	2Q5	Q15	Q13
19	2Q8	2Q6	Q16	Q14
20	GND	2Q7	GND	Q15
21	V <sub>CC2</sub>	2Q8	V <sub>CC2</sub>	Q16
22	3Q8	GND	Q17	GND
23	3Q7	NC	Q18	NC
24	3Q6	V <sub>CC2</sub>	Q19	V <sub>CC2</sub>
25	3Q5	3Q8	Q20	Q17
26	3Q4	3Q7	Q21	Q18
27	3Q3	3Q6	Q22	Q19
28	3Q2	3Q5	Q23	Q20
29	3Q1	3Q4	Q24	Q21
30	4Q8	3Q3	Q25	Q22
31	4Q7	3Q2	Q26	Q23
32	4Q6	3Q1	Q27	Q24
33	4Q5	4Q8	Q28	Q25
34	4Q4	4Q7	Q29	Q26
35	4Q3	4Q6	Q30	Q27
36	4Q2	4Q5	Q31	Q28
37	4Q1	4Q4	Q32	Q29
38	STROBE	4Q3	SERIAL OUT	Q30
39	S1	4Q2	DATA IN	Q31
40	V <sub>CC1</sub>	4Q1	V <sub>CC1</sub>	Q32
41	----	NC	----	NC
42	----	STROBE	----	SERIAL OUT
43	----	S1	----	DATA IN
44	----	V <sub>CC1</sub>	----	V <sub>CC1</sub>

NC = No connection

FIGURE 2. Terminal connections.

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Device type 01

LOGIC SYMBOLS

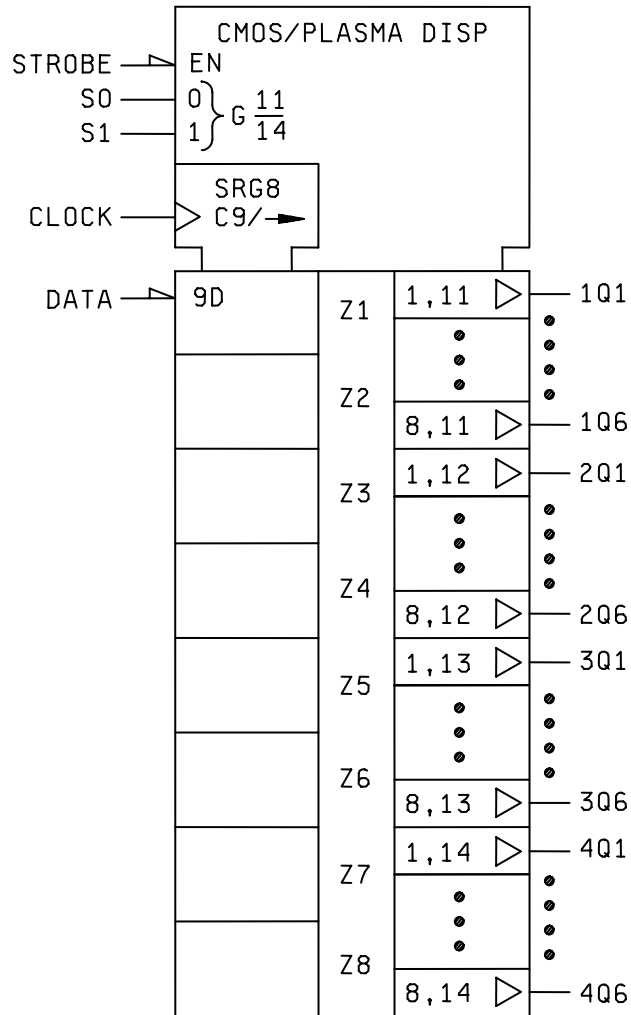


FIGURE 3. Logic symbols and functional block diagrams.

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FUNCTIONAL BLOCK DIAGRAM (POSITIVE LOGIC)

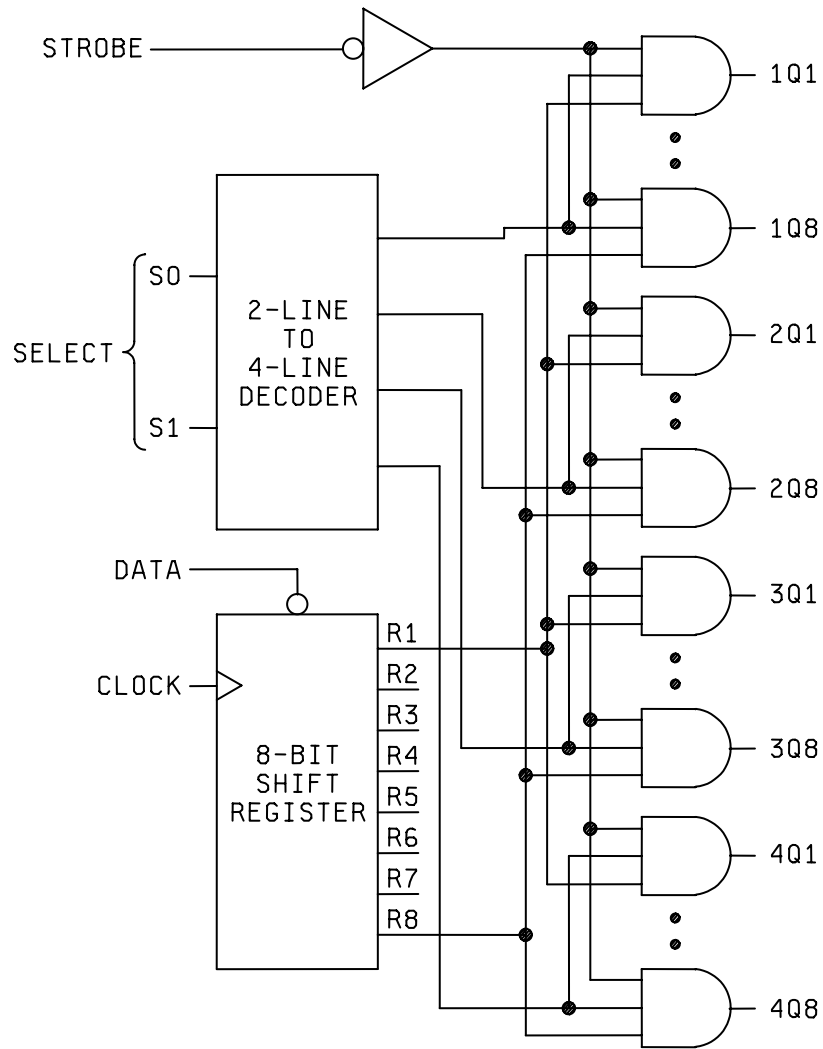


FIGURE 3. Logic symbols and functional block diagrams – Continued.

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LOGIC SYMBOLS

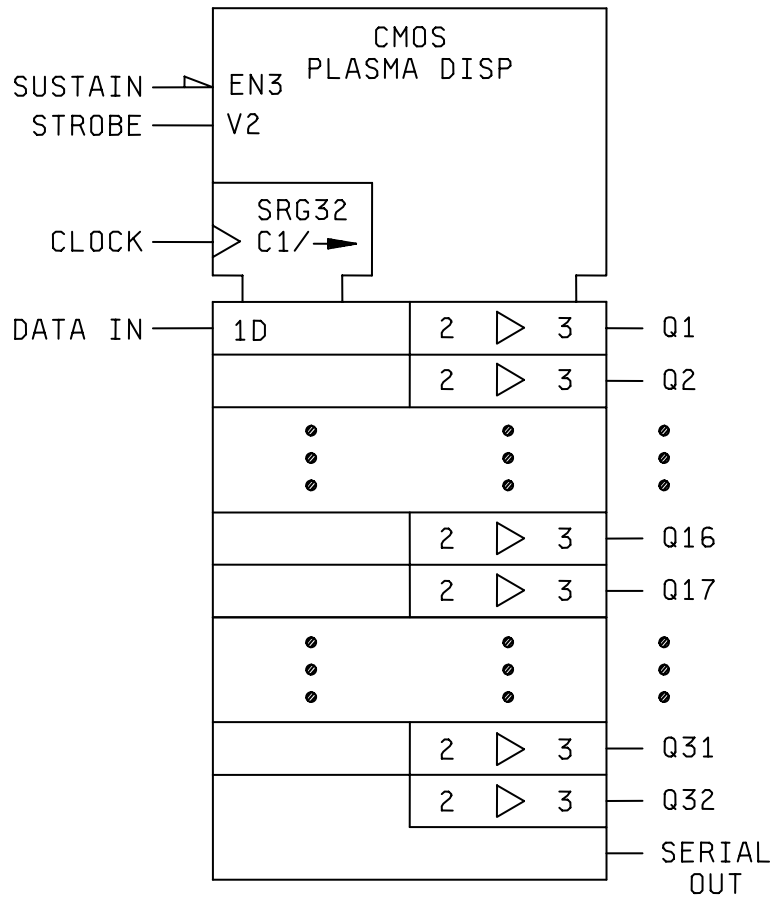


FIGURE 3. Logic symbols and functional block diagrams – Continued.

<p><b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</p>	<p>SIZE <b>A</b></p>		<p><b>86018</b></p>
		<p>REVISION LEVEL <b>D</b></p>	<p>SHEET <b>12</b></p>

FUNCTIONAL BLOCK DIAGRAM (POSITIVE LOGIC)

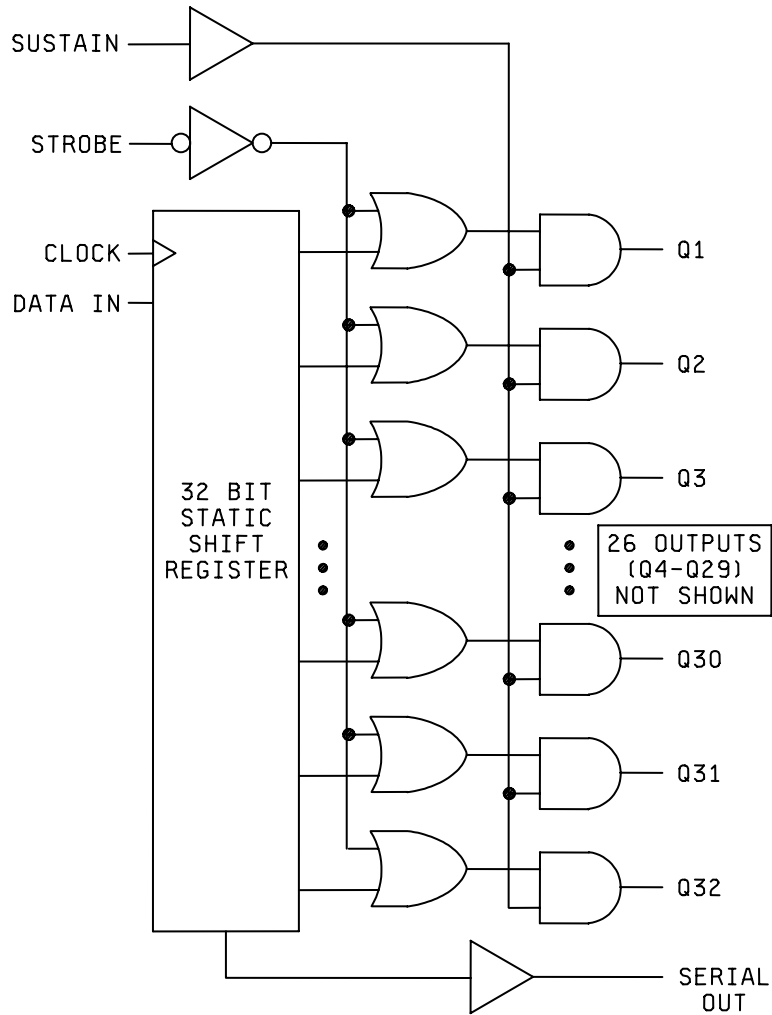


FIGURE 3. Logic symbols and functional block diagrams – Continued.

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		REVISION LEVEL D	SHEET <b>13</b>

Device type 01

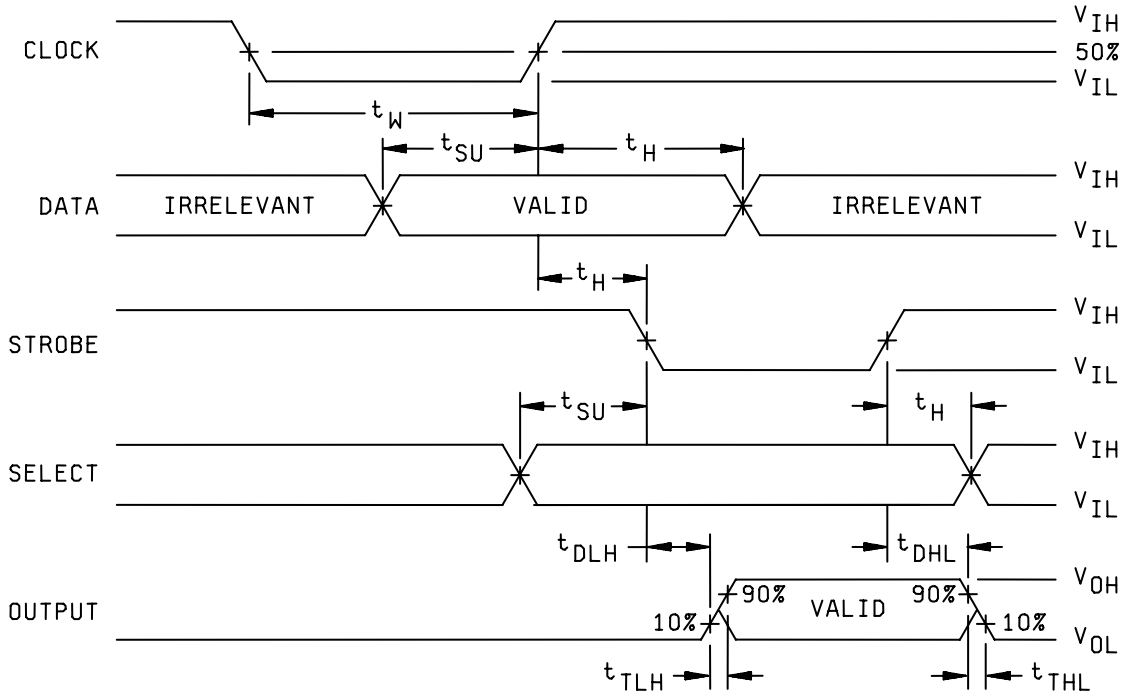
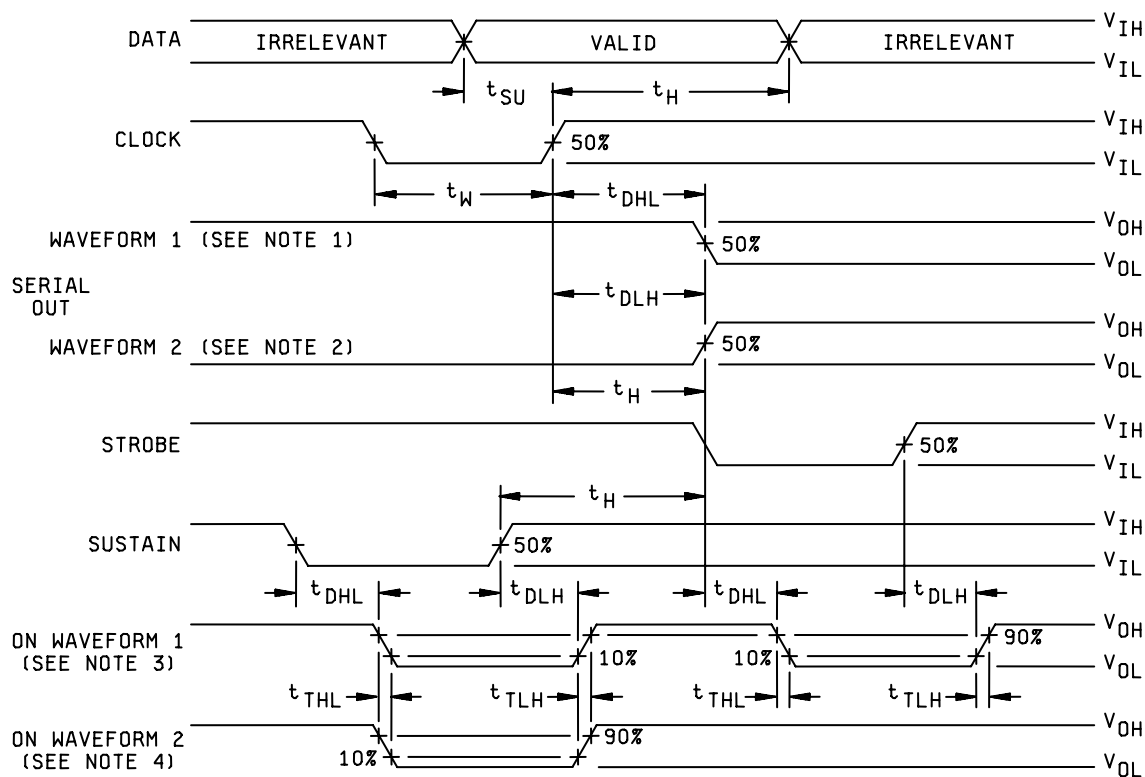


FIGURE 4. Switching waveforms.

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Device type 02



NOTES:

1. Serial data out waveform for internal condition such that a logic low is registered in R32.
2. Serial data out waveform for internal conditions such that a logic high is registered in R32.
3.  $Q_n$  output with a logic low stored in associated register  $R_n$ .
4.  $Q_n$  output with a logic high stored in associated register  $R_n$ .

FIGURE 4. Switching waveforms – Continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1.

\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

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6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-07-07

Approved sources of supply for SMD 86018 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
8601801QA	3V146	55500EJ/BQA
	<u>3/</u>	SNJ55500EJ
8601801XA	3V146	55500EFJ/BXA
	<u>3/</u>	SNJ55500EFJ
8601801ZA	3V146	55500EFD/BZA
	<u>3/</u>	SNJ55500EFD
8601802QA	3V146	55501EJ/BQA
	<u>3/</u>	SNJ55501EJ
8601802XA	3V146	55501EFJ/BXA
	<u>3/</u>	SNJ55501EFJ
8601802ZA	3V146	55501EFD/BZA
	<u>3/</u>	SNJ55501EFD

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE  
number

Vendor name  
and address

3V146

Rochester Electronics  
10 Malcolm Hoyt Drive  
Newburyport, MA 01950

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.