REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Remove vendor CAGE 34335 for device type 04. Change to military drawing format. Editorial changes throughout.	87-07-02	N A Hauck
B	Changes in accordance with NOR 5962-R160-96	96-06-26	Michael A Frye
C	Boilerplate update, part of 5 year review. ksr	05-09-01	Raymond Monnin
D	Boilerplate update, part of 5 year review. ksr	11-03-19	Charles F. Saffle

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED

REV																				
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REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Sandra Rooney

CHECKED BY
D A DiCenzo

APPROVED BY
N A. Hauck

DRAWING APPROVAL DATE
15 February 1986

REVISION LEVEL
D

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, 256 X 1-BIT LOW POWER, SCHOTTKY BIPOLAR RAM, MONOLITHIC SILICON

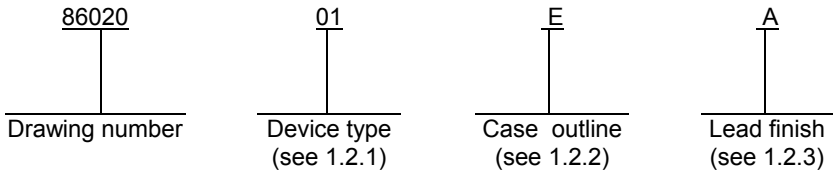
SIZE	CAGE CODE	
A	**14933**	**86020**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	27LS00	256-bit low power Schottky bipolar RAM three-state	55 ns
02	27LS00A	256-bit low power Schottky bipolar RAM three-state	45 ns
03	27LS01	256-bit low power Schottky bipolar RAM open collector	55 ns
04	27LS01A	256-bit low power Schottky bipolar RAM open collector	45 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	CDIP2-T16 or GDIP1-T16	16	dual-in-line package
F	CDFP3-F16 or GDFP2-F16	16	flat package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -0.5 V dc to +5.5 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) 1/ ..... 1.6 W
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}):
  Case E ..... (See MIL-STD-1835)
  Case F ..... (See MIL-STD-1835)
Junction temperature (T_J) ..... +175°C
Output current, inputs ..... 30 mA
DC input current ..... -30 mA to +5 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IN}) ..... 2.0 V dc
Maximum low-level input voltage (V_{IL}) ..... 0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS})..

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) TA = +125ºC, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = minimum I_{OH} = -2.0 mA $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	01, 02	2.4		V
Output low voltage	V_{OL}	V_{CC} = minimum I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	All		0.45	V
Input high level	V_{IH}	Guaranteed input logical high voltage for all inputs 1/	1, 2, 3	All	2.0		V
Input low level	V_{IL}	Guaranteed input logical low voltage for all inputs 1/	1, 2, 3	All		0.8	V
Input low current	I_{IL}	V_{CC} = maximumV_{IN} = 0.4 V	1, 2, 3	All		-0.25	mA
Input high current	I_{IH}	V_{CC} = maximumV_{IN} = 2.7 V	1, 2, 3	All		20	µA
Output short circuit current	I_{OS}	V_{CC} = maximum V_{OUT} = 0.0 V	1, 2, 3	01, 02	-20	-60	mA
Power supply current	I_{CC}	All inputs = GND V_{CC} = Maximum	1, 2, 3	02, 04		115	mA
				01, 03		70	
Input clamp voltage	V_{CL}	V_{CC} = Minimum, I_{IN} = -18 mA	1, 2, 3	All		-1.2	V
Output leakage current	I_{CEX}	$V_{CS} = V_{IH}$ or $V_{WE} = V_{IL}$ V_{OUT} = 2.4 V	1, 2, 3	All		30	µA
		$V_{CS} = V_{IH}$ or $V_{WE} = V_{IL}$ V_{OUT} = 0.4 VV_{CC} = maximum	1, 2, 3	01, 02	-30		µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay from address to output	t_{PLH}(A) t_{PHL}(A)	See figure 4 2/ 3/ 4/	9, 10, 11	01, 03		55	ns
				02, 04		45	
Delay from chip select (low) to active output and correct data	t_{PZH}(CS) 5/ _ t_{PZL}(CS) 5/		9, 10, 11	01, 03		30	ns
				02, 04		25	
Delay from write enable (high) to active output and correct data	t_{PZH}(WE) 5/ _ t_{PZL}(WE) 5/	See figures 4, 5, and 6 2/ 3/ 4/	9, 10, 11	01, 03		55	ns
				02, 04		45	
				01, 03		55	
				02, 04		45	
Setup time address (prior to initiation of write)	t_s(A)		9, 10, 11	All	5		ns
Hold time address (after termination of write)	t_h(A)		9, 10, 11	All	5		ns
Setup time data input (prior to termination of write)	t_s(DI)		9, 10, 11	01, 03	35		ns
				02, 04	30		
Hold time data input (after termination of write)	t_h(DI)		9, 10, 11	All	5		ns
Minimum write enable pulse width to insure write	t_{pw}(WE)		9, 10, 11	01, 03	35		ns
				02, 04	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay from chip select (high) to inactive output (HI-Z)	t_{PHZ}(CS)	See figure 4 2/ 3/ 4/	9, 10, 11	01, 03		30	ns
	t_{PLZ}(CS)			02, 04		25	
Delay from write enable (low) to inactive output (HI-Z)	t_{PLZ}(WE) t_{PHZ}(WE)		9, 10, 11	All		40	ns

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise, or both. Do not attempt to test these values without suitable equipment.

2/ Output is preconditioned to data in during write to ensure correct data is present on all outputs when write is terminated. (No write recovery glitch).

3/ t_{PLH}(A) and t_{PHL}(A) are tested with S closed and C_L = 50 pF with both input and output timing referenced to 1.5 V.

4/ For open collector (03, 04), all delays from write enable ($\overline{WE}$) or chip select ($\overline{CS}$) inputs to the data output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$, and $t_{PZL}(\overline{CS})$ are measured with S closed and C_L = 50 pF and with both the input and output timing referenced to 1.5 V.

5/ For three-state output (01, 02) $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S open, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S open and C_L < 5 pF and are measured between the 1.5 V level on the input to the V_{OH} -500 mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S closed and C_L < 5 pF and are measured between the 1.5 V level on the input and the V_{OL} +500 mV level on the output.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A, 8B, 9, 10, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroups 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I. Subgroups 7, 8A, and 8B shall consist of verifying the truth table specified on figure 2.

Device Types	All
Case Outlines	E and F
Terminal Number	Terminal Symbol
1	A_1
2	A_0
3	$\overline{CS}$
4	$\overline{CS}$
5	$\overline{CS}$
6	$\overline{D}_0$
7	A_4
8	GND
9	A_5
10	A_6
11	A_7
12	$\overline{WE}$
13	D_1
14	A_3
15	A_2
16	V_{CC}

FIGURE 1. Terminal connections.

Input			Data output Status D_0 (t_n + 1)	Mode
$\overline{CS}$	$\overline{WE}$	D1		
H	X	X	Output disabled	No selection
L	L	L	Output disabled	Write '0'
L	L	H	Output disabled	Write '1'
L	H	X	Selected bit (inverted)	Read

H = High
L = Low
X = Don't care.

FIGURE 2. Truth table.

DEVICE TYPES 01 AND 02

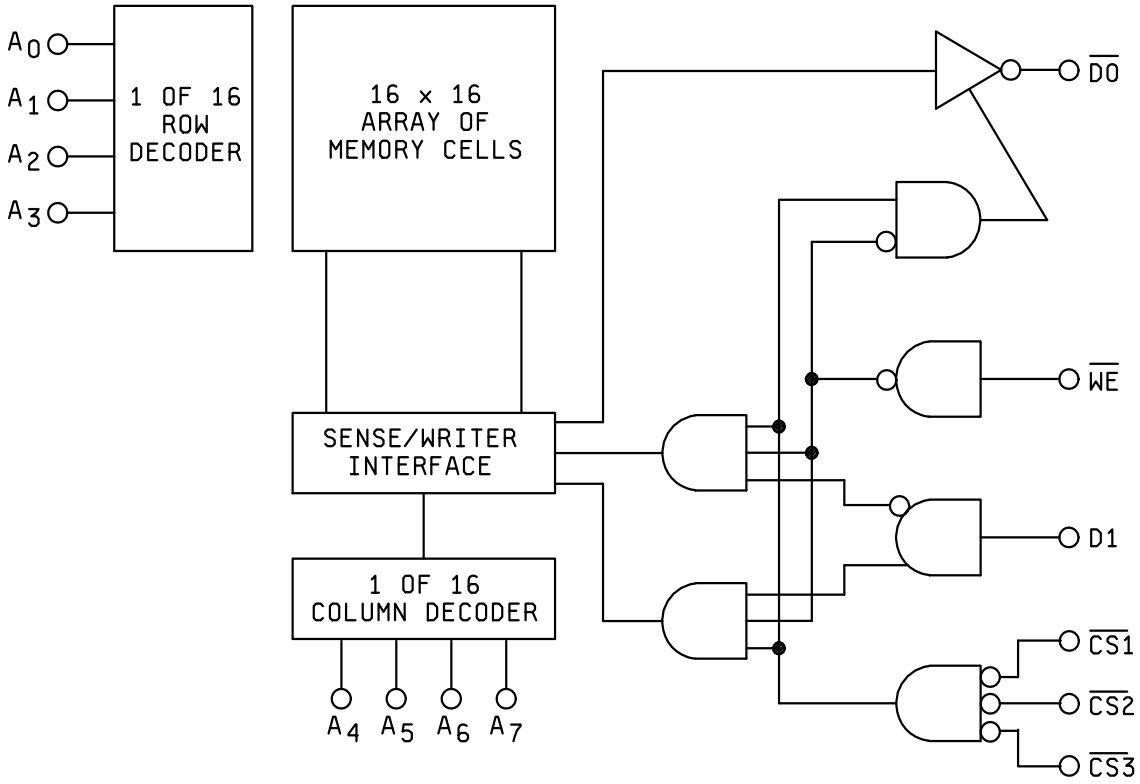


FIGURE 3. Logic diagrams.

DEVICE TYPES 03 AND 04

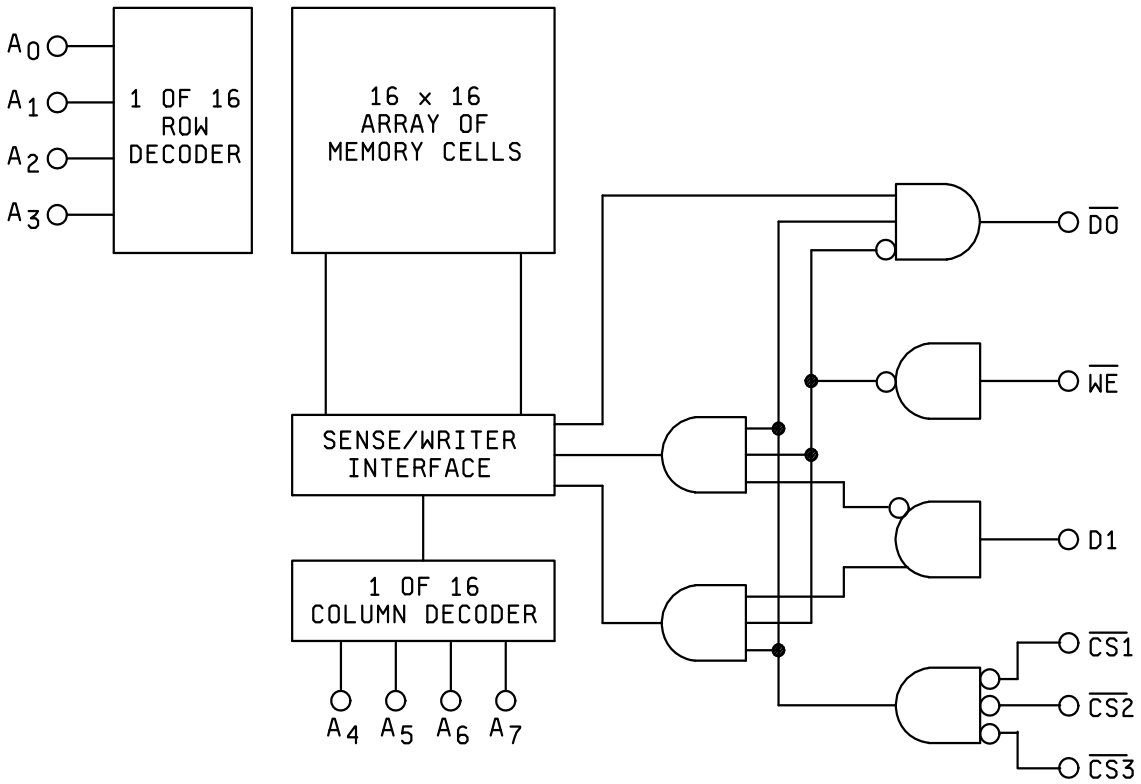


FIGURE 3. Logic diagrams - Continued.

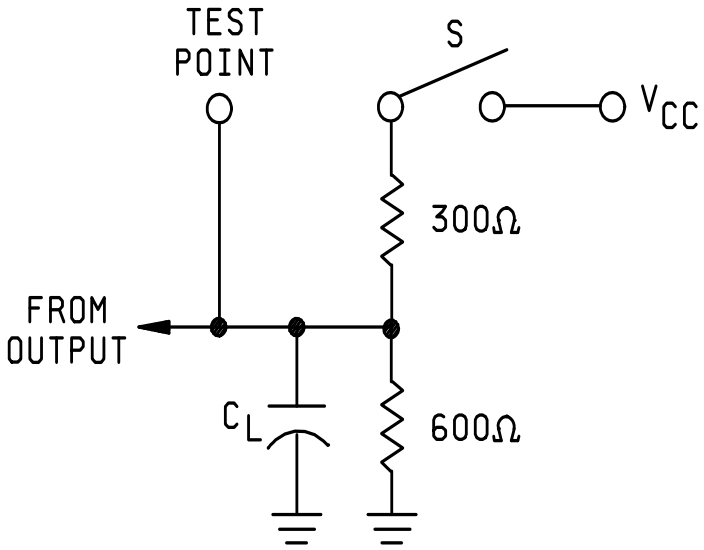


FIGURE 4. Switching test circuit.

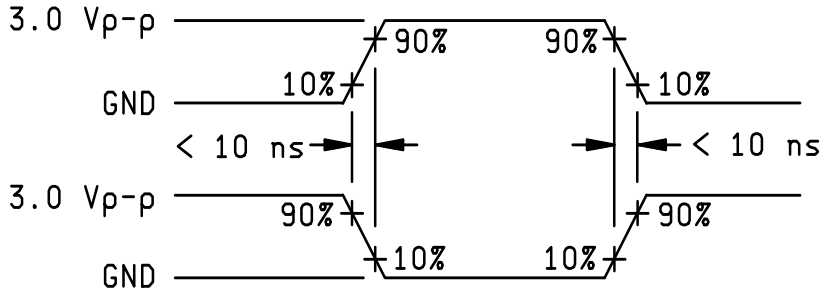
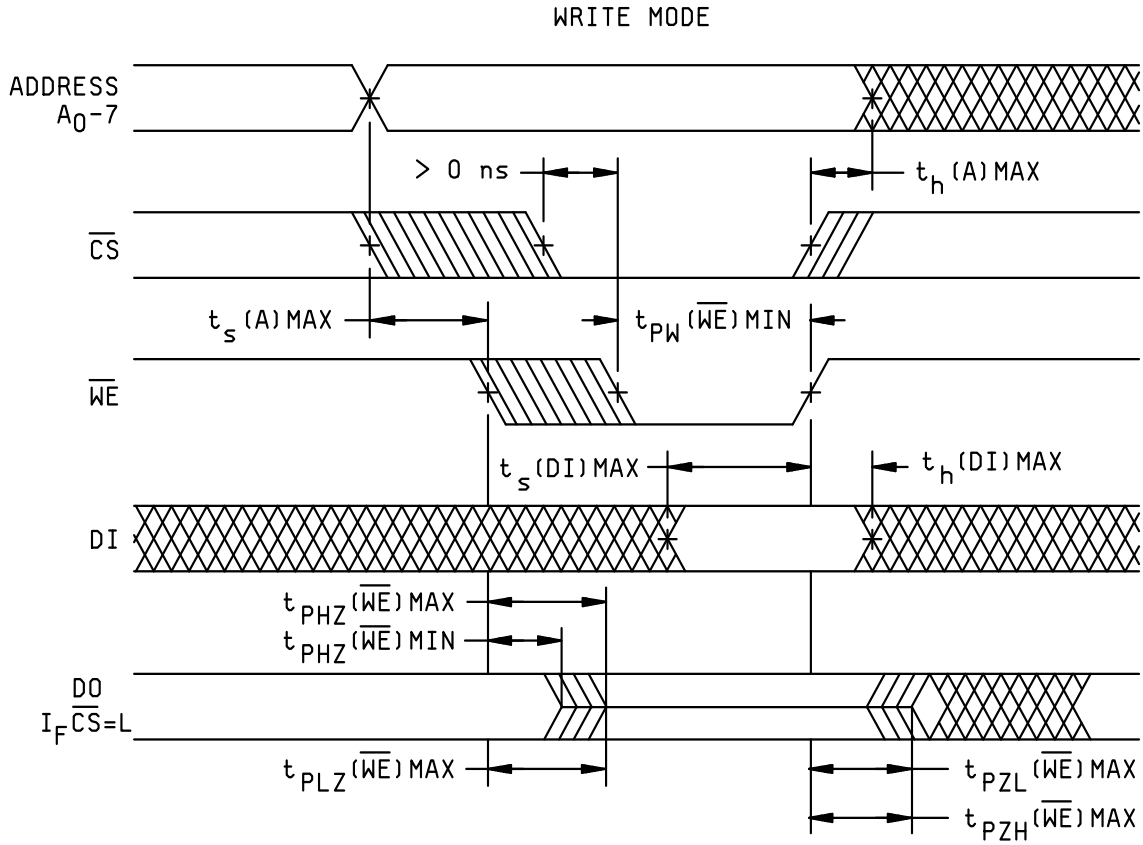
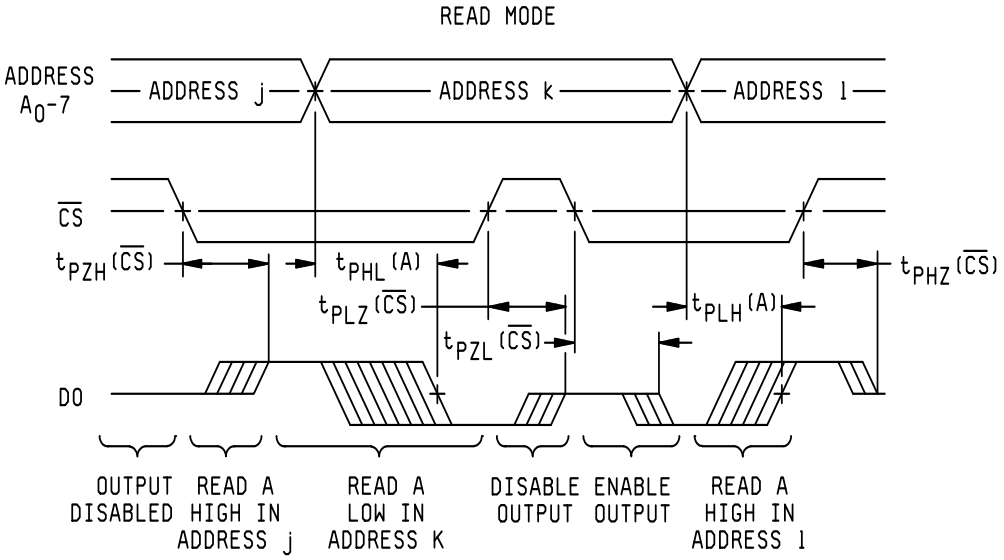


FIGURE 5. Switching test waveform.



Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max must be allowed before the address may be changed again. The output will be inactive (floating for device types 01 and 02) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

FIGURE 6. Switching waveforms.



Switching delays from address and chip select inputs to the data output. For devices 01 and 02, disabled output is "OFF", represented by a single center line. For devices 03 and 04 a disabled output is HIGH.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUT	OUTPUT
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

FIGURE 6. Switching waveforms - Continued.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-03-19

Approved sources of supply for SMD 86020 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8602001EA	3/ 3V146 0DKS7	AM27LS00/BEA 27LS00/BEA GEM09201QEA
5962-8602001EC	0DKS7	GEM09201QEC
5962-8602001FA	3/ 3V146 0DKS7	AM27LS00/BFA 27LS00/BFA GEM09201QFA
5962-8602001FC	0DKS7	GEM09201QFC
5962-8602002EA	3/ 3V146 0DKS7	AM27LS00A/BEA 27LS00A/BEA GEM09202QEA
5962-8602002EC	0DKS7	GEM09202QEC
5962-8602002FA	3/ 3V146 0DKS7	AM27LS00A/BFA 27LS00A/BFA GEM09202QFA
5962-8602002FC	0DKS7	GEM09202QFC
5962-8602003EA	3/	AM27LS01/BEA
5962-8602003FA	3/	AM27LS01/BFA
5962-8602004EA	3/	AM27LS01A/BEA
5962-8602004FA	3/	AM27LS01A/BFA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950
0DKS7	Sarnoff, David Research Center 201 Washington Road Princeton, NJ 08540-6449